Front-End Electronics Control and Monitoring for the LHCb Upgrade

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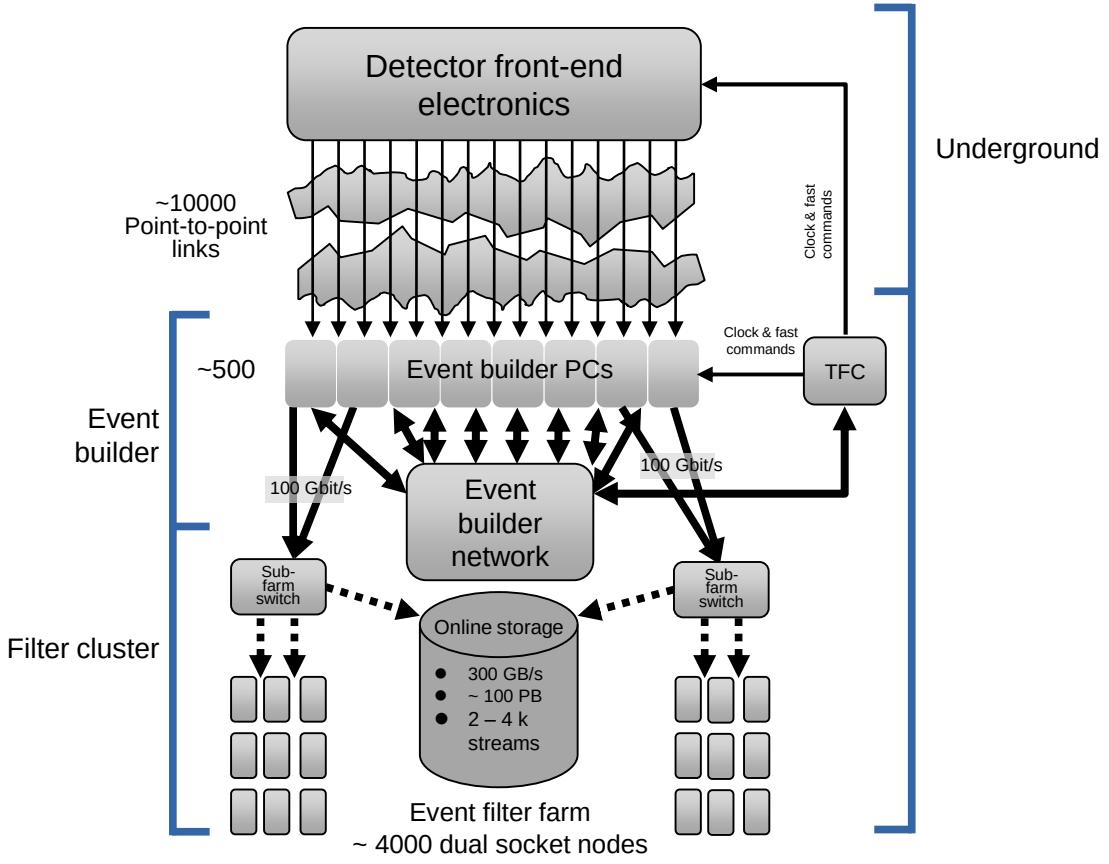
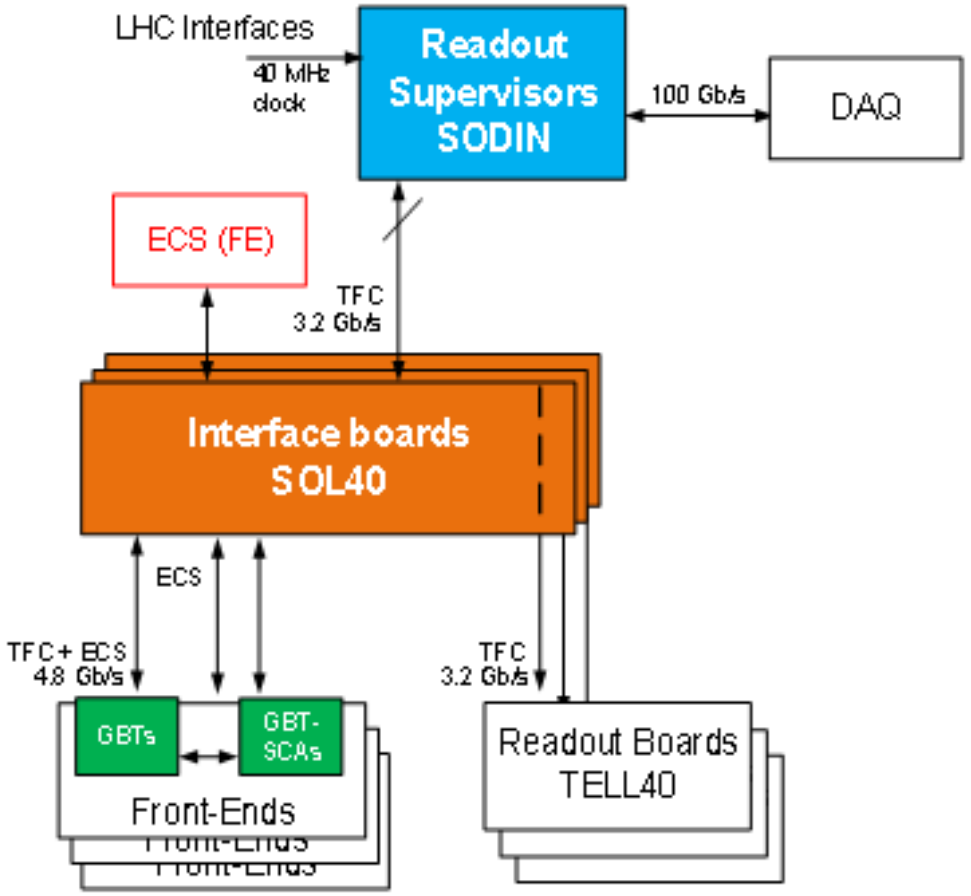
The LHCb Upgrade

- No hardware trigger on the data readout
- All the sub detectors will completely or partially refurbish their electronics
- Optical links used for data readout, TFC (timing and fast control) and slow control (ECS)
  - CERN GBT protocol used across the whole detector

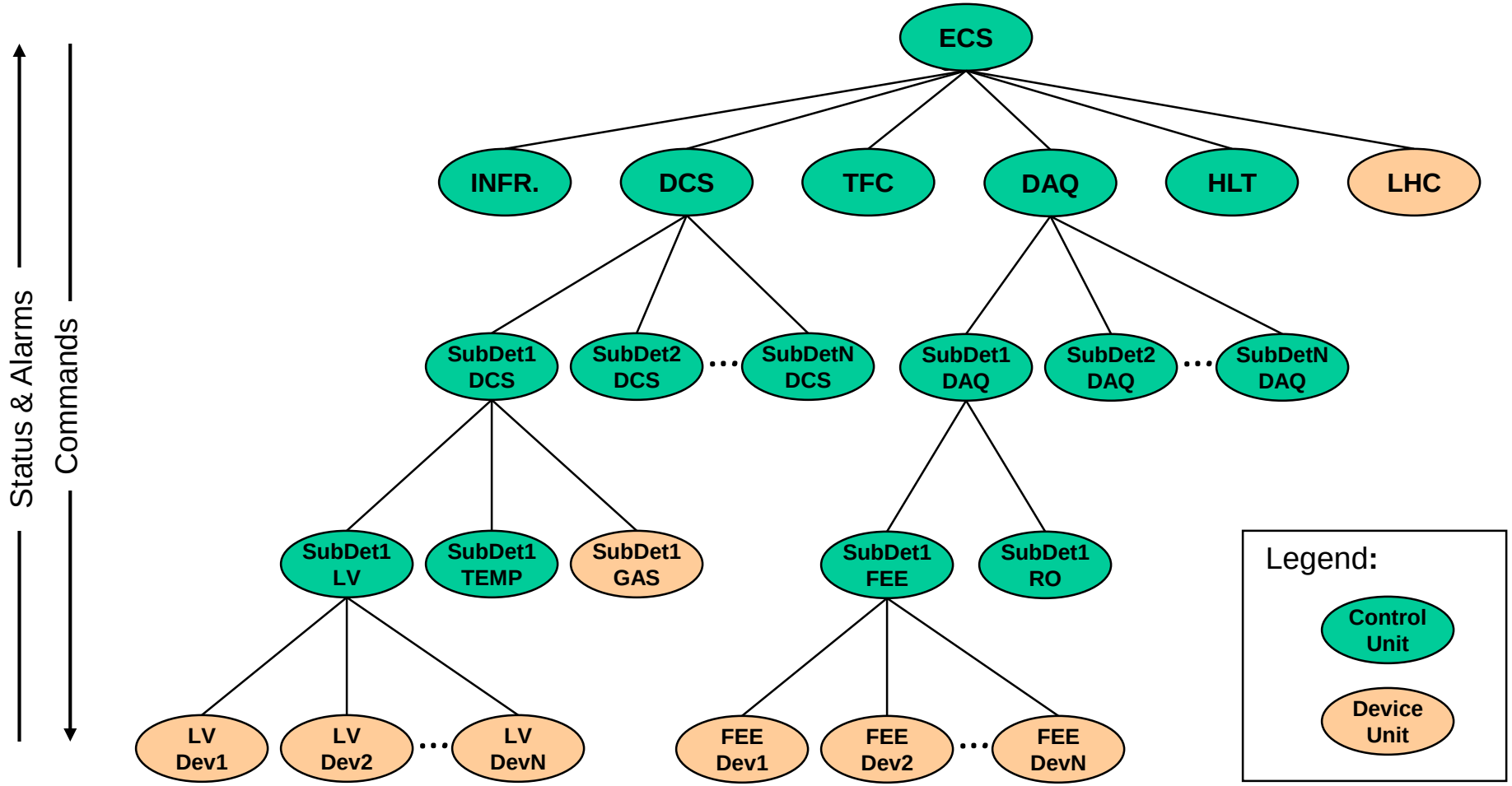


TFC and Slow Control architecture

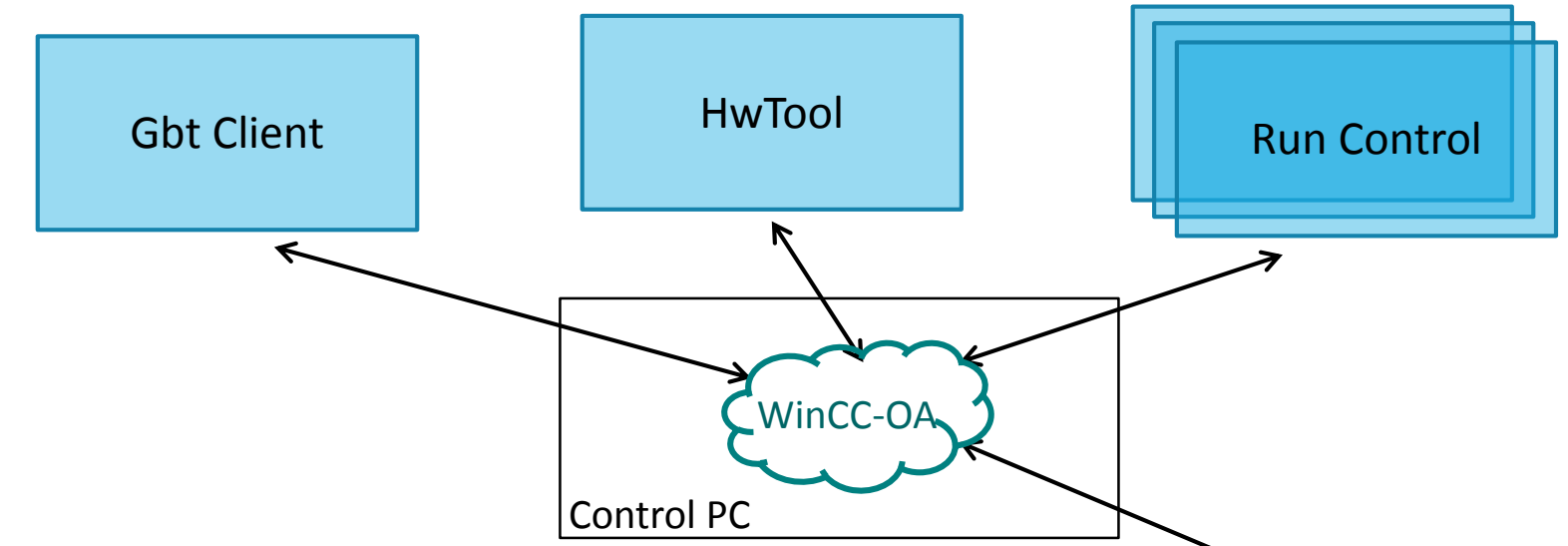


- PCIe40 board for readout, TFC and ECS (three firmware flavors)
  - 48 bidirectional optical links to FEE
  - 2 dedicated optical link to distribute timing information to readout
  - 100 Gbps PCIe gen 3
- CERN GBT chipset used by all the sub detectors
  - GBTx chip (high speed link)
  - GBT-SCA (user buses like I2C, JTAG…)
- Data paths and Control paths are separated to prevent lockouts

The LHCb Run Control System



Electronics Upgrade Control System



Components:

- Run Control
- Hardware Tool
- WinCC_OA
- GBTServer (PCIe lib + DIM)
- PCIe driver
- SOL40 (optical drivers and firmware)
- Front-End (GBT chipset)

Requirements and challenges for ECS

Requirements

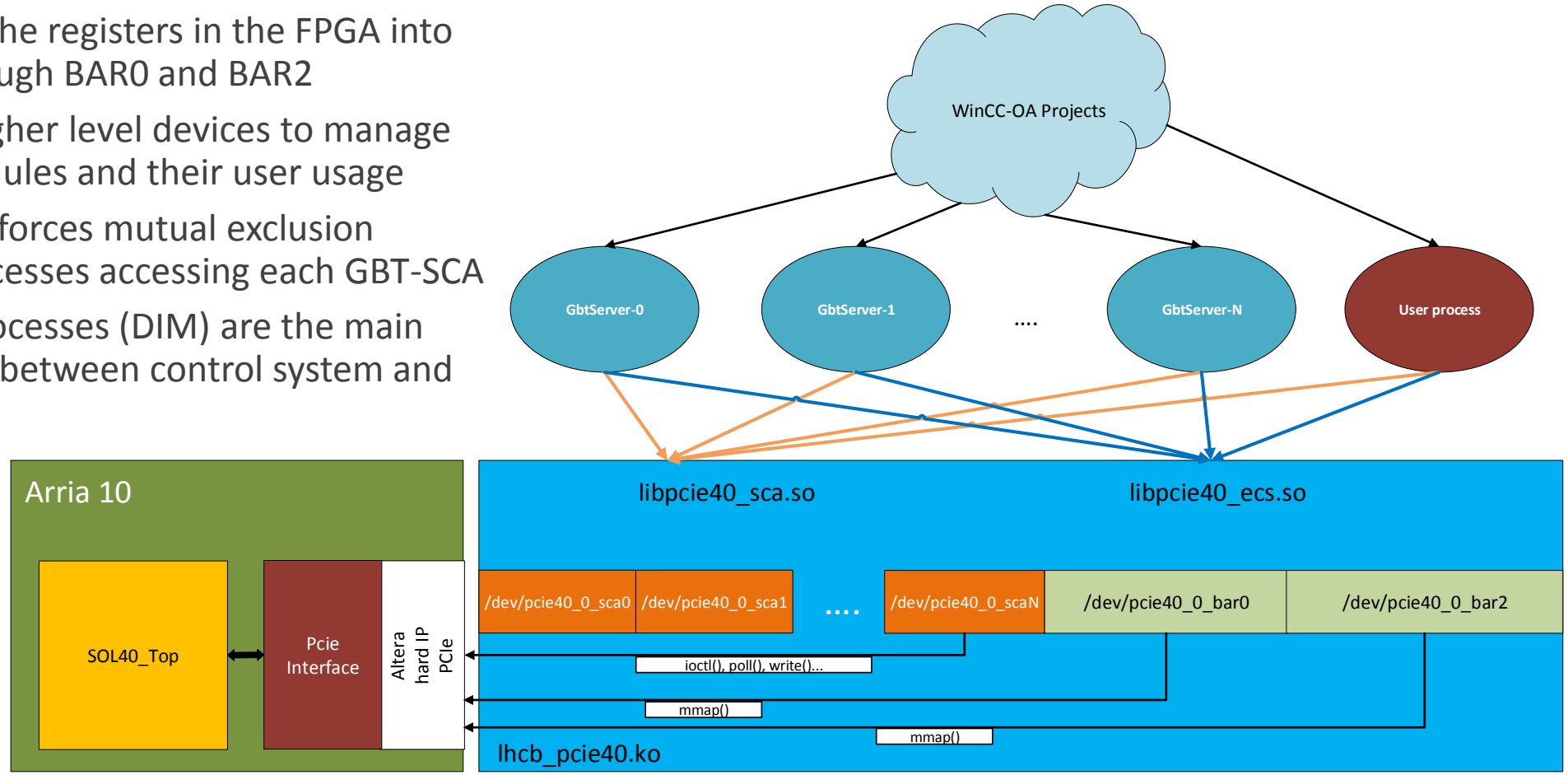
1. It has to relieve the central control system from the GBT-SCA protocol handling
2. Preferably relieve the distributed software units from micromanaging the GBT-SCA operations.
3. Firmware must be able to serve a maximum of 48 GBT links, each serving a maximum of 22 SCAs each
4. Must allow Run Control to configure all the Front-End devices simultaneously

Challenges

1. GBT-SCA was not made for speed but for radiation hardness, user has to wait for reply every time.
2. Simple Front end transactions require several SCA transactions.
3. We want to pack as much functionality in as little boards as possible

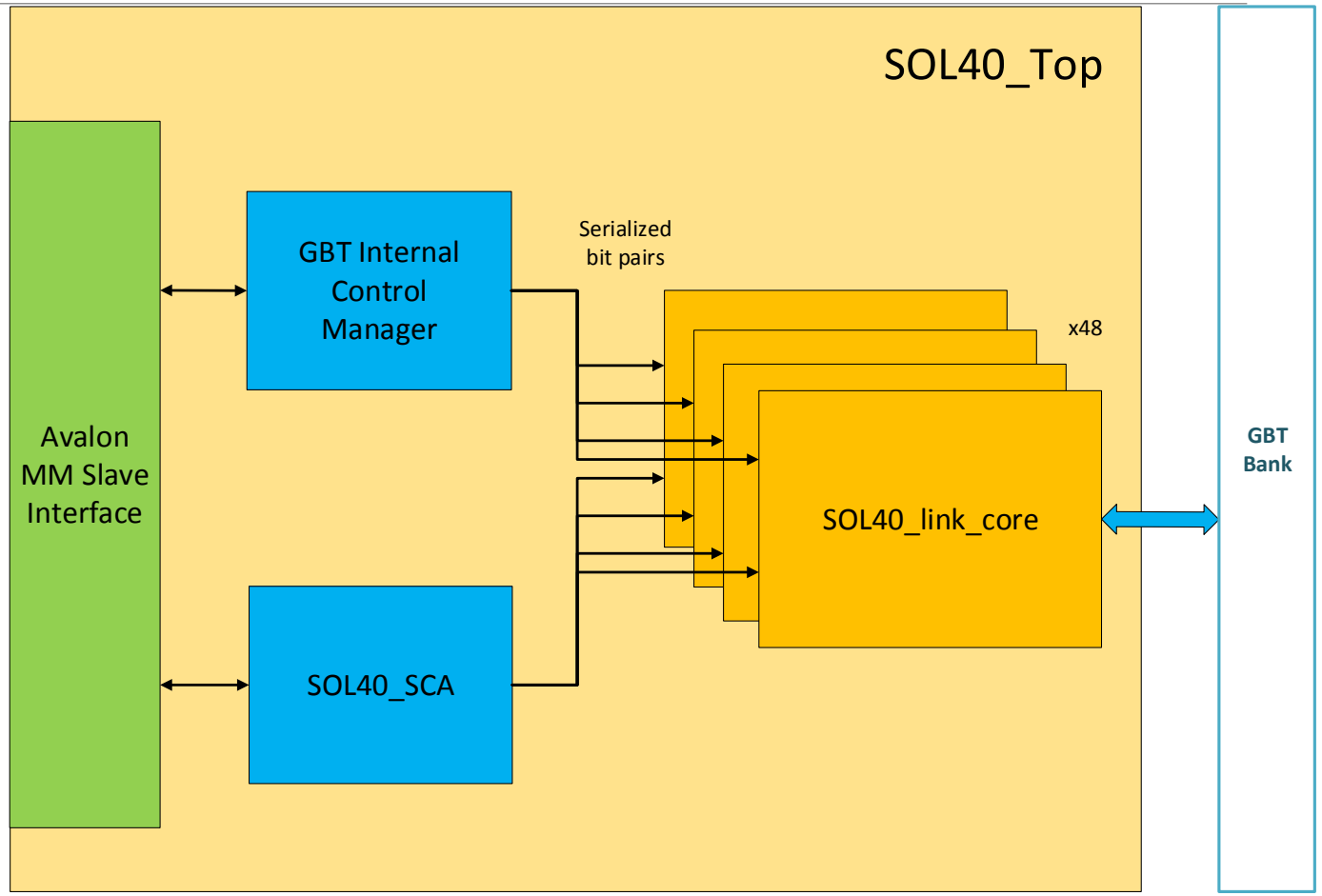
Software architecture

- Driver maps the registers in the FPGA into memory through BAR0 and BAR2
- Additional higher level devices to manage GBT-SCA modules and their user usage
- SCA driver enforces mutual exclusion between processes accessing each GBT-SCA
- GbtServer processes (DIM) are the main intermediate between control system and hardware.



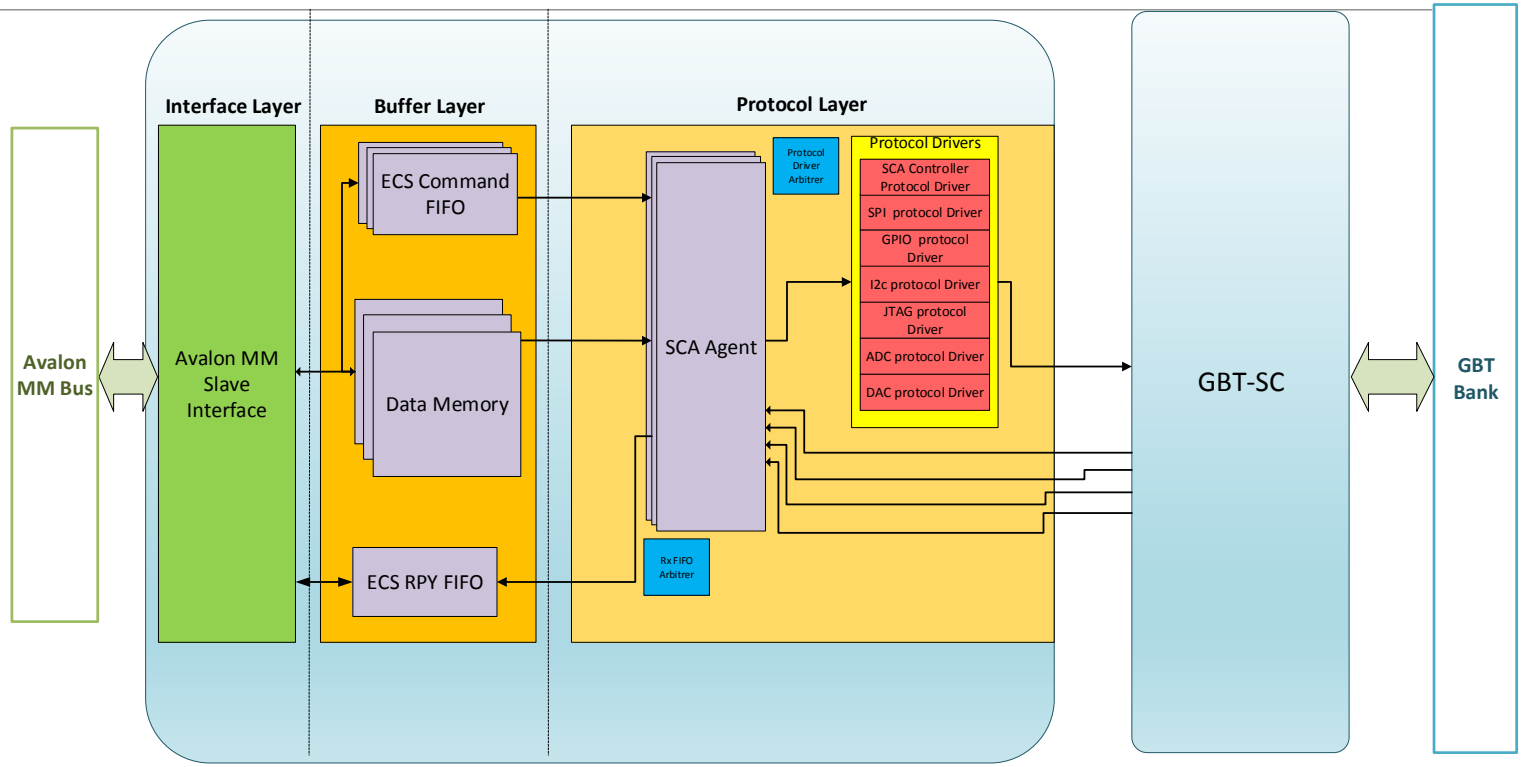
SOL40 firmware core

- SOL40_SCA:
  - Shares resources between many links
  - Handles conversion of ECS commands into SCA commands
- GBT Internal Control Manager:
  - Manages communication with the IC (Internal Control) of the GBTx in each of the 48 links
- SOL40_link_core
  - Implements e-link mapping for every sub-detector
  - Possibility of mix and match
  - Implements delays to TFC commands



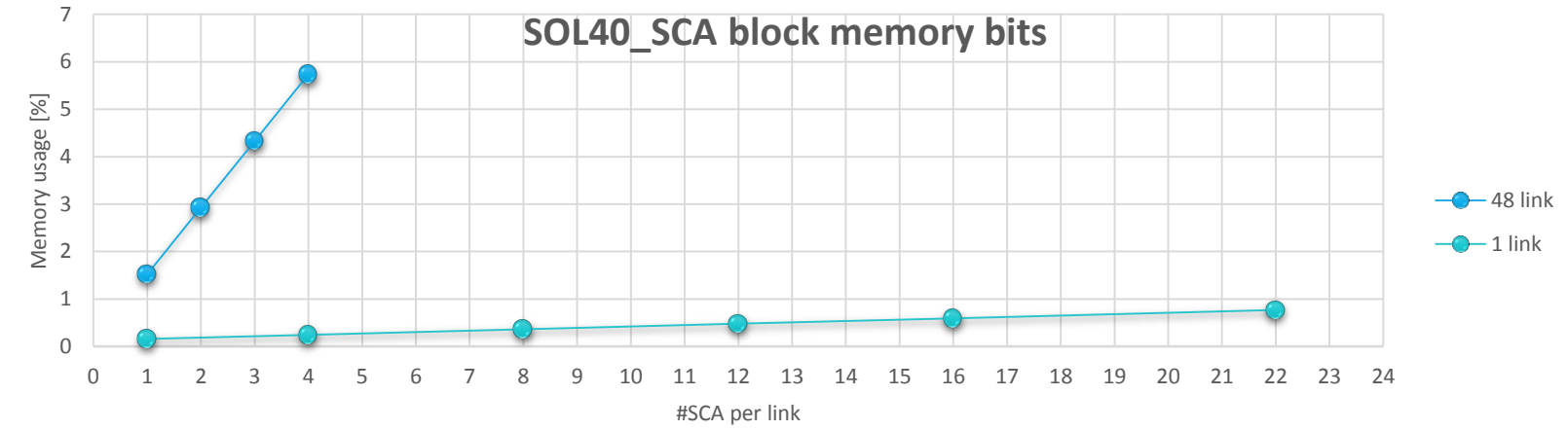
SOL40_SCA firmware core

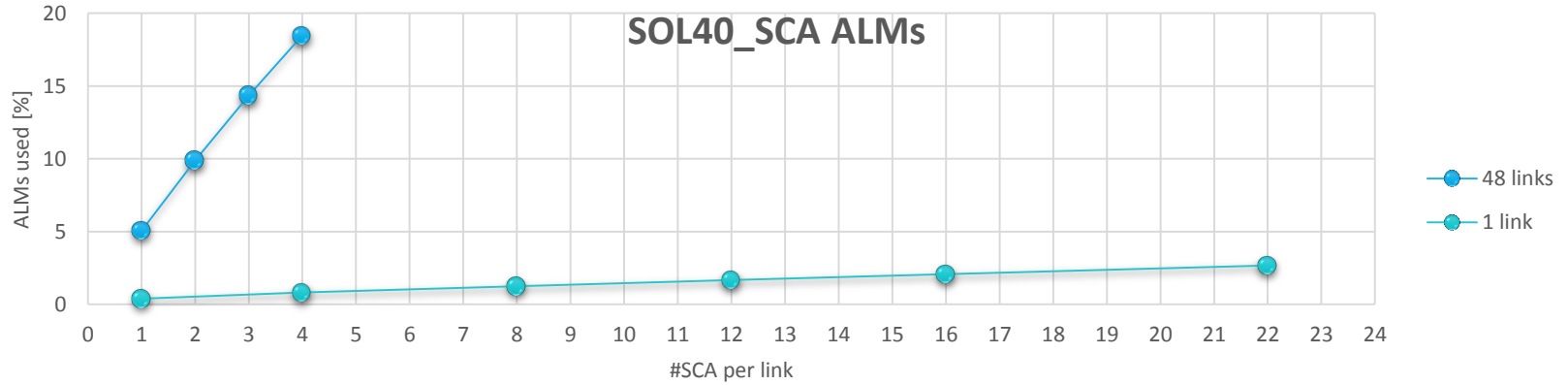
- GBT-SC core responsible for SCA packets serialization and encoding.
- User layers adapted to use less logic (more memory) and be configurable on compilation
- 1 user command can be multiplied into several SCA commands thanks to protocol layer.
- Each SCA operated in parallel
- Commands are identified with an ID given by the driver.
- Memory and FIFO size configurable



Command word 0	Gbt Link [31:24]	SCA elink index [23:16]	SCA channel number [15:8]	Cmd code [7:0]
Command word 1	Protocol specific word [31:0]			
Command word 2	Data Address [31:16]		Data length [15:0]	
Command word 3	Command Identifier [31:0]			

SOL40_SCA FPGA resource usage





Use cases

RICH subdetector:

- Remote configuration of Kintex 7 FPGA
  - ~1500 FPGAs
  - < 3 s per FPGA
  - Partial configuration in case of SEUs (TMR)
- Configuration of the Data Link GBTx chips (2.3k)
- Configuration and monitoring of custom SPI devices (30k chips)

SciFi subdetector:

- ~580 TFC/ECS GBT links
  - ~4700 IGLOO 2 FPGAs (~1 min per FPGA, flash based)
  - ~2400 Data links
  - ADC, I2C and GPIO for monitoring
- Configuration and monitoring of FPGA firmware through I2C

Summary

- Design of the Front-End monitoring and configuration system takes the interconnections between several parts into account
  - Software relieved on any low level protocol handling and most send-wait cycles
  - Control system only has to send 1 command to firmware for several SCA commands to be executed
- New design is configurable to adapt to every sub-detector's needs.
- Resources need to be shared further to be able to reach all the SCAs in the worst cases, without raising the number of SOL40 boards
- Many parts of the system already tested and the architecture will be ready for commissioning the detector