

# **FELIX based readout of the Single-Phase ProtoDUNE detector**

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EP-DT  
Detector Technologies



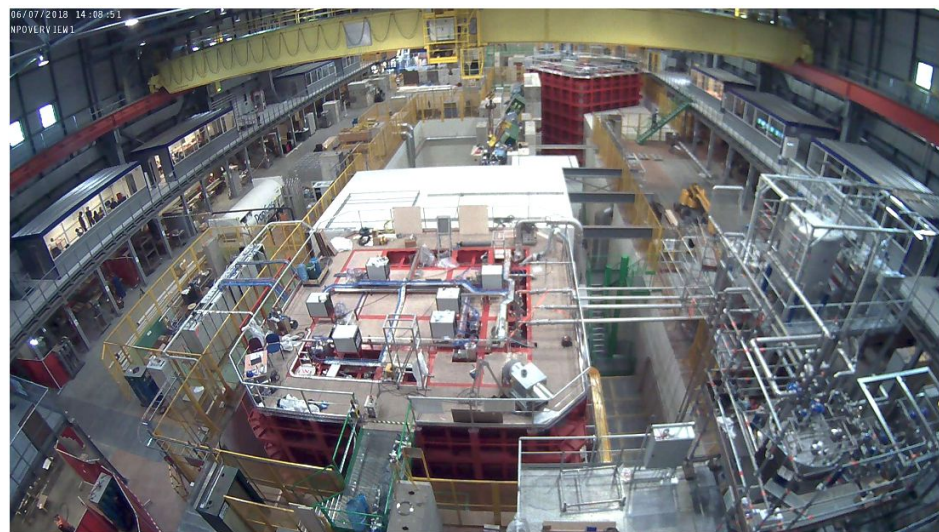
# ProtoDUNE Single Phase

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Largest monolithic single phase LArTPC detector and test beam built to date:

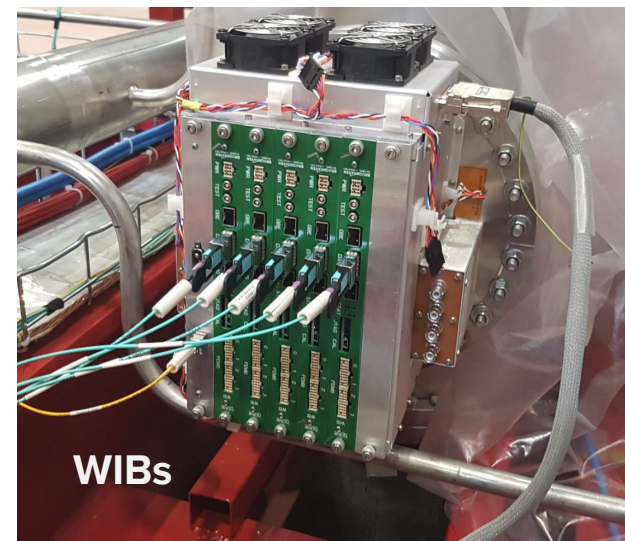
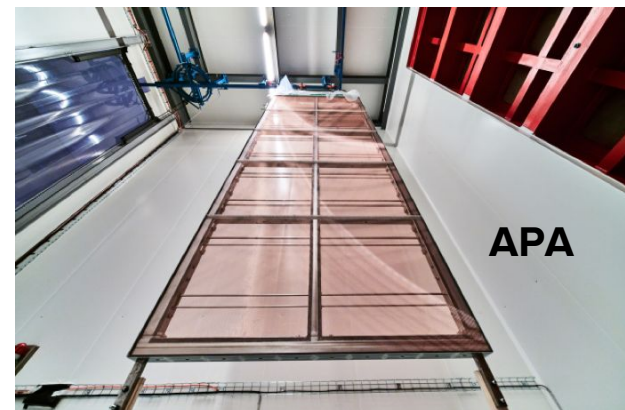
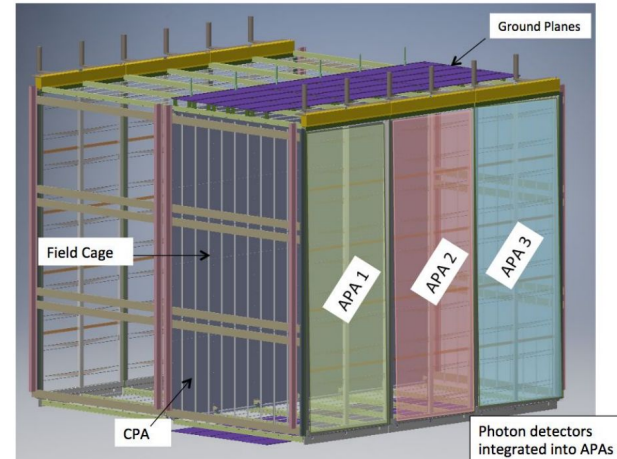
- Goal is to **validate detector design, construction and data acquisition solutions** for DUNE's Single Phase Far Detectors
  - 10x10x10 **LArTPC**
  - 800 tonnes of LAr
  - Located **on surface** → **external trigger** needed
- **Extreme schedule:**
  - Project launch: Q1 2016
  - Expected data taking: **Q4 2018**
- DAQ approach: use **ready-to-use solutions**
  - minimise development time

More on ProtoDUNE in yesterday's plenary [talk](#) by Karol Hennessy



# Data flow and volume

- **LArTPC** → ionisation tracks are collected by the wires of the **Anode Plane Assemblies (APAs)**
- **Cold electronics** in the detector **digitise signals** recorded by wires at **2 MHz**
- **Warm interface boards (WIBs)** then group the resulting channels into **frames**, each of which consists of a single **500 ns time slice of the grouped channels** (128 or 256)
- Output via **optical links** to DAQ:
  - 2x 9.6 Gb/s or 4x 4.8 Gb/s supported, depending on readout solution
  - Continuous **timestamped data frame** streams
- Each APA (2560 channels) is read out by 5x WIBs for a **total payload of about 74 Gb/s**



# FELIX readout solution for ProtoDUNE

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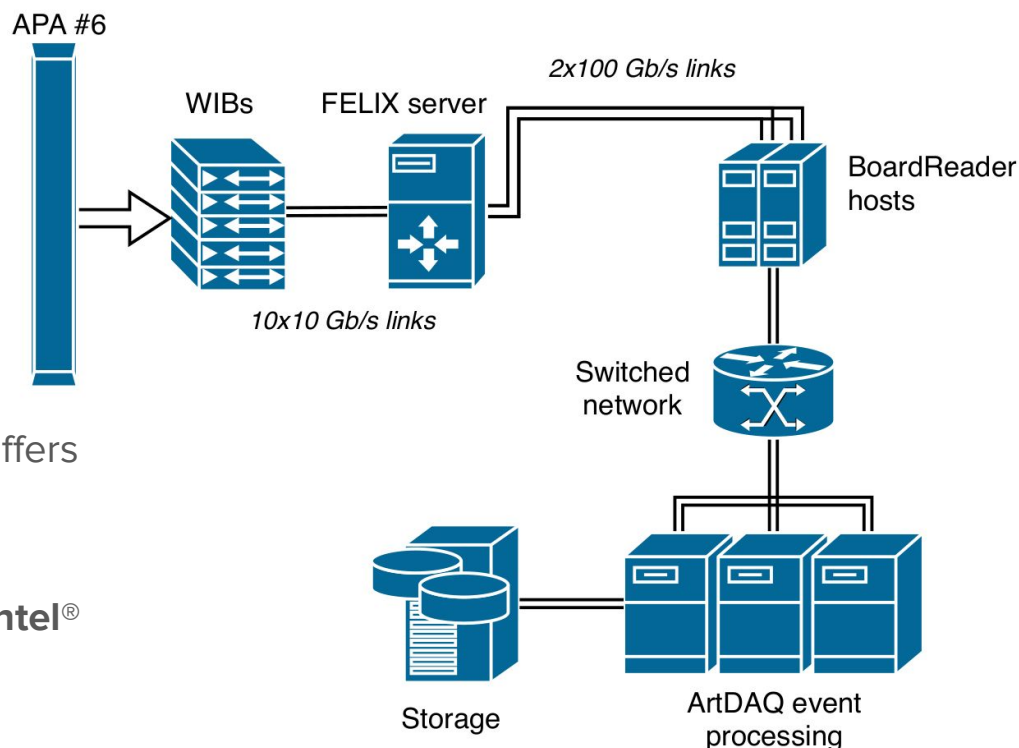
The **F**ront-**E**nd **L**ink e**X**change will be the readout system of the ATLAS experiment after LS2:

- Approach relying on **servers and COTS to do data processing**
  - PCIe based FPGA custom card
- **Networked scalable system**

In **ProtoDUNE Single Phase**:

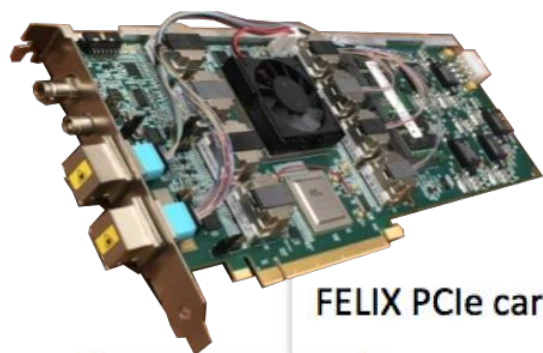
- **Software trigger selection**
  - State of the art, lock-free circular buffers
- **Software compression**
  - Will be hardware accelerated with **Intel® QuickAssist Technology (QAT)**

**Plan to read out a full APA (1 of 6)**



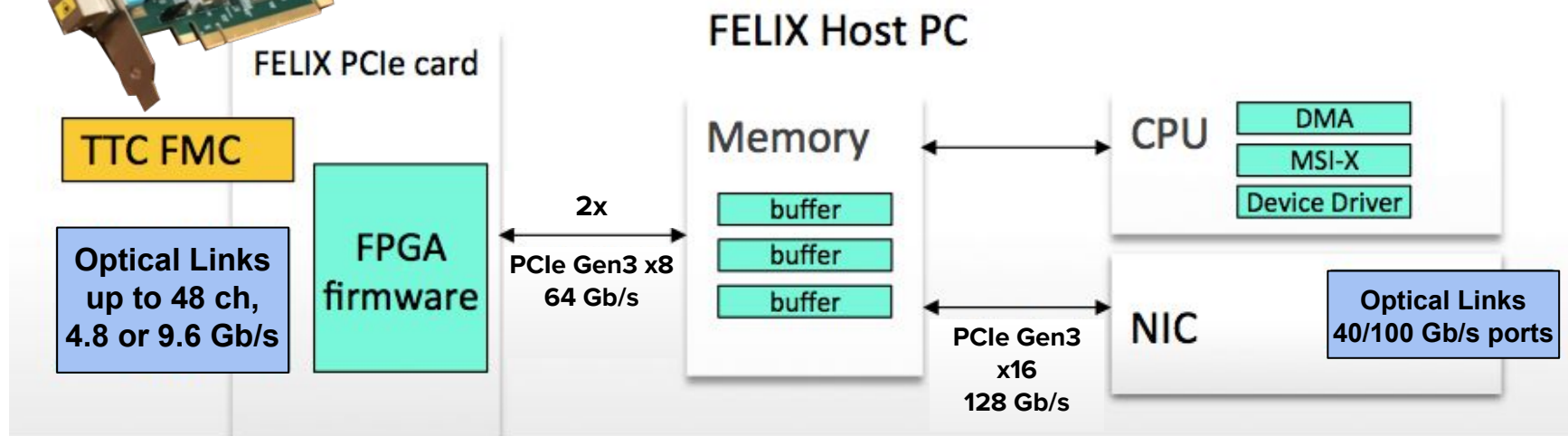


- **Front-End Link eXchange**
  - Routes data between detector electronics and high-speed network-connected hosts (data, control, timing, trigger)
  - **Move data handling away from custom hardware directly connected to the detector electronics**
  - PCIe card(s) on a host running routing software (*felixcore*)



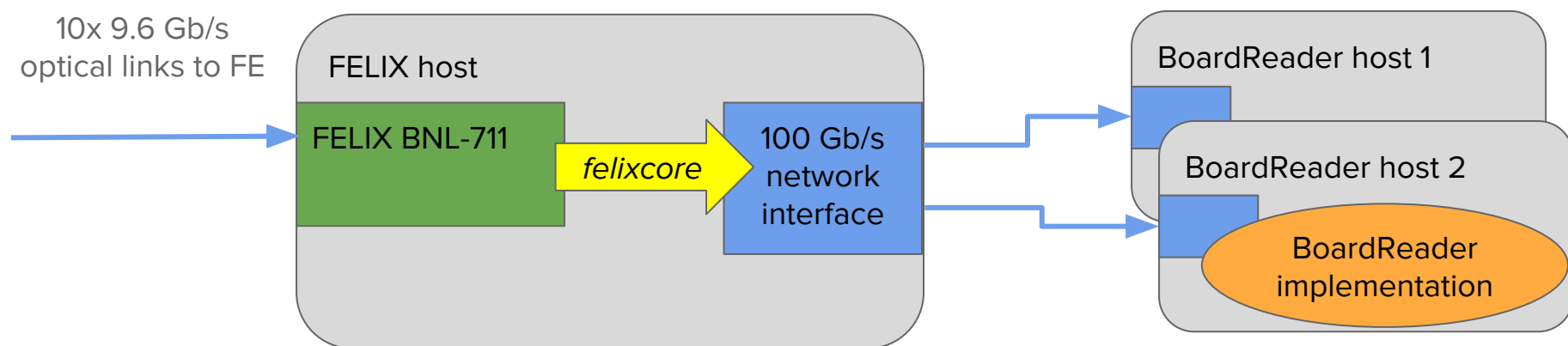
FELIX PCIe card

- **BNL-711**
  - Xilinx Kintex Ultrascale
  - Up to 48 optical links (MiniPODs)



# FELIX readout implementation

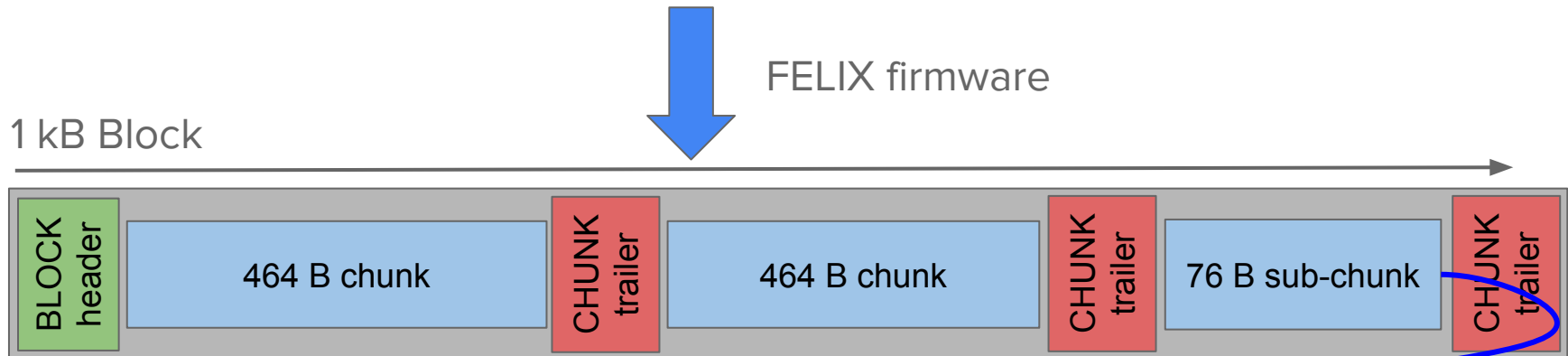
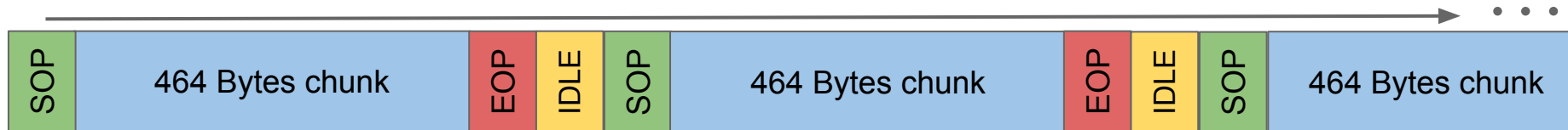
- A FELIX card receives **464 bytes frames at fixed 2 MHz** from 10x 9.6 Gb/s optical links -> about **74 Gb/s total data rate** excluding 8b/10b encoding
- Use of FELIX software suite to **publish frames through network** maintaining the 10 separated link streams: *felixcore*
- **Mellanox ConnectX-5 100 Gb/s** used for networking
- **Trigger matching and compression** performed in custom “BoardReader” applications



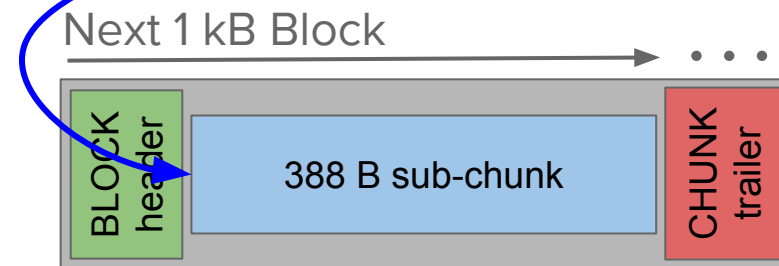
# Data flow overview

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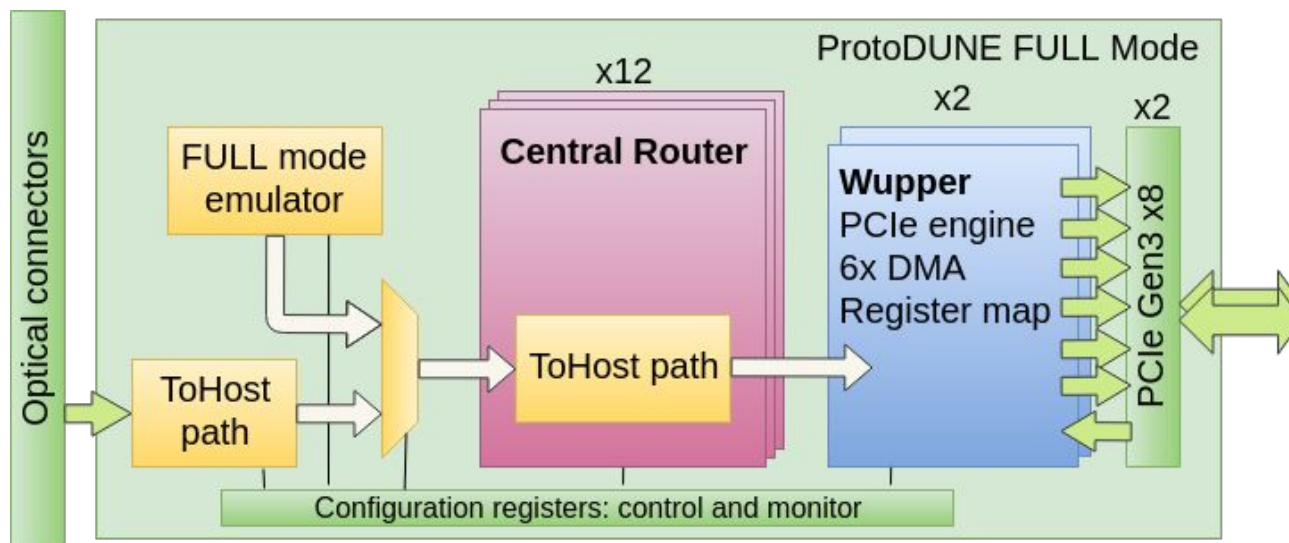
- Incoming data framed by SOP/EOP into fixed size chunks



- Firmware prepares **1 kB “blocks”** for **DMA transfer**
- Software processes these blocks from host memory, **parsing chunks and sub-chunks**



- In order to sustain the high rate of incoming frames (2 MHz) and high throughput requirements, **modest modifications of the firmware** were introduced:
  - Chunks are packed together in order to **minimise memory-copy effort** at the publisher software level. **Rate of networking calls** is also greatly reduced.
  - DMA payload (**block**) **size increased** in order to optimise parsing.
  - **Multiple descriptors** (one per link) DMA'ing into different memory areas.

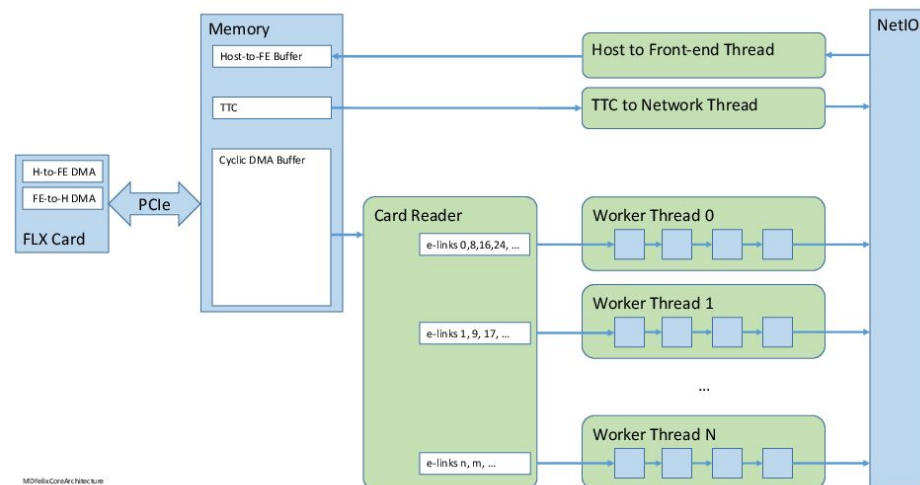




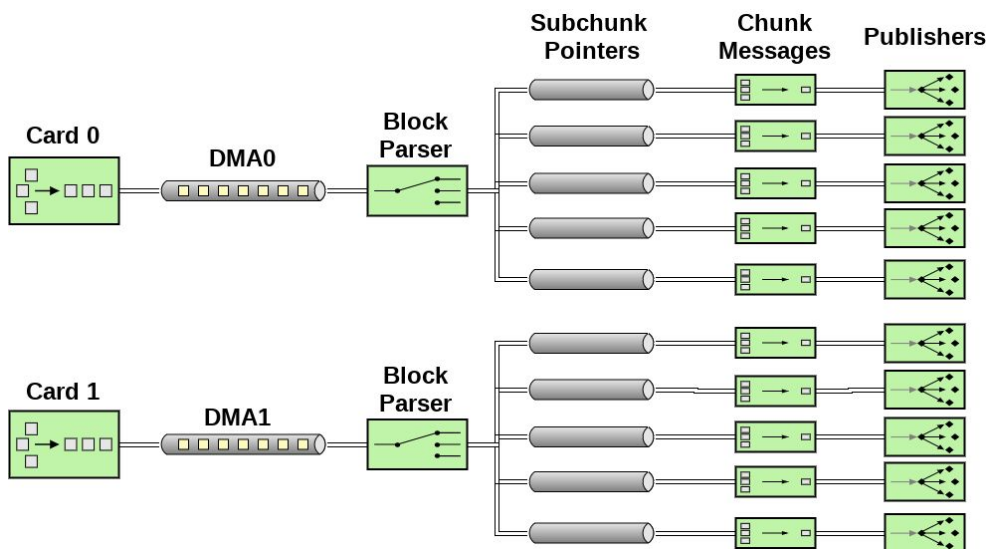
# The *felixcore* application

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- In the ATLAS generic version, *felixcore* is in charge of **routing data from the detector to the networked software clients** and vice versa.
- Supports **several back-ends**, such as **TCP/IP** and **Infiniband** integrated in the **NetIO** messaging layer.



MDNetCoreArchitecture

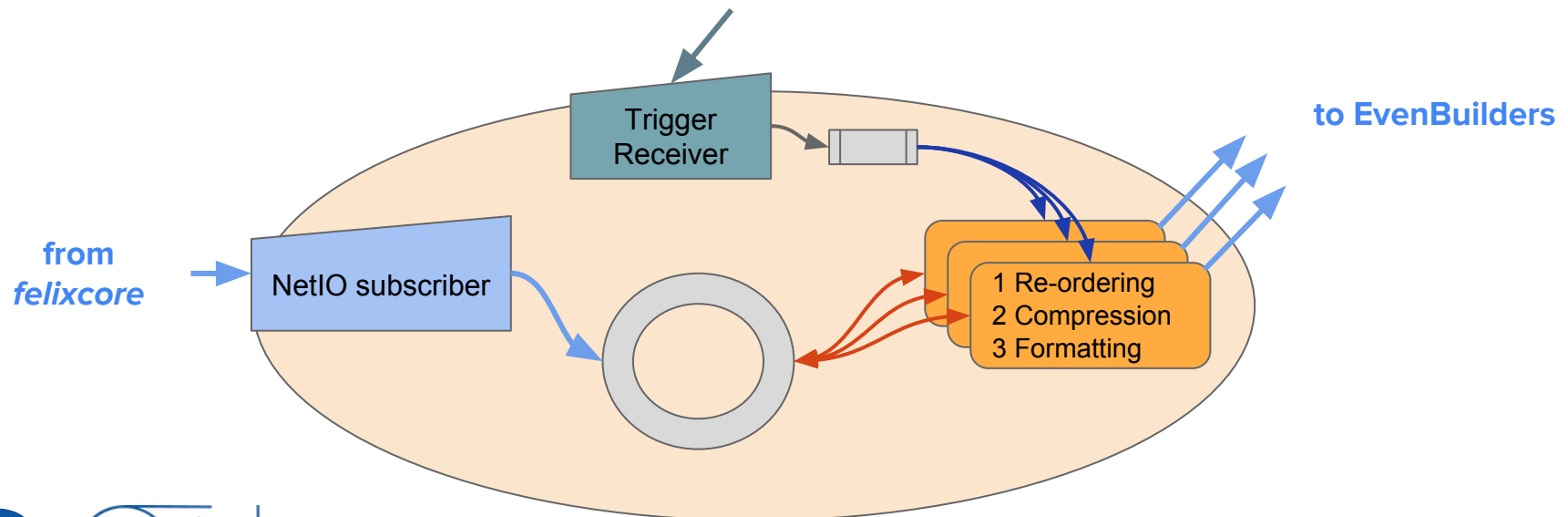


- In **ProtoDUNE** only **uni-directional traffic from detector** is used and data fragments have a fixed size
- **Optimised** in order to achieve the required data throughput:
  - Simplified data routing by means of a **dedicated threads per physical link**
  - **Scatter/gather technique** used in the **TCP/IP**

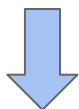
# FELIX BoardReader implementation

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- The FELIX BoardReader is implemented as part of the [artdaq](#) data acquisition framework
- **Receives and buffers data continuously**
  - One subscriber thread for each link populating a SPSC queue (lock-free implementation from the [Folly](#) library)
- A specialized thread **extracts data from buffer, matching a 5 ms time-window** based on the **trigger request** from EventBuilders **at 25Hz** (baseline rate)
- Re-ordering and **compression of data**
- Complete fragment with compressed data is sent downstream to EventBuilders



- **ProtoDUNE target compression factor set to 4** (implications in storage hardware projections)
  - **Efficient compression can be achieved by re-ordering the frames** to contiguous ADC data for individual channels
- Compression should also keep up with the 25 Hz trigger rate and the about 46 Mbytes payload size → **Hardware accelerated compression**



- **Intel® QuickAssist Technology (QAT)**
  - Under study at CERN
  - Can offload the CPU and compress faster
- **Intel® Xeon® Scalable processors** with **integrated QAT support used in BoardReader hosts**
- Allows a **reduction of the time** required for the compression of one data fragment
  - from about 100-200 ms (software only)
  - **to about 5-9 ms (accelerated)**

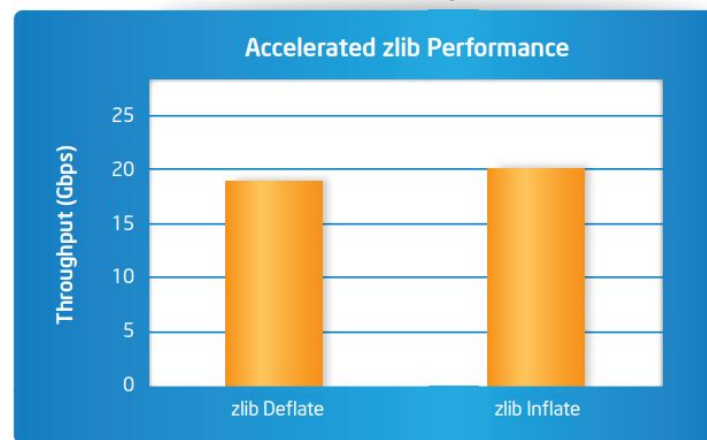


Figure 5. Accelerated zlib Performance for Compression and Decompression (Using a single Intel® Communications Chipset 8950)

- ProtoDUNE expects to receive **beam during Q4 2018**
- **One APA** will be read out using the **FELIX readout system**
- FELIX is based on the concept of having a **thin interface between the front-end and commodity hardware**
- Input rate is sustained using **firmware and software modified** from the original ATLAS version
- Data is sent to software BoardReaders, performing **trigger matching and lossless compression**
- The FELIX readout is in use for detector commissioning and is being finalized for **data taking with beam in September 2018**



