The H2020 FET-HPC projects ExaNeSt and EuroExa are part of a larger initiative aiming to demonstrate the feasibility of a European technology based ExaScale HPC system in the next 5–8 years. The consortia are a balanced mix of academic and research excellence and SMEs well established at European level. INFN is mainly involved in network design, system integration and platform benchmarking through real scalable applications.

**ExaNeSt (2015-2019)** project main goals:
- Evaluation of Exascale-enabling technologies.
- Architecture hardware/software co-design of a novel system-level interconnect, distributed NVM (Non-Volatile Memory) storage and advanced cooling infrastructure for an ARM-based ExaFlops-class supercomputer benchmarked through a rich set of real scalable applications.
- Integration of a small scale (200 computing nodes) demonstrator based on last generation high end SoC FPGAs.

**EuroExa (2017-2021)** leverages ExaNeSt results to deliver a world-class HPC pre-Exascale demonstrator:
- Consortium: 16 partners (SME 40%).
- Duration: 42 months.
- Budget 20 M€.

**Highlights of ExaNeSt hardware**

**QFDB Node**

- Xilinx Zynq Ultrascale+ MPSoC
- Mezzanine & Cooling Mechanics

**The Node: QFDB (Quad-FPGA Daughter-Board):**
- x4 Ultrascale+ FPGAs (16 cores)
- 64 GB DDR4 (16 GB/FPGA @160Gbps)
- 512 GBytes SSD/NVMe
- All-to-all intra-node topology.
- 10 HSS 10 Gbps links to external world.
- 120mm x 130mm

**Hierarchical Network: ExaNet**
- PHY based on High-throughput High Speed Serial Links (HSS) with custom flow control & protocol.
- Tier-0: Intra-QFDB: 2x2+2 HSS links per FPGA with “all-to-all” (one hop) topology.
- Tier-1: Inter-QFDB: 10 bidirectional HSS links, 20 Gbps peak aggregated bandwidth, multiple configurable topologies.
- Tier-3: Inter-Chassis: ToR (Top of Rack) custom switch based on a Virtex Ultrascale+ FPGA.
- Tier-4: Photonics for inter-racks communications.

**ExaNet Prototype first results:**
- 4 Trenz systems, 2x2 mesh topology.
- 2 running ports: 1 for data (pck/2er), 1 for ACKs (mbox).
- Running at 156MHz.
- 10Gbps links.

**System Architecture and Technology**

**Euroexa Computing Nodes:**
- TB1/TB2 Node: QFDB (v2).
- TB3 Node: custom designed multi-core ARM SoC tightly integrated with FPGAs (network & accelerators).

**Blade**
- 16 Node half depth 1u chassis.
- 2x 3.2Kw per U (back2back).
- Hybrid (Switched + Direct) network topology.
- 2.56 Tbps aggregate switching performance.
- Total Liquid Cooling technology.
- Hot water out, chiller-less operation.

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