Low power, large scale HPC platforms for scientific and engineering applications: status of ExaNeSt and EuroExa H2020 FETHPC projects.

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In the last few years the European Union has launched several initiatives aiming to support the development of an European-based HPC industrial/academic eco-system made of scientific and data analysis application experts, software developers and computer technology providers. In this framework the ExaNeSt and EuroExa projects respectively funded in H2020 research framework programs call FETHPC-2014 and FETHPC-2016 are inscribed.

ExaNeSt project is active from 2015 and its main goals are to evaluate enabling technologies and to design architecture of a novel system-level interconnect, distributed NVM (Non-Volatile Memory) storage and advanced cooling infrastructure for an ARM-based ExaFlops-class supercomputers. ExaNeSt is building a small scale (200 computing nodes) demonstrator based on last generation high end SoC FPGAs, interconnected by "ExaNet"- a novel, unified (for data and storage traffic), low latency, high throughput, RDMA-based interconnect architecture - and benchmarked through a rich set of real scalable applications.

EuroExa projects, started on September 2017, will leverage on ExaNeSt results to deliver a world-class HPC pre-Exascale platform prototype. EuroExa will build a brand new high end microprocessor embedding multiple ARM A73 cores directly interfaced to large FPGAs integrating computing accelerators and scalable network architecture.

INFN involvement is in the area of network development and benchmark through scientific application providing proprietary neural network simulation code (DPSNN) and Lattice Boltzmann Methods.

In this talk, after a brief introduction of the motivations, goals and plan of activities of ExaNeST and EuroExa projects, I will report on the status of system R&D in particular on network architecture design, implementation and evaluation through execution of application kernels.

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