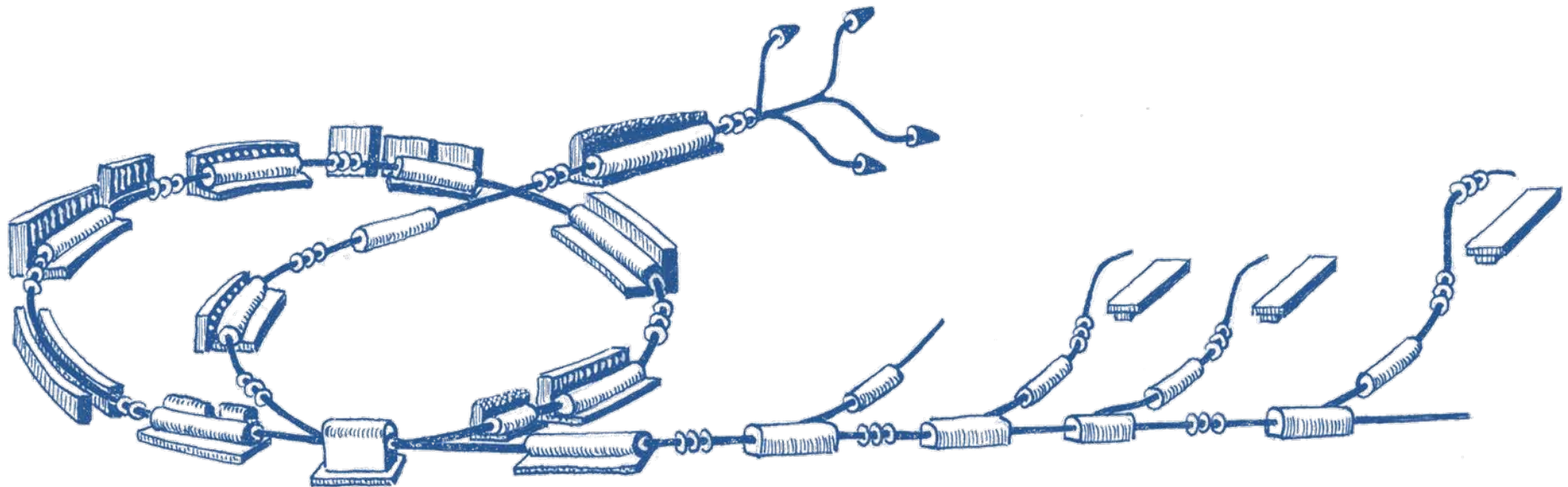
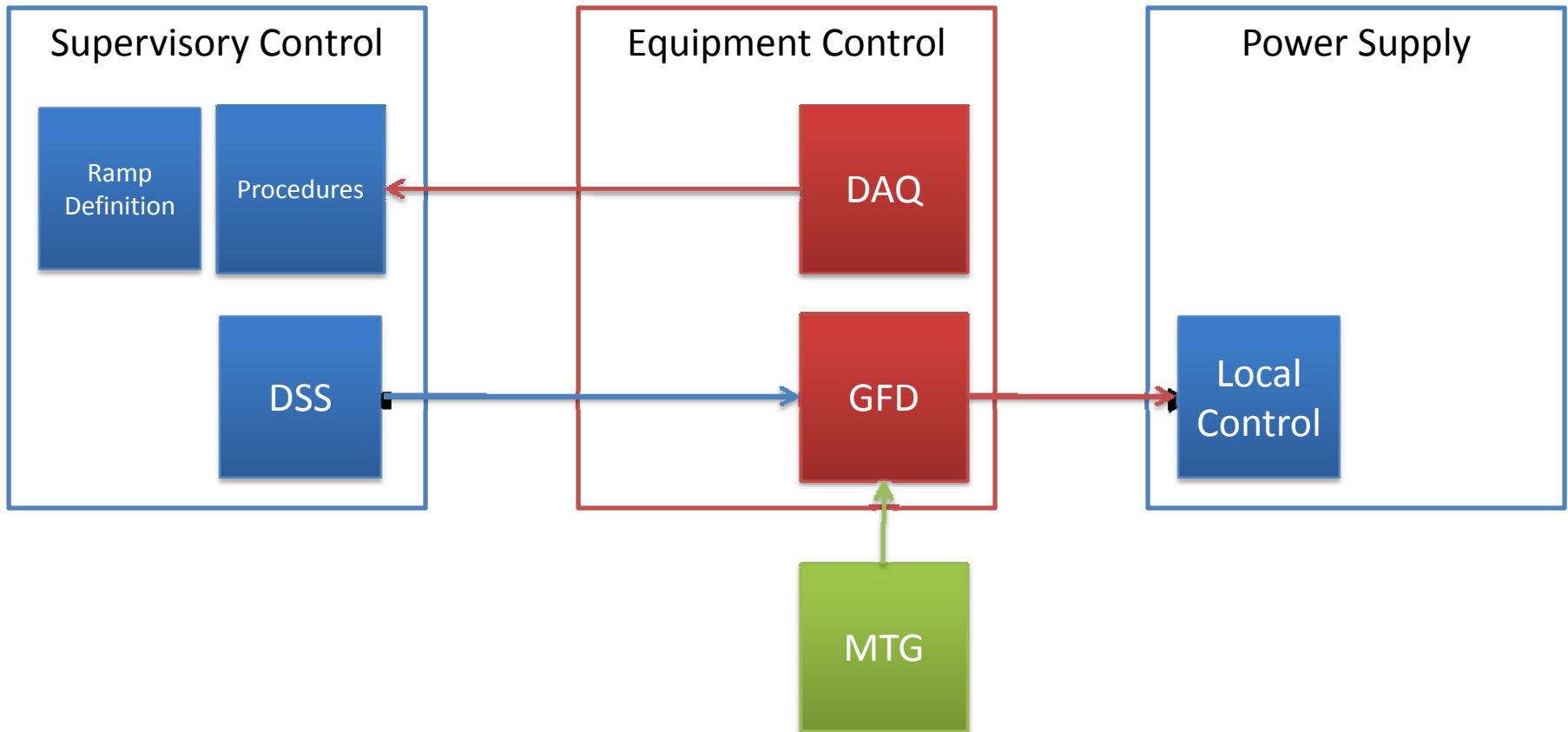


MedAustron Controls Workshop 1

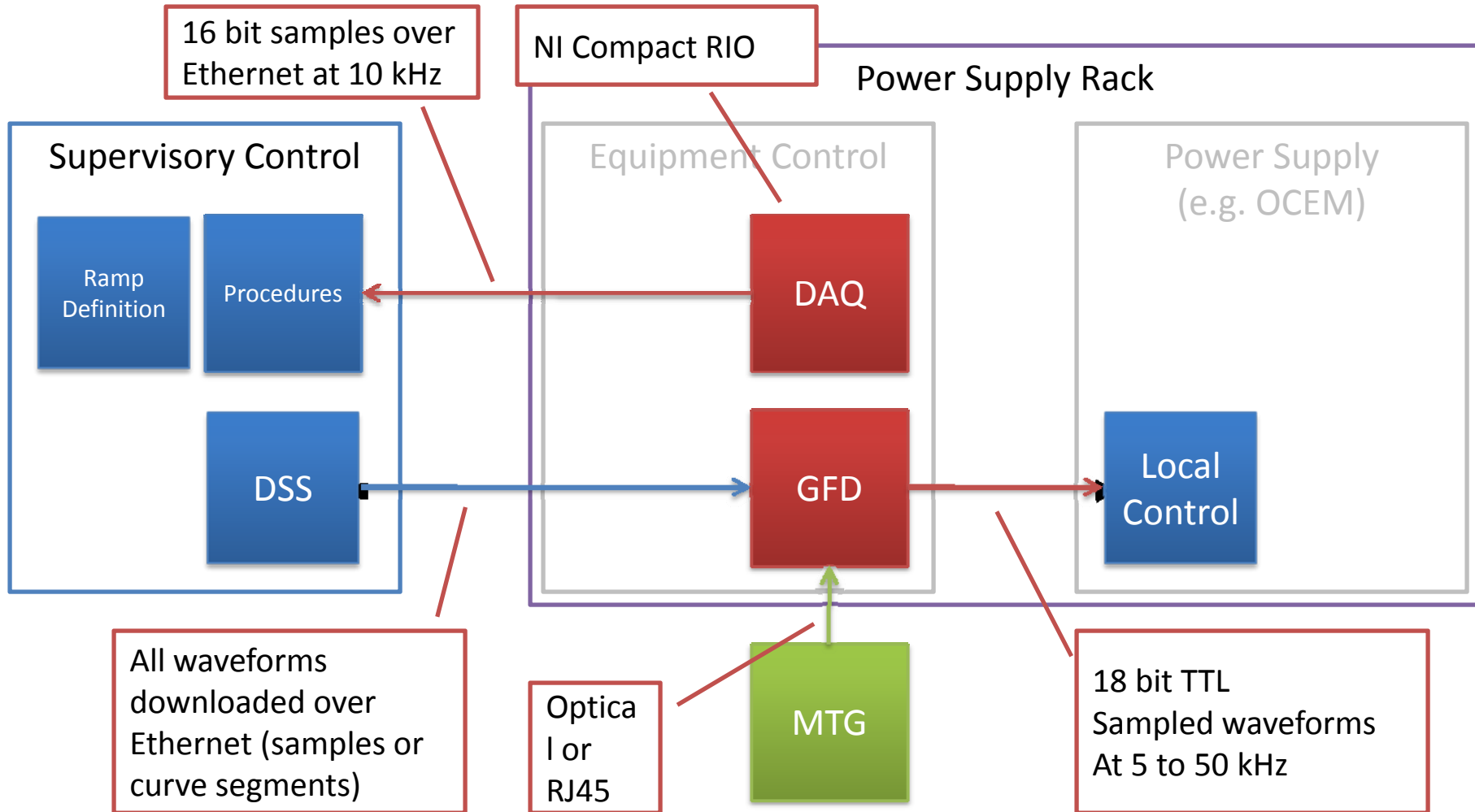
CNAO Power Supply Controls



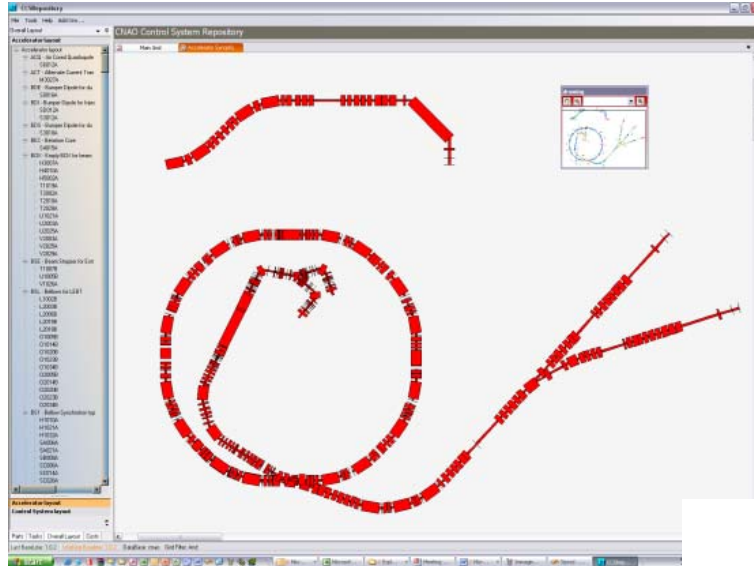
Logical Architecture



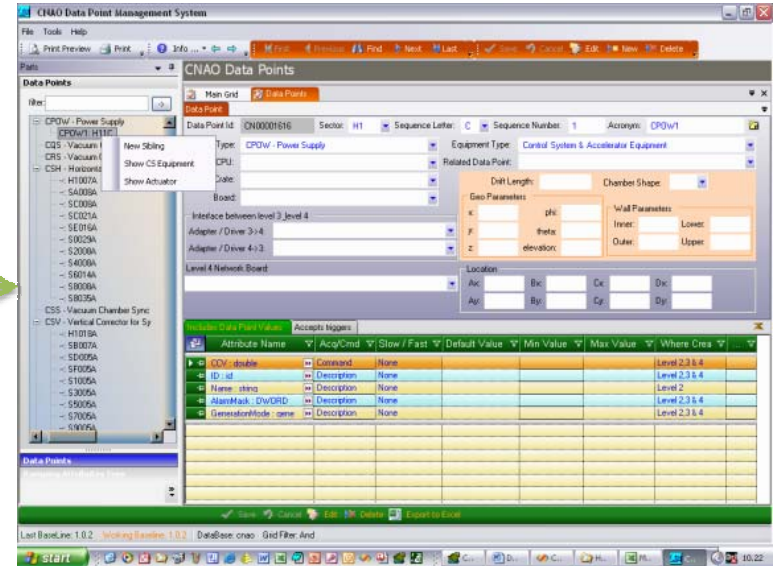
Physical Architecture



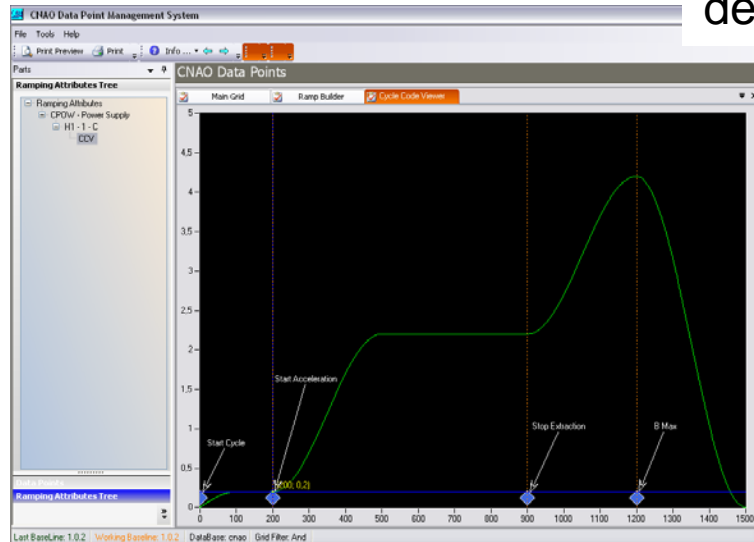
Support Software integrated with PVSS



Datapoint definition



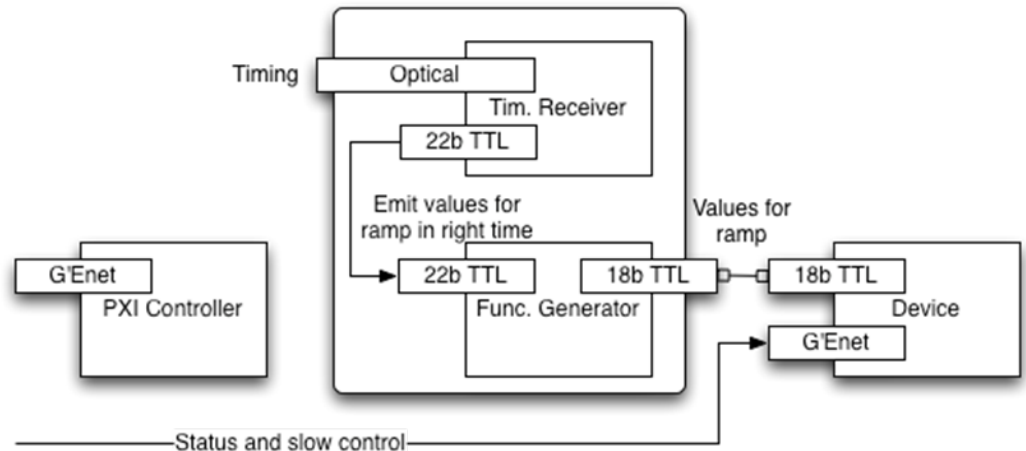
Ramp definition



Configuration provision



Digital Function Generator



- Compact PCI crate
- 1 CPU as controller
- 1 FPGA for “anything IO” with
 - 96 pin SCSI-5 plug for output
 - Protocol to power supply logic controller uses 18 bit
 - 96 pin SCSI-5 plug for input from timing receiver card
- 1 timing receiver card (by SIDEA)
 - 1 opto in, 1 22 bit TTL out to FPGA board

Physical Layout (Example)

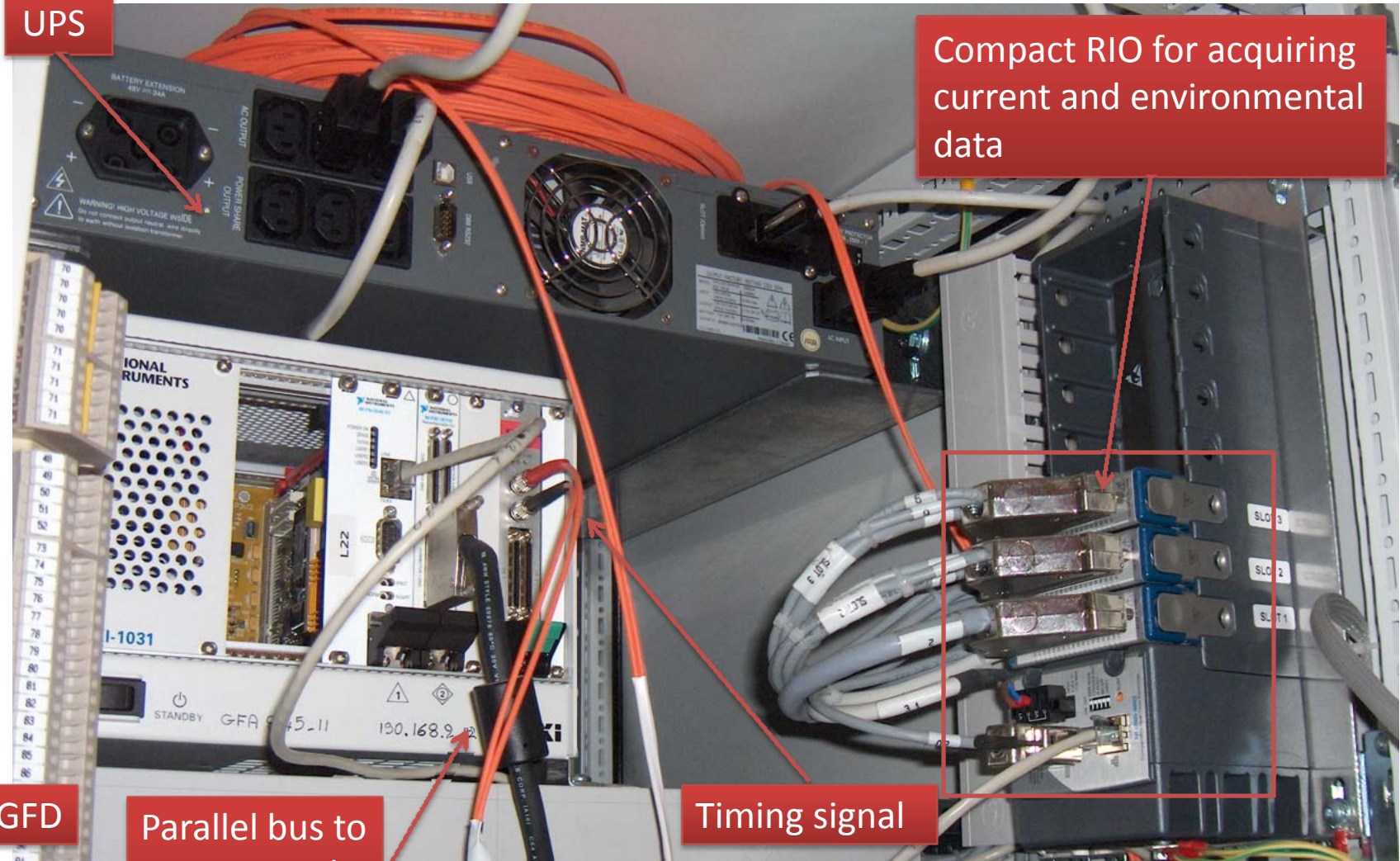
UPS

Compact RIO for acquiring current and environmental data

GFD

Parallel bus to
Power supply
Control logic

Timing signal



Advantages

- Entirely **Commercial Off the Shelf**
- **Separation of concerns**
 - Responsibility of power supply functioning belongs to power supply company
- **Generic** design
 - Wherever waveform production is needed
- All waveforms are resident in function generator
- Simple integration with timing and B-train system
- Uses standard Ethernet apart from timing signals
- Good resolution and timing performance
- Support software can be purchased from CNAO
 - Waveform generation, distribution, configuration
 - Integrated with PVSS

Disadvantages

- Price
 - cPCI crate, controller, FPGA boards, cRIO, UPS
 - About 10'000 CHF per unit for control and acquisition
 - 2.5 MIO CHF for control another 0.5 MIO for DAQ
- Space
 - Bulky, sometimes no space within power supply
 - Difficult to access in case of problems
 - Safety when opening power supply
 - Sometimes on top of power supply

Same Design – Different technology

- **PC104** with “anything IO” **FPGA based IO**
 - 600 CHF CPU, 300 CHF FPGA, 300 CHF timing receiver, rounded to 1'500 CHF for control
 - Complete solution should cost less than 3'000 CHF per unit.
 - Examples:
mesanet.com (4I65),
connectTech.com (FreeForm104 Spartan based)
Shop for more at
http://www.fpga-faq.com/FPGA_Boards.shtml
- **NI single board Rio** sbRIO-96xx O(1500 CHF)
- Keep simplicity of CNAO design
- Keep generic approach
- Lower price comparable to other solutions

NI sb-RIO96xx

