WP6

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for Ivan and Gianluigi

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WP Tasks

- **WP Coordinators: Gianluigi Casse, Ivan Peric**
- **Goal: Exploration of an innovative tracking-detector technology based on active CMOS sensors**
- Task 1: Scientific Coordination (KIT, UNILIV)
- **Task 2: Simulation (CNRS-CPPM, UBONN, STFC-RAL, UNIGLA)**
  - Perform TCAD process simulations and Geant4 simulations for test structures and sensor prototypes for different CMOS processes
  - Optimize sensor designs based on simulation results
  - Organise simulation workshops
- **Task 3: Sensor Development (CEA, CNRS-CPPM, KIT, UBONN, STFC-RAL, UNIGLA, UNILIV)**
  - Design test structures and sensors
  - Design pixel sensors matching different readout ASIC footprints
  - Prepare designs for MPWR submissions exploring different foundries
  - Characterise test-structures and sensors using electrical measurements, lasers, sources and test beams
  - Perform irradiation campaigns to validate the radiation hardness of each process technology and sensor design
- **Task 4: Hybridisation (INFN-GE, IFAE, UNILIV**)
  - Perform basic R&D on capacitive interconnection
  - Setup production facilities for full-prototype assemblies (chips on test boards)
  - Deliver full assemblies to all participating projects
  - Investigate options for future industrialisation of the interconnection process

WP Milestones

- MS7: Simulation workshop on HV/HR-CMOS TCAD and Geant4 simulations
  - ACHIEVED
- MS11: Multi Project Wafer Run (MPWR) submission
  - ACHIEVED
- MS26: First test beam campaign with initial sensor prototype assemblies
  - ACHIEVED
- MS27: First irradiation campaign with sensor prototype assemblies
  - ACHIEVED
- D6.5: Optimised interconnection process -> MS42
  - DELAYED -> MS42
- MS28: First functional HV/HR-CMOS assembly with capacitive interconnection
  - ACHIEVED

Task 3: Overview

CCPD developments:

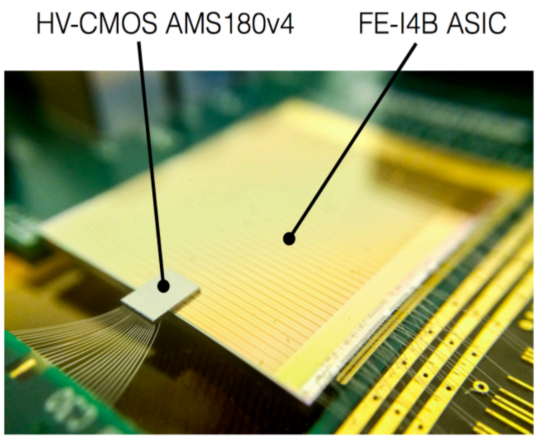
- LF_CPPD/LF_CPIX
- H18CCPD
- H35DEMO (CCPD)

CCPD 2nd generation - Monolithic sensors

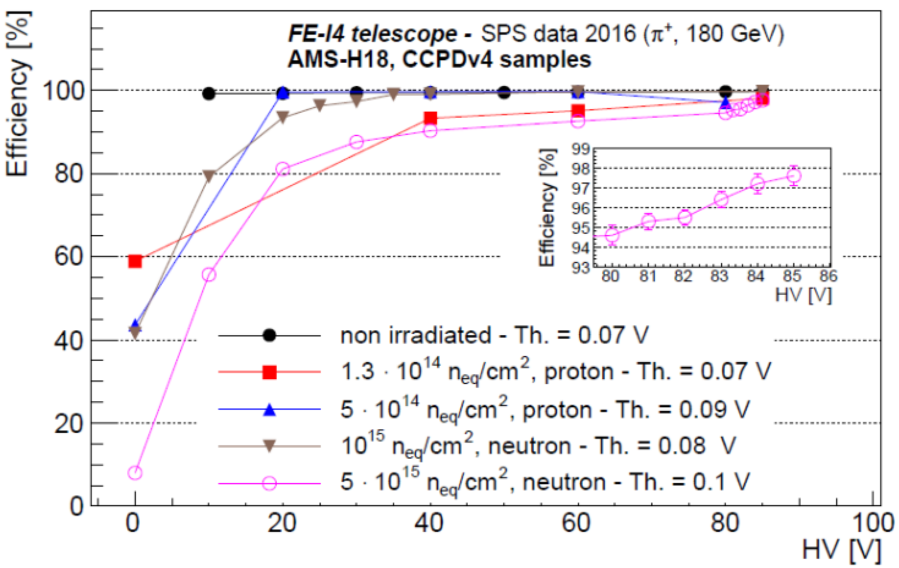
- H35DEMO (Standalone)
- LF_MONOPIX
- LF_ATLASPIX
- ATLASPIX/MUPIX8

Sensor	Technology	Size (mm^2)	Pixel Matrix	Pixel Size (μm^2)
LF_CPPD	LFA15 (150nm)	5 x 5	140 x 32 pixels	33 x 125
LF_CPIX	LFA15 (150nm)	10 x 9.5	34 x 168 pixels	50 x 250
LF_MONOPIX	LFA15 (150nm)	10 x 9.5	142 x 36 pixel	50 x 250
H18CCPD	AMS H18 (180 nm)	2.2 x 4.4	Different versions	25 x 25, 33 x 125, 25 x 125, 25 x 350
H35DEMO	AMS H35 (350 nm)	18.49 x 24.4	4 matrices: 16x300 (x2), 23x300 (x2)	50 x 250
LF_ATLASPIX	LFA15 (150nm)	10 x 10	5 matrices	40 x 100 , 40 x 60, 40 x 250
MuPix8/ATLASPix	AMS H18 (180 nm)	22.6 x 21.3	2 matrices	25 x 25 , 25 x 50 , 33 x 125, 50 x 60, 40 x 125, 80 x 81

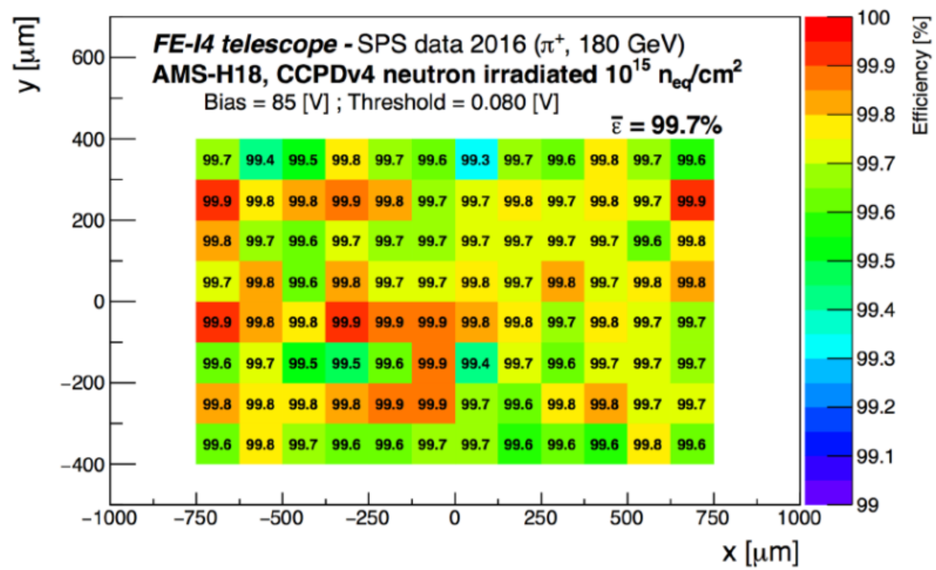
H18 CCPD - Results



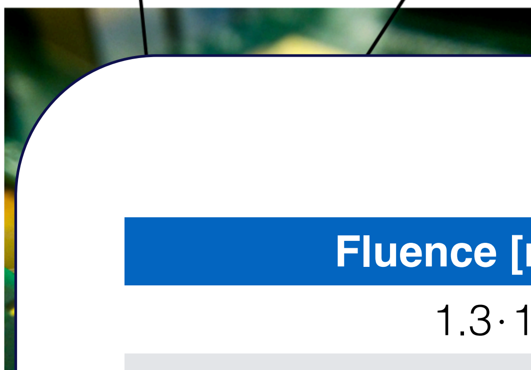
- **HVCMOS CCPD** sensors implemented in AMS H18 technology on standard 10 Ω cm substrate (CCPDv4)
- Irradiated to fluences between 1.3 x 10^{14} and 5·x 10^{15} n_{eq}/cm^2 and tested in beam (full matrix test). The average hit efficiencies of from 97.6 % (highest fluence) to 99.7% have been measured in the test beam at SPS with full matrices.
- These values are comparable to hit efficiencies of planar pixel sensors.



CCPDv4: *Measured detection efficiencies in the beam test versus applied bias voltage.*



"Testbeam results of irradiated AMS H18 HV-CMOS pixel sensor prototypes"
arXiv:1611.02669 [physics.ins-det]



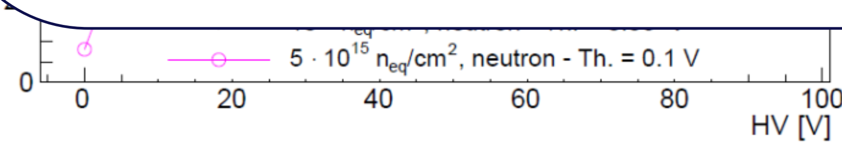
- **HVCMOS CCPD** sensors implemented in AMS H18 technology on standard 10 Ω cm substrate (CCPDv4)

H18 Performance

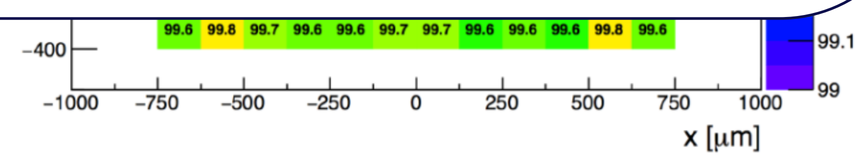
Fluence [n_{eq}/cm^2]	Average Hit Efficiency
$1.3\cdot10^{14}$	98.1%
$5\cdot10^{14}$	99.7%
$1\cdot10^{15}$	99.7%
$5\cdot10^{15}$	97.6%

- Results for all fluences better than 97%
- Fluence relevant for outer-pixel layers exhibited 99.7% hit efficiency

T. Weston et al.,
"An overview of recent HV-CMOS results"
12th Trento Workshop on advanced Silicon Radiation Detectors



CCPDv4: *Measured detection efficiencies in the beam test versus applied bias voltage.*

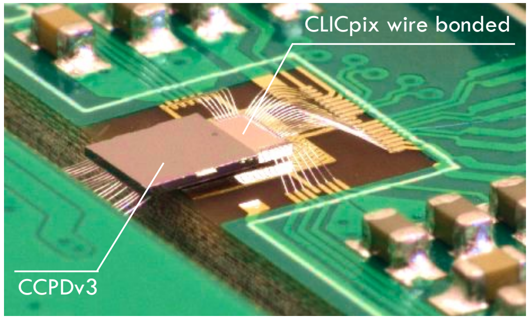


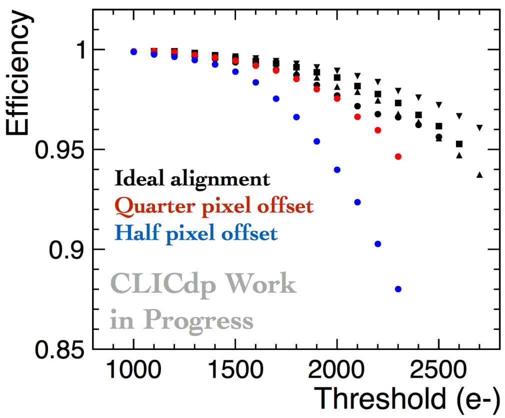
M. Benoit et al.,
"Testbeam results of irradiated AMS H18 HV-CMOS pixel sensor prototypes"
arXiv:1611.02669 [physics.ins-det]

H18 CCPD - Results

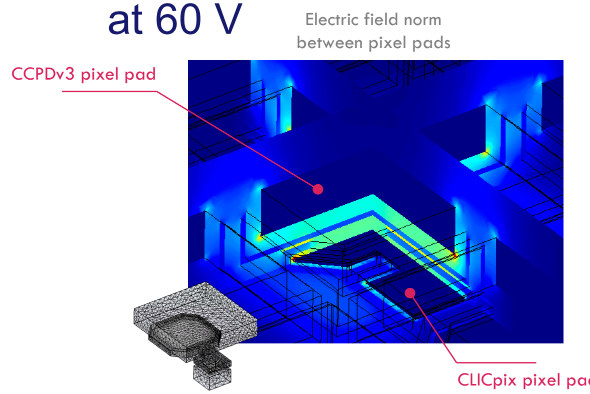
HV-

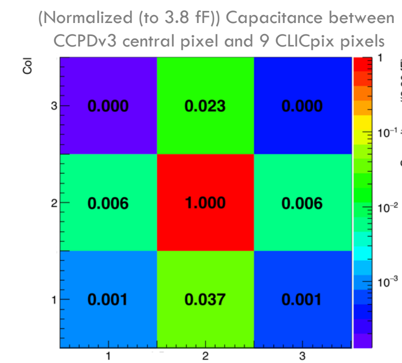
CCPDv3 for CLIC





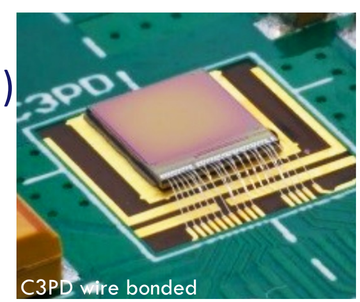
- **CCPDv3 sensors have been glued to CLICpix ASICs**
- Pixel size of 25x25 um^2
- Results shows good control on the gluing process
  - Coupling studies with FEM Simulations
    - Capacitance to closest pixel: 3.8 fF
- Good efficiency at target threshold (even for misaligned samples)
  - Threshold of 1200 electrons the efficiency of the assembly is higher than 98 %, increasing to 99.9 % at 60 V

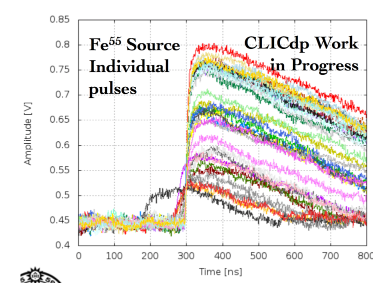




C3PD Sensor for CLIC

- Bigger pixel matrix (128x128 pixels with 25 µm pitch)
- Different pixel electronics
- Guard ring around HV-CMOS pixels pads
- Measurements done in stand-alone mode

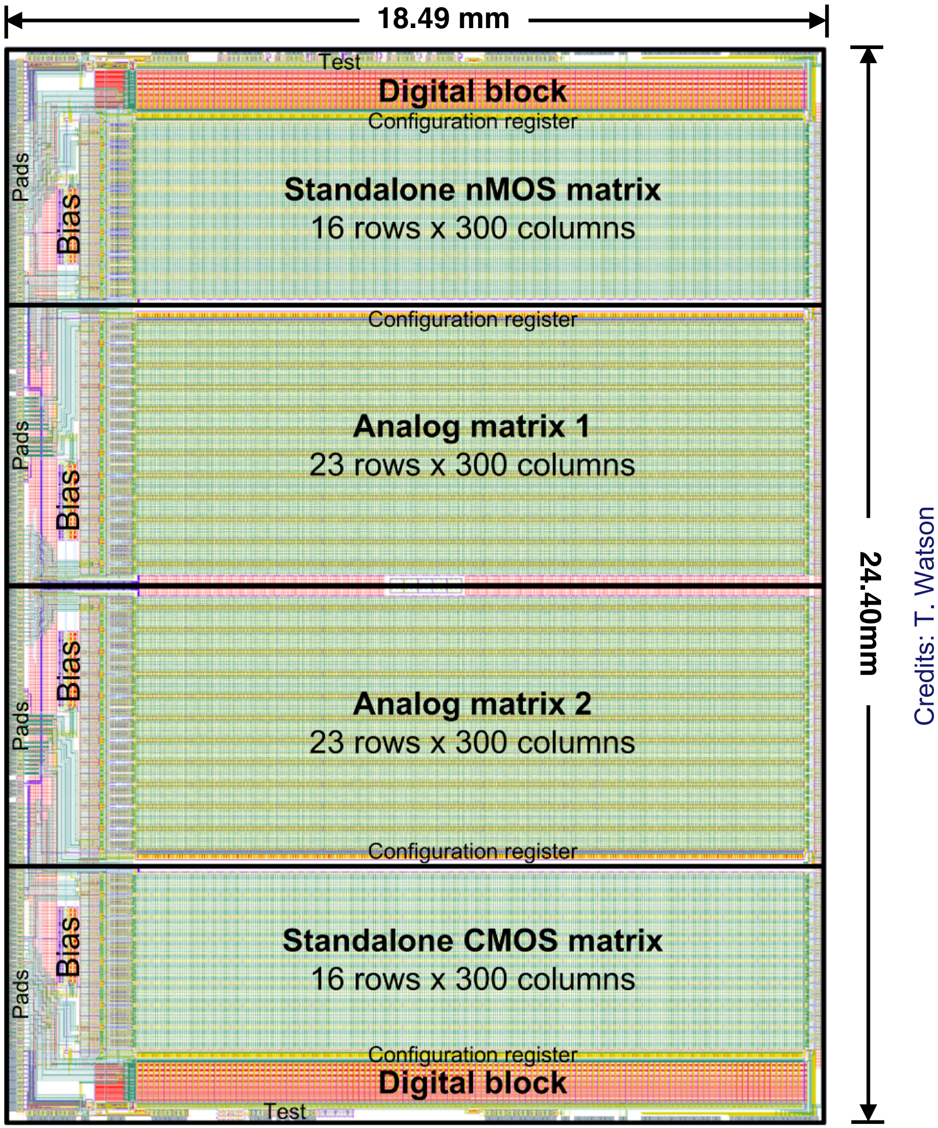




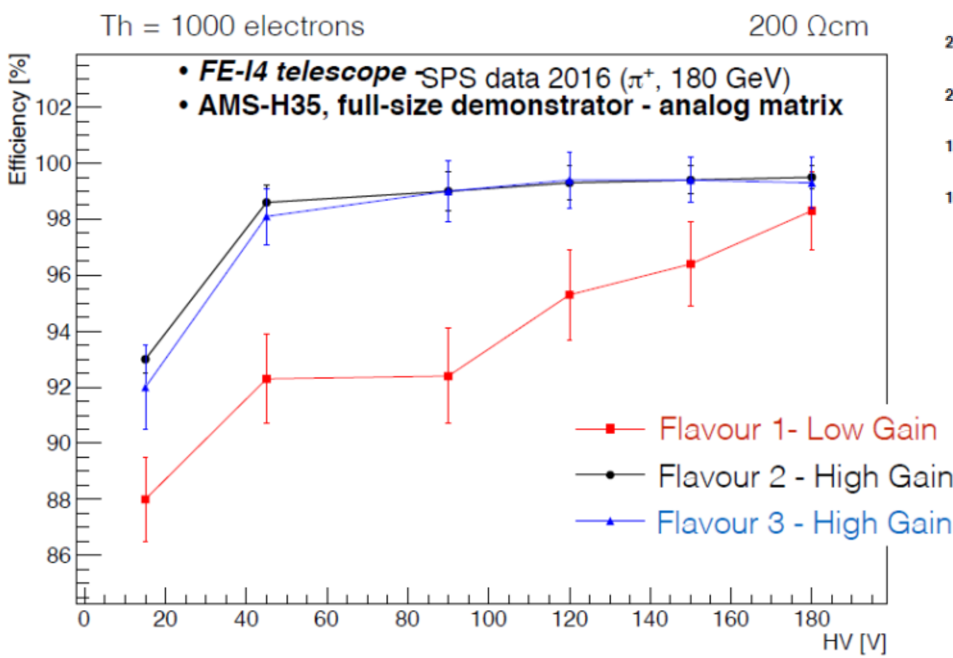
H35 DEMO

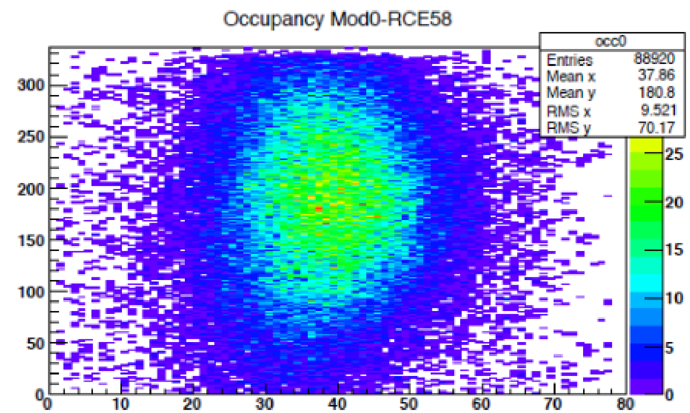
- **2 matrices of pixels with R/O coupled to FEI4. Pixels without comparators.**
- 2 monolithic matrices of pixels with standalone R/O. Pixels with nMOS/CMOS comparators. Digital blocks (FE-I3 style) are in the periphery of the matrices.
- Different pixel flavours
- Test structures for TCT/e-TCT and sensor capacitance measurement
- Pixel size: 50 µm x 250 µm for 1-to-1 connection to FEI4
- Timing resolution: 25 ns –
- Readout speed: 320 MHz
- Rad-hard design - Resistivity: 20 Ω·cm, 80 Ω·cm, 200 Ω·cm, 1k Ω·cm - Detection efficiency > 99% in test beams

CCPD (1-8)



- Test beam measurement at SPS (September-November 2016)
- > 99% detection efficiency has been measured with matrices
- > 99% of hits have timewalk less than 50ns





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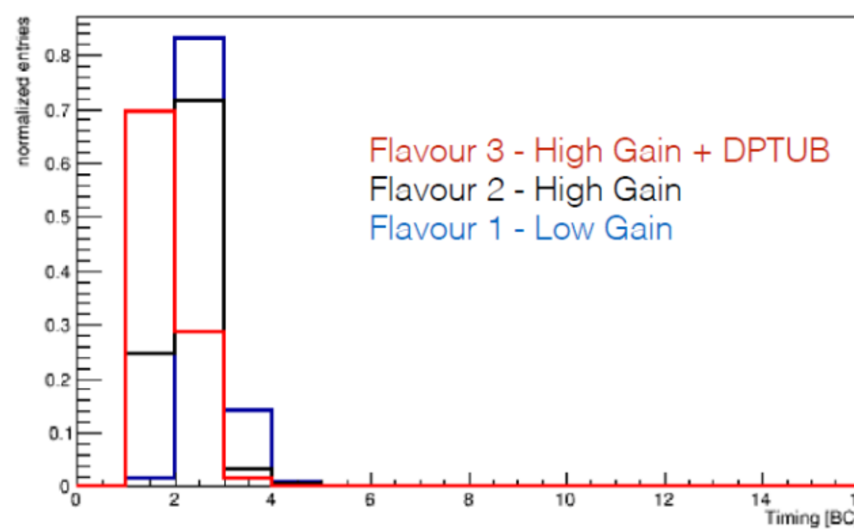


- 200 Ω · cm, non-irradiated
  HV scan for 3 pixel flavours of Analog matrix
- Already from 90V bias, **efficiency of 99%**

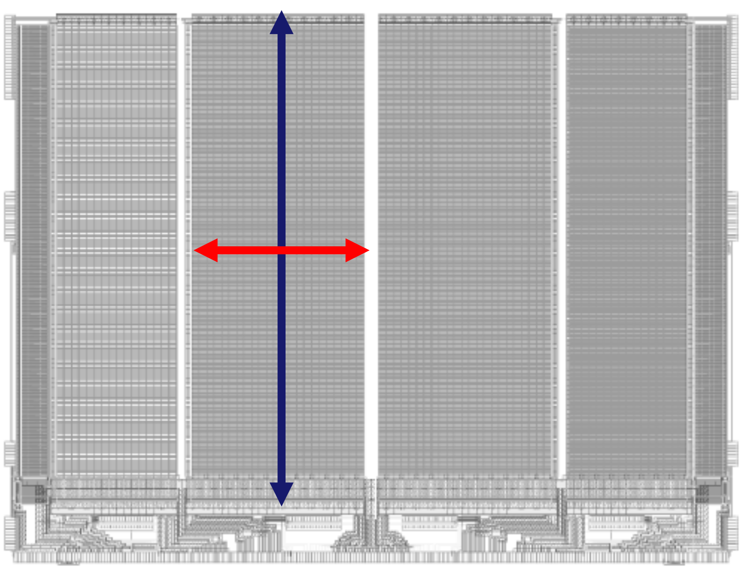
- **99% of charge collected within 2 BC**
- Observe differences in characteristics of each of the pixel flavours

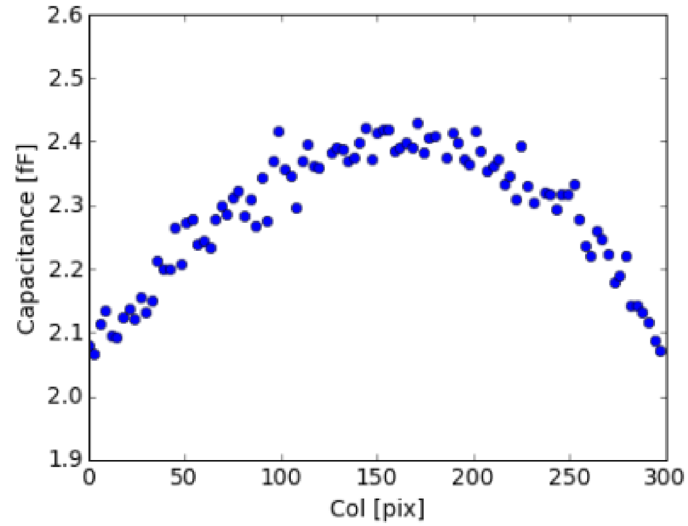
The H35DEMO has the possibility that external signals are applied to the pixel pads used for the capacitive signal transmission. In this way, the coupling capacitance can be measured for every pixel.

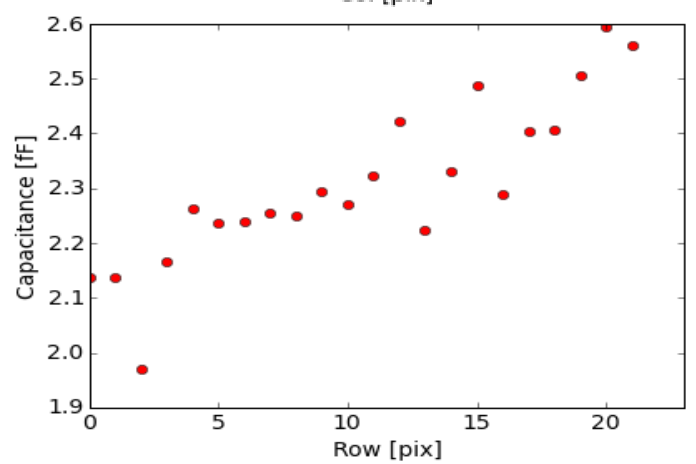
The coupling capacitive on a large area is quite uniform. The coupling capacitance varies from 2.05 fF to 2.4 fF, which is a suitable value for signal transmission.

Measurement: Toko Hirono, University of Bonn

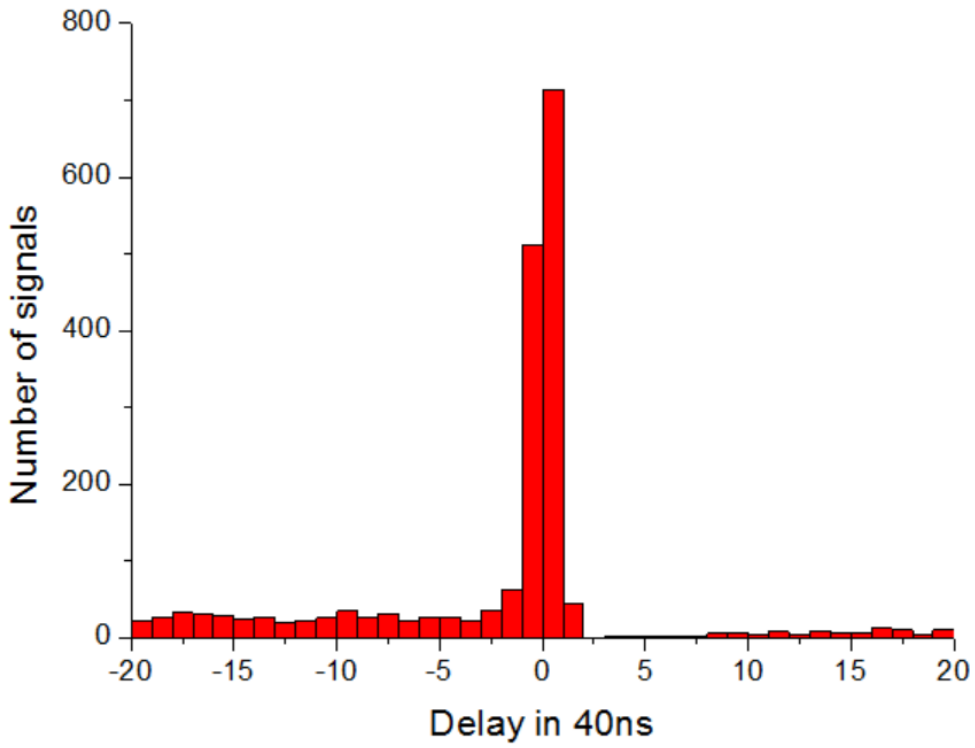
Coupling capacitance between HVCMOS pixel pads and FEI4 amplifier pads have been measured (Bonn) along a pixel row of 1.5 cm length.



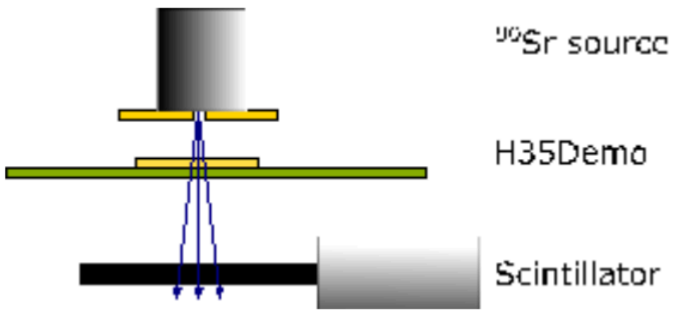


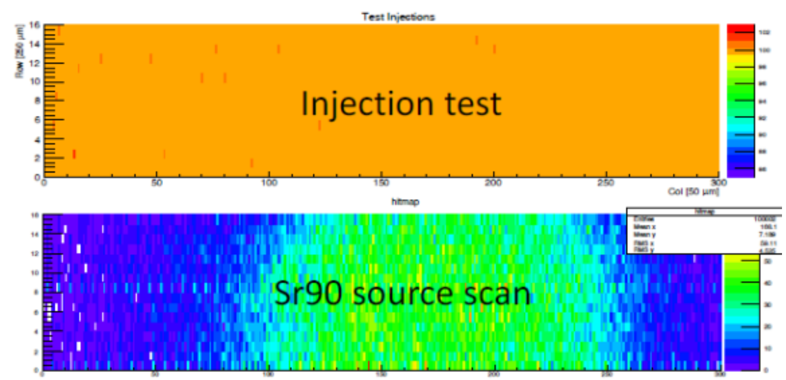


- The H35DEMO has the possibility can be readout as a monolithic sensor
- Zero suppression and time measurement on chip
- TWCC



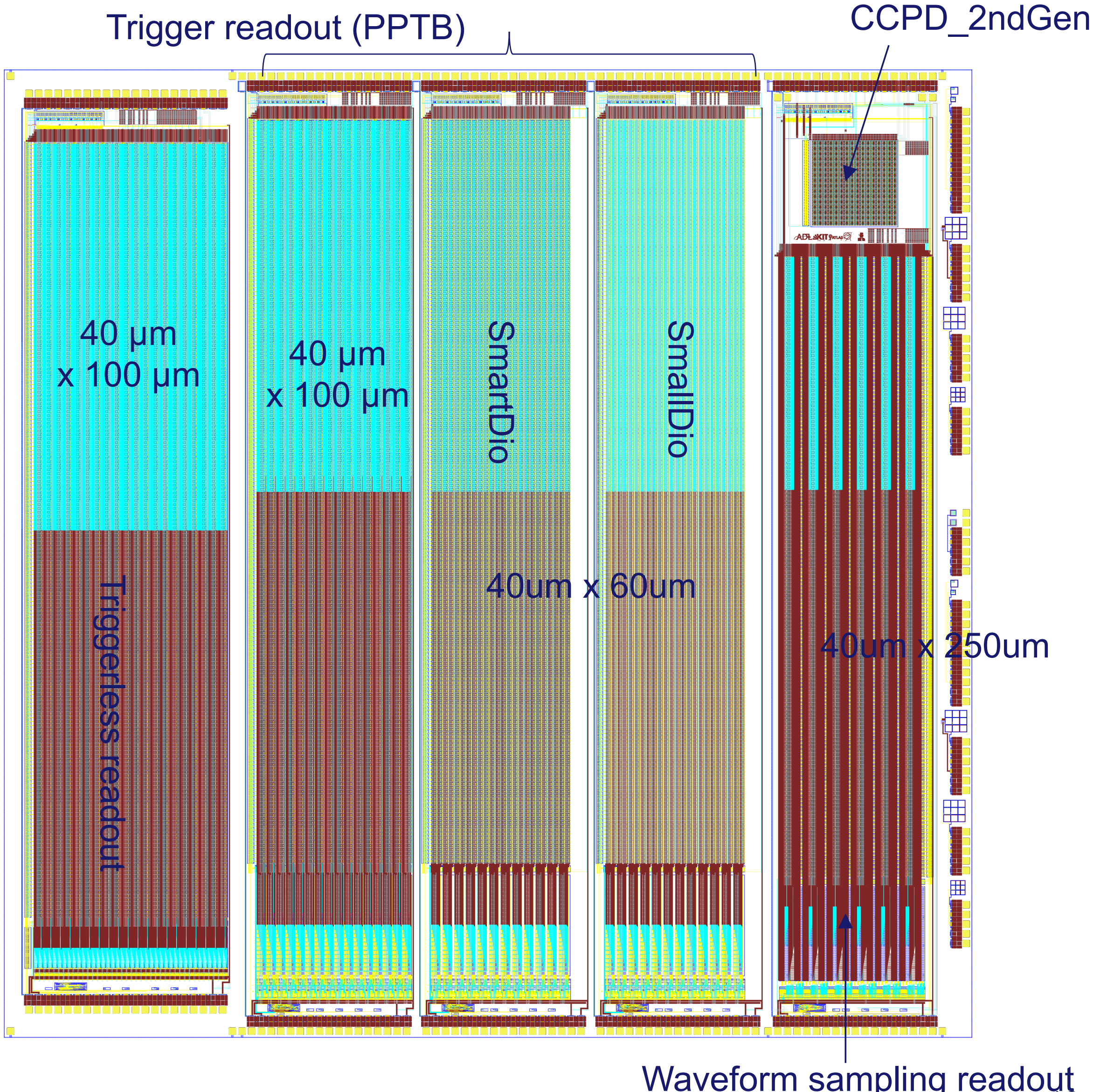
Time resolution – difference between the time stamp and the trigger moment





LF_ATLASPIX

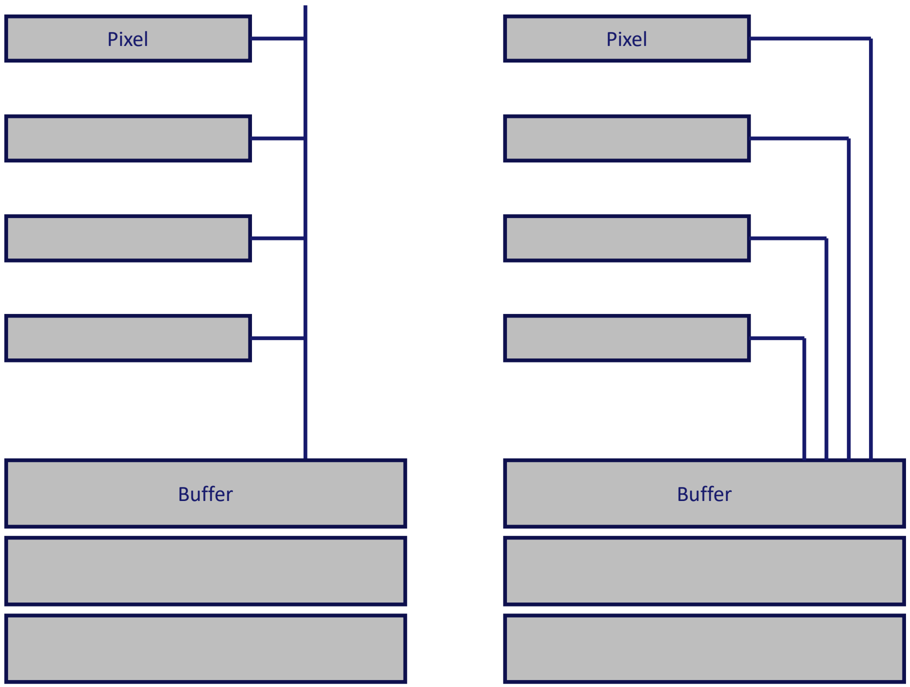
- Technology LFA15 (150nm)
- Design by IFAE, KIT, Uni. Geneva and Uni. Liverpool
- Different pixel sizes
- Different matrices (1 CCPD and 5 monolithic) and test structures
- Resistivities: 100 Ω·cm, 500-1k Ω·cm, 1.9k Ω·cm and 3.8k Ω·cm
- 4-well HVCMOS process



2ndGen

Readout types:

1. Trigger-less (column drain)
2. Triggered with parallel pixel to buffer connection (PPTB)



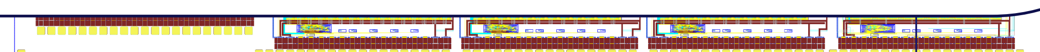
Trigger-less (column drain) **PPTB**

Trigger-less

Hit information (address, time stamp) is generated in the digital part of the pixel. Digital parts in one column share a data bus. In the case of multiple hits, the data are readout in serial way. The digital part of the pixel physically separated from the pixel sensor itself

PPTB

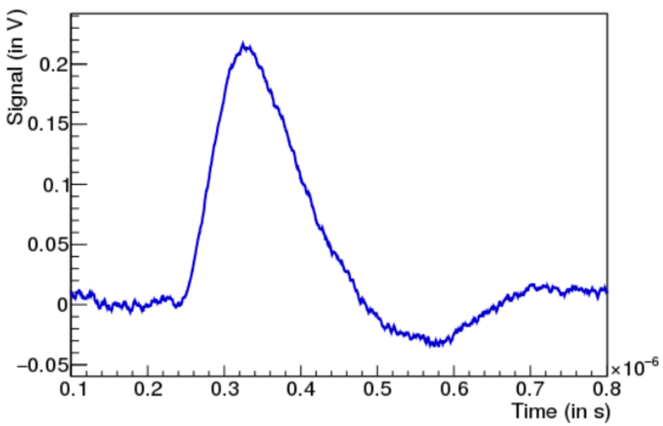
The hit information is transferred from pixels to the trigger-buffers with a parallel bus. The pixels contain amplifier and comparator. A trigger buffer receives the comparator outputs, generates hit information (address and time stamp) and keeps the information for the duration of the trigger delay.

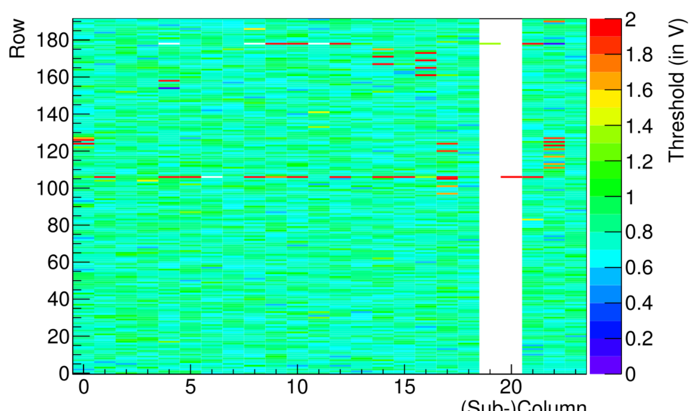


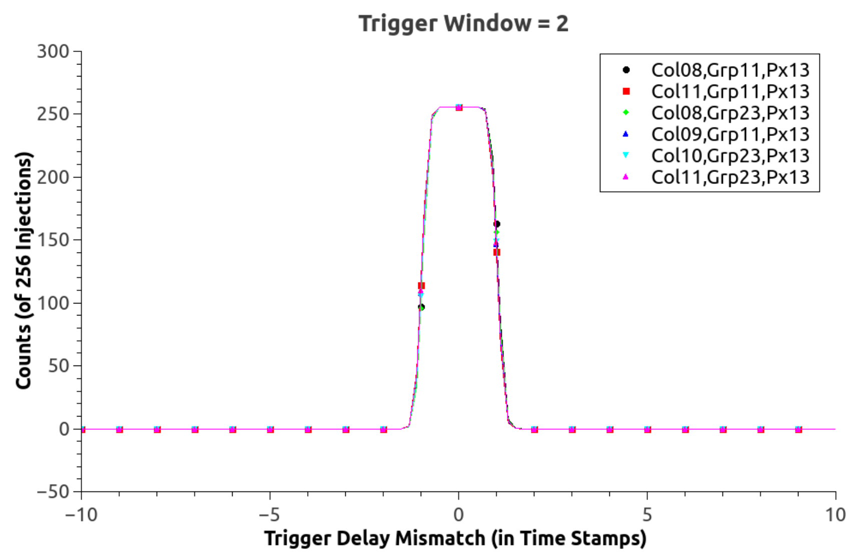
Waveform sampling readout

LF_ATLASPIX - Results

- Parallel-Pixel-to-Buffer Readout Principle is working. Triggered Readout is working with an accuracy of the order of 20 ns
- Response to test injection amplitude of 0.5V, that yields to a charge signal of about 1800 e
- Test of the trigger readout
- Threshold scan of full matrix







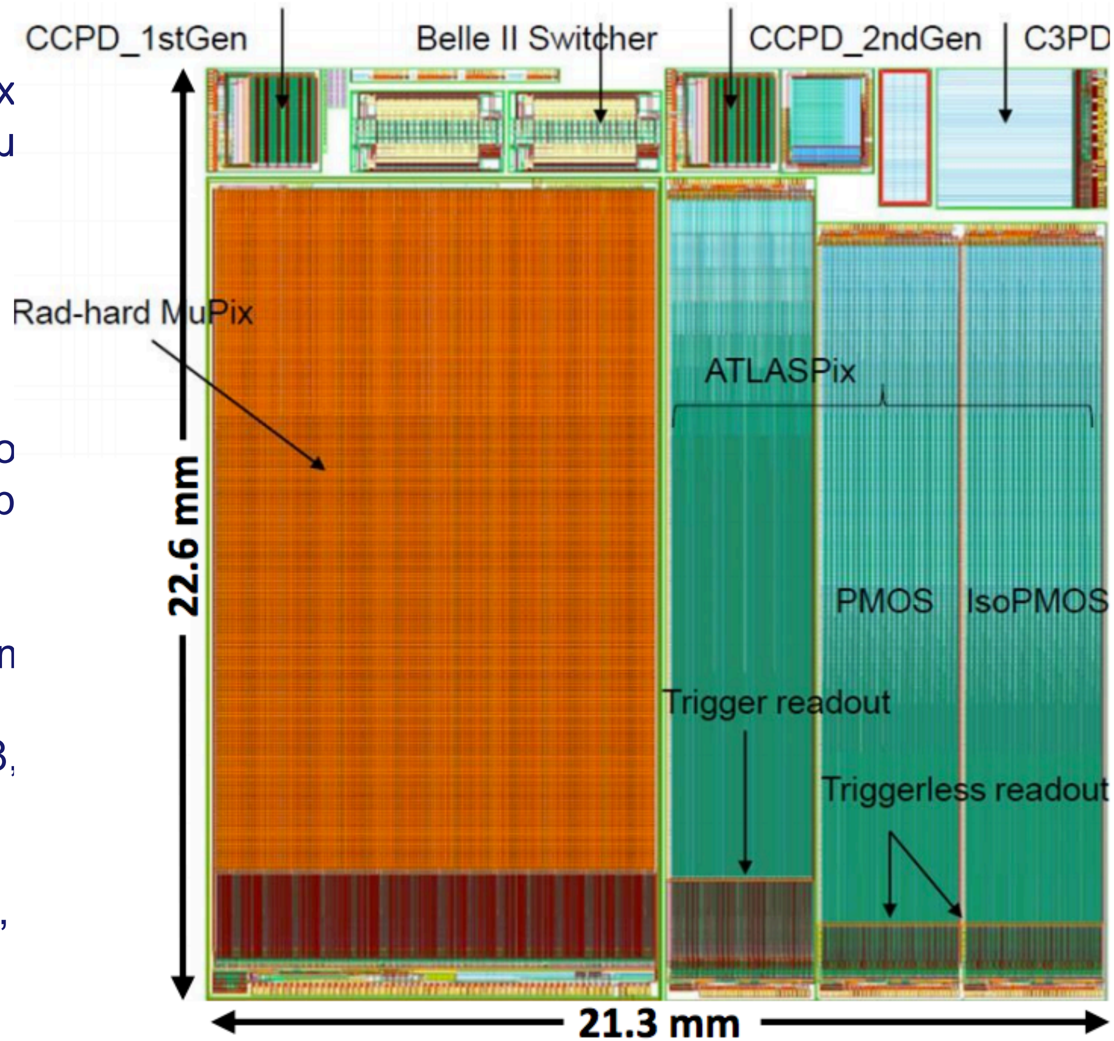
Detection Efficiency

Matrices of pixels for ATLAS

- Pixel size: 25 μm x 25 μm, 25 μm x μm, 33 μm x 125 μm, 50 μm x 60 μ 40 μm x 125 μm

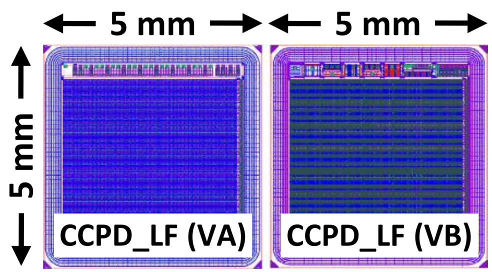
MuPix8

- Pixel size: 80 μm x 81 μm
  - Matrix with 200 x 128 pixels
- Pixels with CSA and output driver o
- Hit info: x-address, y-address, 10-b 6-bit amplitude
- Time resolution: 6.25 ns
- Nominal power consumption: 300 n per matrix
- Hit driven, triggerless R/O (MuPix8, Simple ATLASPix)
- Triggered R/O (M ATLASPix) - Resistivity: 20 Ω·cm, 50-100 Ω·cm, 400 Ω·cm, 600-1.1k Ω·cm



I. Peric, 12th Trento Workshop, 2017

Submitted, expected for April 2017



LF_CPPD Design by Bonn, CPPM, KIT

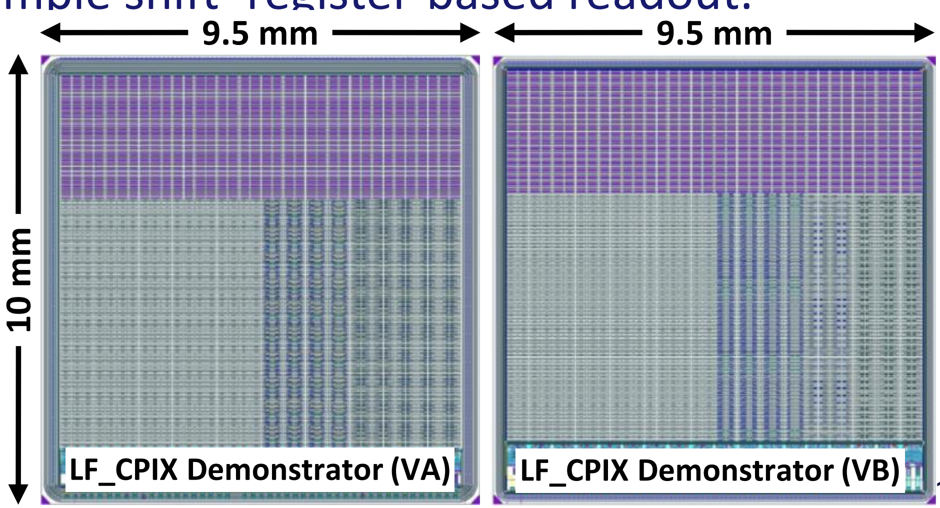
- 33 µm x 125 μm^2 pixels
- R/O coupled to FE-I4
- Sub-pixel encoding, res: 2k Ω·cm
- Standalone R/O for test

LF_CPIX submission contains two chips each with an area of 1 cm × 1 cm.

Design by Bonn, CPPM, CEA-IRFU

The chips contain three pixel matrices.

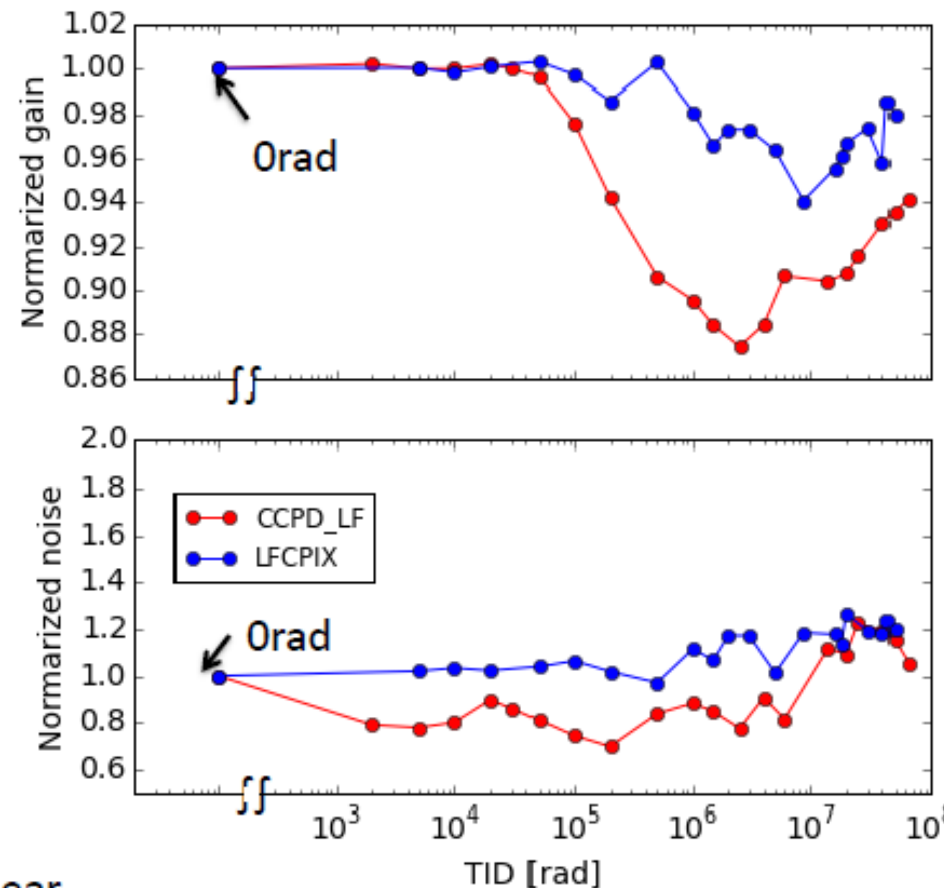
- **Matrix 1** : passive ("non CMOS") pixels.
- **Matrix 2 :** analog-digital pixels. These pixels use a charge sensitive amplifier with attached CMOS comparator and a simple shift- register-based readout.
- **Matrix 3:** analog pixels. These pixels employ only amplifiers. It is possible to access the amplifier- and comparator-outputs in all CMOS pixels.
- The pixel size is 250 µm × 50 μm^2.
- 2 kΩcm p-type substrate.



LF-CCPD fully characterized under X-ray, neutron and proton irradiations. At TID=50 MRad the increase of leakage current, gain decrease, noise increase and threshold tunability are acceptable

LF-CPIX design and optimization with TCAD tools, better breakdown voltage, after TID=50 MRad better gain degradation (~10%), good threshold tunability

Gain and noise under radiation level



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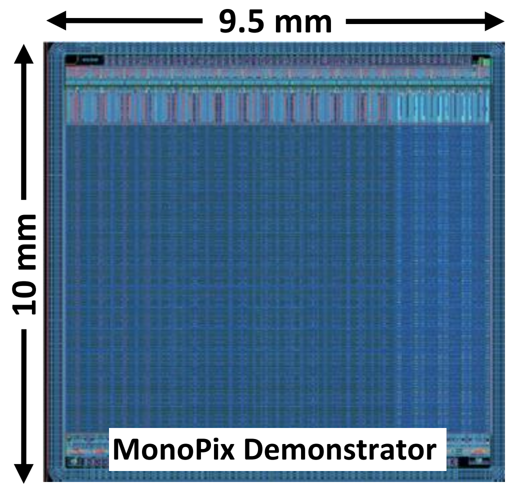
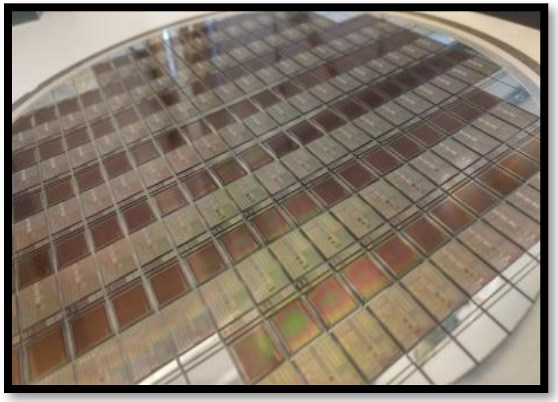
Gain degradation is reduced in LF-CPIX (2nd chip).
Decrease of the gain is less than 10% and noise increase is about 30%

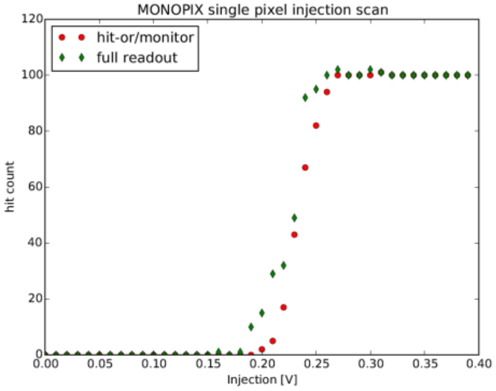
LF_MONOPIX sensor is a variant with monolithic readout.

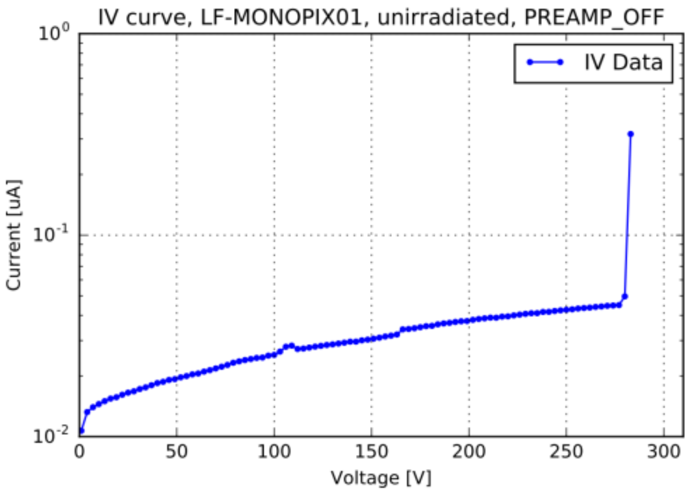
- **Design by Bonn, CPPM, CEA-IRFU**
- The chip area is 1 × 1 cm^2
- The pixel size 250 µm × 50 μm^2.
- 8 bit LE/TE/ToT
- Each pixel contains a digital block that is similar to the block used for the “standalone” pixels of H35DEMO or in the ATLAS pixel readout ASIC FEI3.





- LF_Monopix wafer received February
  - Diced in March, wire bonded and tested in Bonn
- **First tests promising**

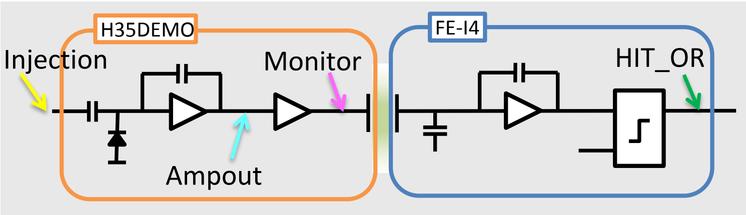




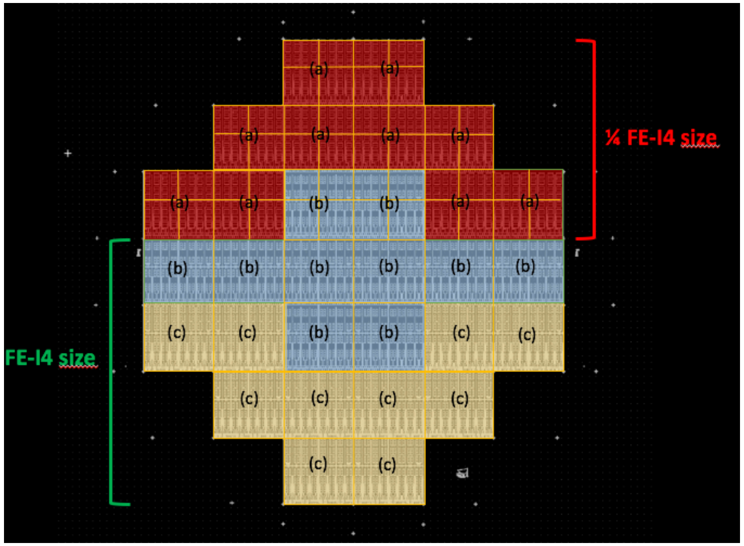
LF-Monopix delivered and fully functional, to be characterized and irradiated

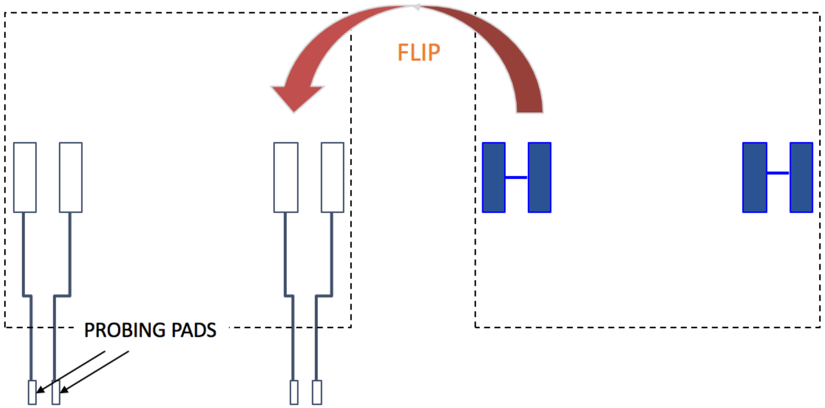
Different ways to study the optimization of coupling capacitance of CMOS:

- **"Indirect Method":** Capacitance of glue layer can be calculated from the injection capacitances of FE-I4
  - Very useful to characterize CCPD devices, but real coupling capacitance can be only extrapolated and can be influenced by cross/parassitic capacitance effects



- **"Direct Method":** The idea is to use a matrix of capacitors to test the uniformity of the glue thickness -> Bonding parameters can be optimized to study the wanted coupling distance and uniformity.



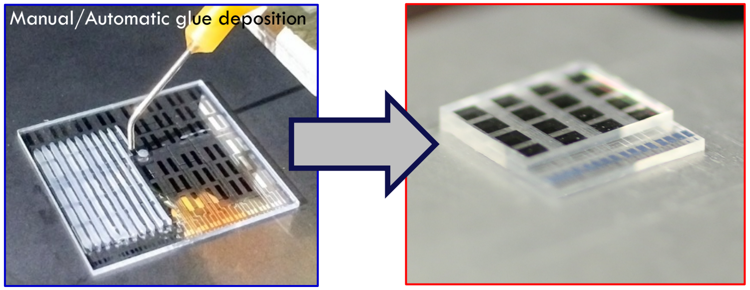


Different ways to study the optimization of coupling capacitance of CMOS:

Batch of 4 dummy 6-inch in fused quartz

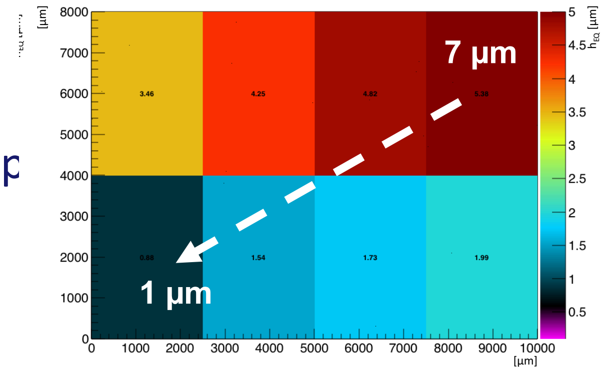
Up to now we processed the first 2 wafers:

- ***Wafer w/o pillars:*** Allowed to perform assemblies tiles on 1x1 cm^2 (1.5×1.5 mm^2 per plate) in Genova and 2x2 cm^2 in Geneva
- ***Wafer with 5 µm pillars:*** Allowed to perform the first assemblies (1.5×1.5 mm^2 per plate).

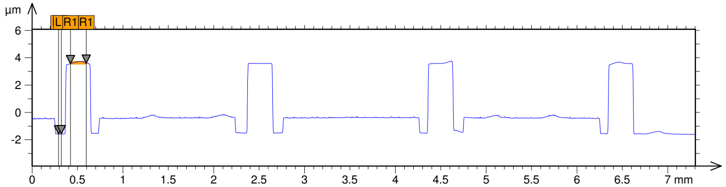


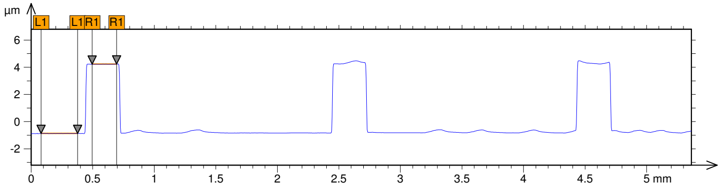
Assemblies done in Genova and Geneve shows a lower uniformity of the glue thickness

- Good repeatability and independence from used flip-chip machine
- Bowing not centred on sample



Tiles with pillars show a better uniformity than the sample with glue, but further studies are necessary to deposit the glue in a control manner to not bias the measurements.





Summary

Task 3:

- Large scale (2 x 2 cm^2) HVCMOS sensors in AMS 350nm technology produced and tested
  - The sensor is implemented of 4 different substrate materials, it contains various tests structures and can be attached (capacitively or with bumps) and readout by FEI4. Monolithic readout is also possible. The sensor can be used for development of interconnection technology. Test beams and irradiations are planned
- Various designs in LFoundry 150 nm process have been submitted – can be readout by FEI4 or as monolithic sensors
- Monolithic and CCPD designs have been submitted and some preliminary tested

Task 4:

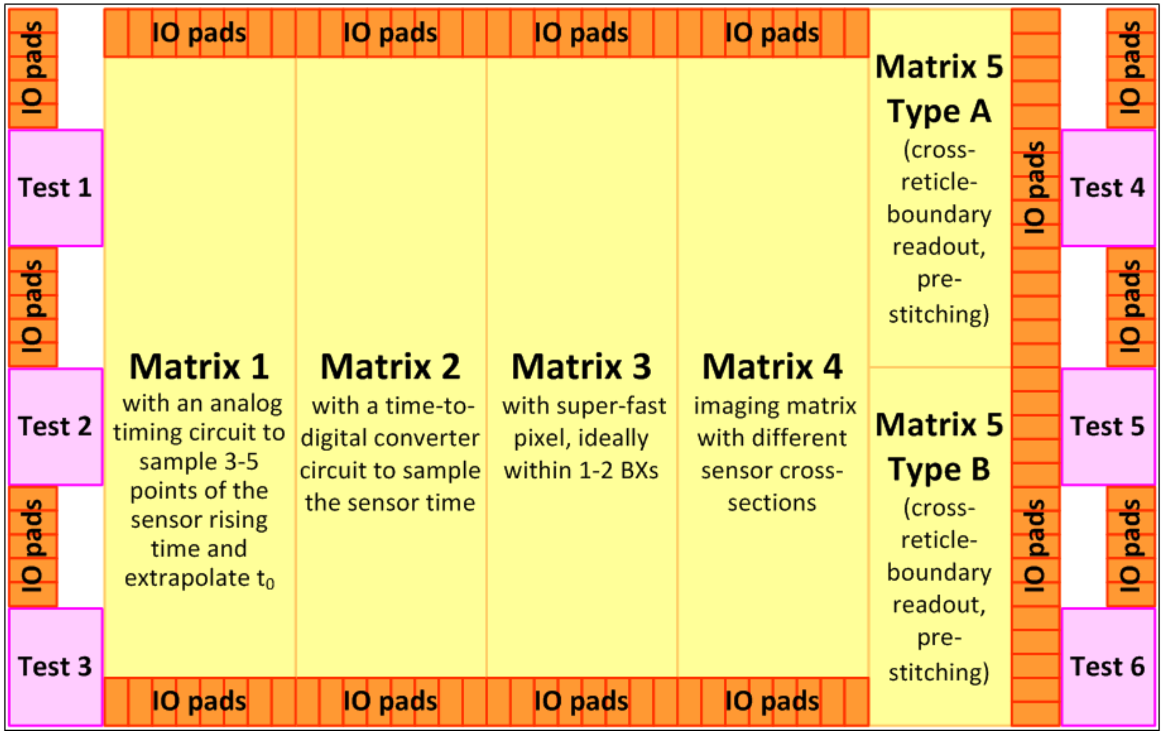
- Capacitive coupling works well on small chips – investigation of the interconnect technology of large chips ongoing

- Several samples H35CCPD and FEI4 are available

WP Deliverables

- **D1: TCAD libraries (M40)**
  - *Extract performance parameters (depletion depth, charge-collection efficiency, timing, etc.)*
- **D2: Sensor-design guidelines (M46)**
- **D3: Performance characterisation results (M46)**
  - *Report on performance characterisation of test structures and sensors, including electrical, laser, source and test-beam measurements*
- **D4: Radiation tolerance assessment**
  - *Report on measured radiation tolerance of optimised test structures and sensors*
- **D5: Optimised interconnection process (M12)**
  - *Basic R&D with different adhesives, dispensing and curing methods on electrical test structures to achieve precise alignment, high and uniform capacitance and sufficient yield and reproducibility. Mechanical and electrical characterisation of the glued assemblies*
- **D6: Assemblies delivered (M40)**
  - Use the sensors produced in Task 6.3 (Sensor development) to produce assemblies of sensors and readout ASICs for all participating projects. Mount assemblies on test boards provided by the participating projects. Make wire-bond connections between chips and PCBs.
- **D7: Recommendation for industrialisation (M46)**
  - Investigate options for hybridisation of large-area assemblies. Adapt the interconnection technology for larger surface areas and make it suitable for mass production with high yield. Investigate wafer-to-wafer bonding options. Select industrial partners for initial tests.
- **D8: Final report (M46)**

LFoundry 150nm HVCMOS



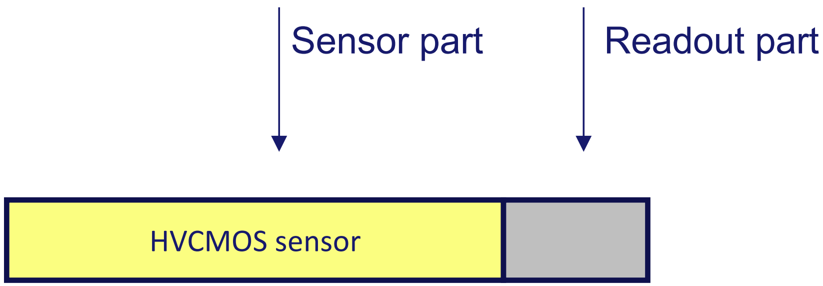
Design effort:

IFAE
R. Casanova
Uni. Barcelona
O. Alonso
Uni. Liverpool
S. Powell
E. Vilella
C. Zhang

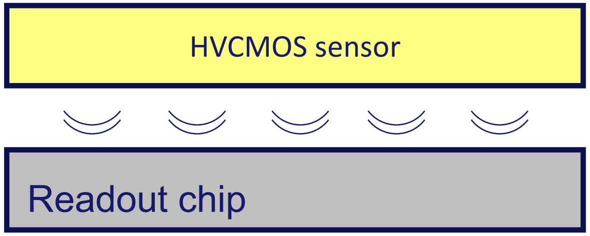
Scope for further design contributions…

Test structure 1	Simple CMOS capacitors to study oxide thickness
Test structure 2	10 x 10 matrix of very small pixels with passive readout
Test structure 3	10 x 10 matrix of very small pixels with 3T-like readout
Test structure 4	Small matrix of pixels for TCT, e-TCT and TPA-TCT measurements
Test structure 5	Single pixels for sensor capacitance measurements
Test structure 6	…

CCPD vs. monolithic sensor

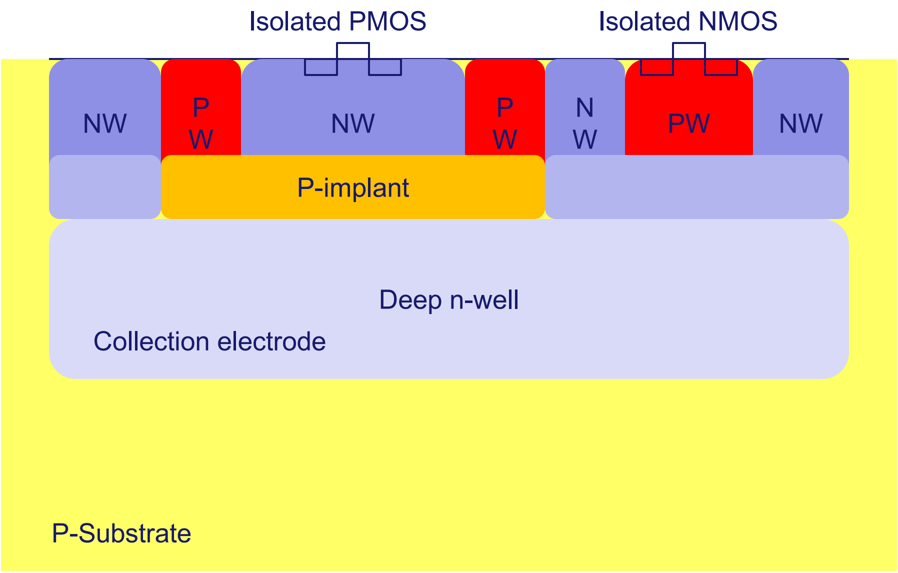


Monolithic detector

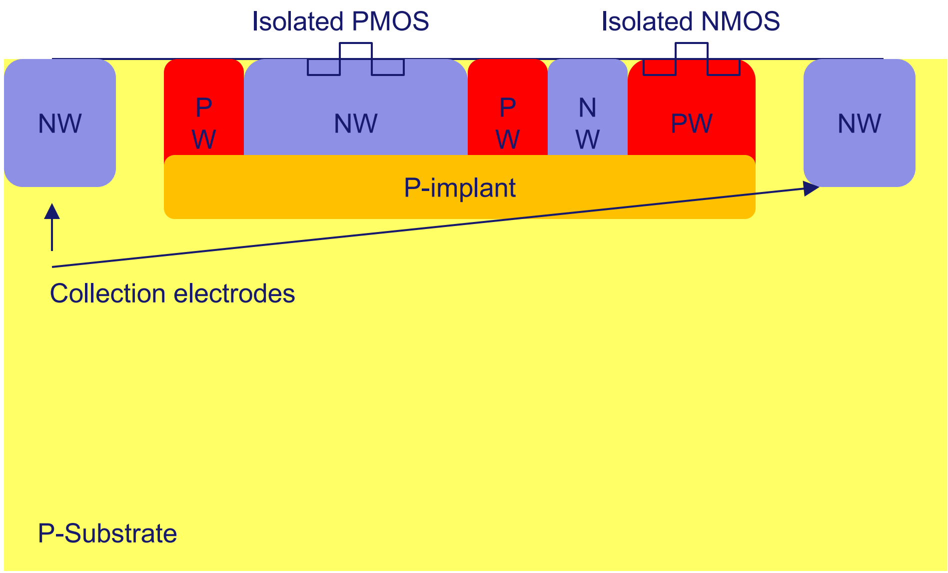


Capacitive coupled pixel detector - CCPD

Smart- vs. small-diode pixel

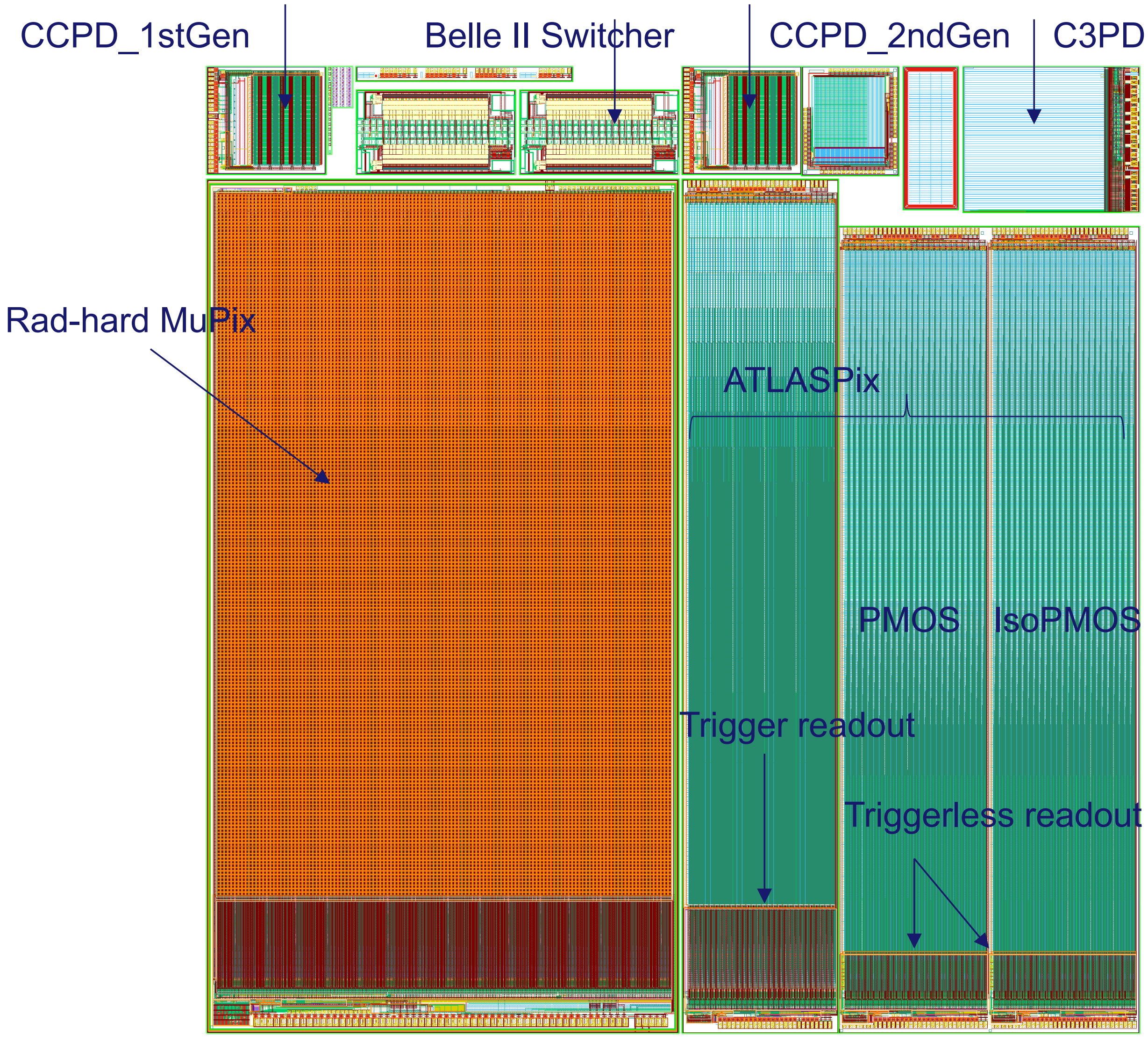


Smart diode pixel in AMS H18 and all LFA15 sensors

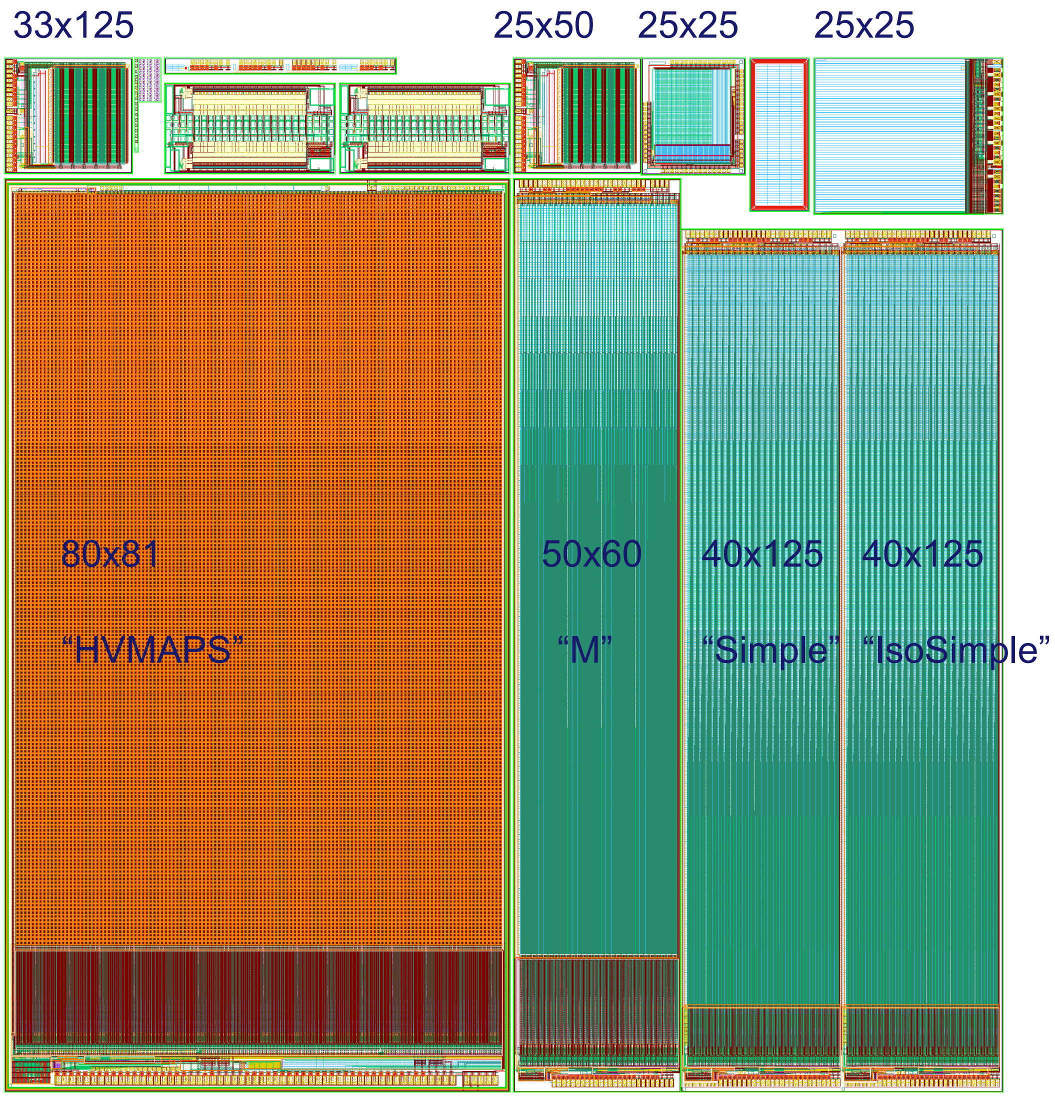


Small diode pixel in LFA15

MUPIX/ATLASPIX



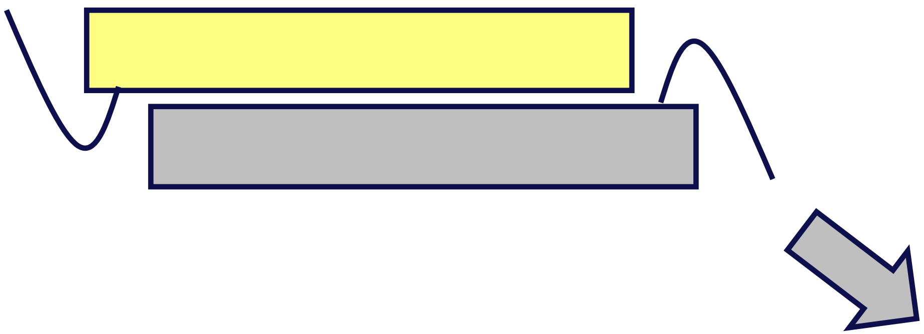
MUPIX/ATLASPIX



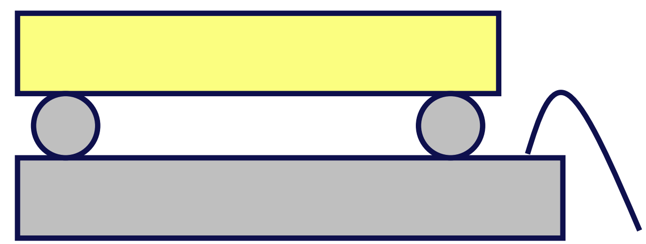
MuPix8, ATLASPIX

Different CCPD Variants:

1st generation

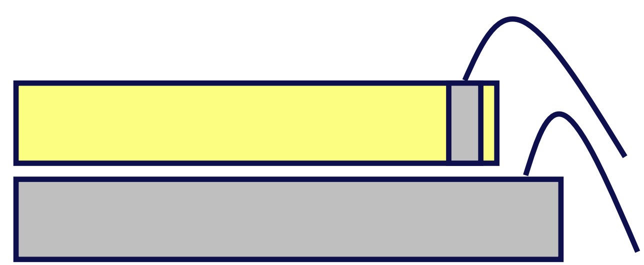


2nd generation



CCPD with a few standard bumps

OR



CCPD with TSVs