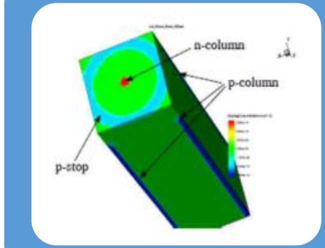
Summary of WP7 activities

Anna Macchiolo, Iván Vila

Paris, 2nd AIDA-2020 Annual Meeting, 07.04.2017

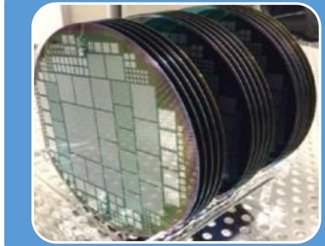
This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 654168.

Overview: Tasks



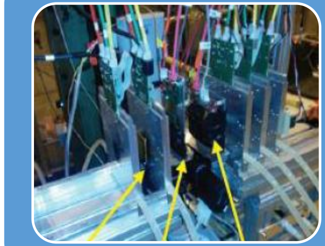
Device Simulation

- Layout optimization.
- Radiation damage modeling
- Optimization signal multiplication structures.



Sensor manufacturing

- Development & improvement of manufacturing processes for planar, 3D and LGAD devices.
- MPWR for thinned 3D and slim/active edge planar.



Detector performance assessment

- Hybrid thin planar & 3D pixels for HL-LHC environment.
- Very small size and thin pixel sensors for CLIC.
- Low Gain Avalanche Detectors for timing and tracking

CERN
FONDAZIONE BRUNO KESSLER
INFN Istituto Nazionale di Fisica Nucleare
Planck-Institut für Phy
(Werner-Heisenberg-Institut)
MANCHESTER 1824 The University of Manchester
CSIC
LAL LABORATOIRE DE L'ACCÉLÉRATEUR LINÉAIRE
LPNHE PARIS
UHH
UNIVERSIDAD DE SEVILLA

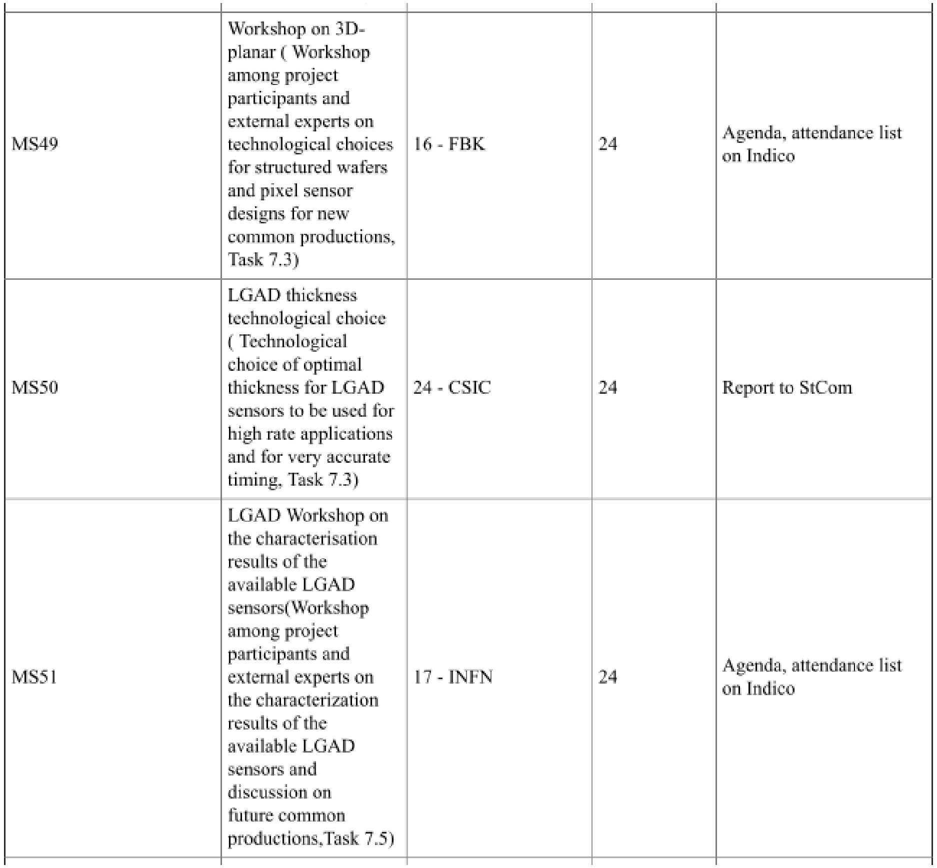
Approaching WP7 Deliverables

Deliverable	Responsible Group	Month due
D7.1 Simulation of 3D pixel sensor cells	INFN	M18 (OCT 2016)
D7.2 Simulation active edge	CERN	M18 (OCT 2016)
D7.3 LGAD simulation	INFN	M18 (OCT 2016)
D7.4 TCAD model radiation damage	INFN	M46 (MAR 2019)
D7.5 Wafer Layout MPW run WP7	CSIC	M30 (NOV 2017)
D7.6 Initial pixel characterization	UNIMAN	M24 (APRIL 2017)
D7.7 Final pixel characterization	MPG-MPP	M46 (MAR 2019)
D7.8 LGAD characterization	INFN	M46 (MAR 2019)

- D7.6 Based on devices from previous non-AIDA funded runs & WP7 2016 test beam results→ report is being circulated within WP7

Coming Milestones

- Dedicated workshop on the three sensor technologies (MS49, MS50) as full-day satellite meeting after the Trento Workshop (23th February)



MS49	Workshop on 3D-planar (Workshop among project participants and external experts on technological choices for structured wafers and pixel sensor designs for new common productions, Task 7.3)	16 - FBK	24	Agenda, attendance list on Indico
MS50	LGAD thickness technological choice (Technological choice of optimal thickness for LGAD sensors to be used for high rate applications and for very accurate timing, Task 7.3)	24 - CSIC	24	Report to StCom
MS51	LGAD Workshop on the characterisation results of the available LGAD sensors(Workshop among project participants and external experts on the characterization results of the available LGAD sensors and discussion on future common productions,Task 7.5)	17 - INFN	24	Agenda, attendance list on Indico

12th «Trento» Workshop on
Advanced Silicon Radiation Detectors
FBK, Trento, Italy
February 20-22, 2017

TOPICS
- Design and simulaztion
- Fabrication Technologies
- Radiation Hardness
- Read out
- System Issues
- Applications

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HFW Sadrozinski SCIPP UCSC USA
Y Unno KEK Japan

Common sensor productions

At least three common productions foreseen in WP7, one for each technology

  - Processing of MPWR for 3D and planar pixel sensors on thinned substrates, compatible with the RD53 chip

- Common submission of LGAD sensors
  - Prototyping of LGAD sensors on thin substrates, down to a bulk thickness of 50 µm

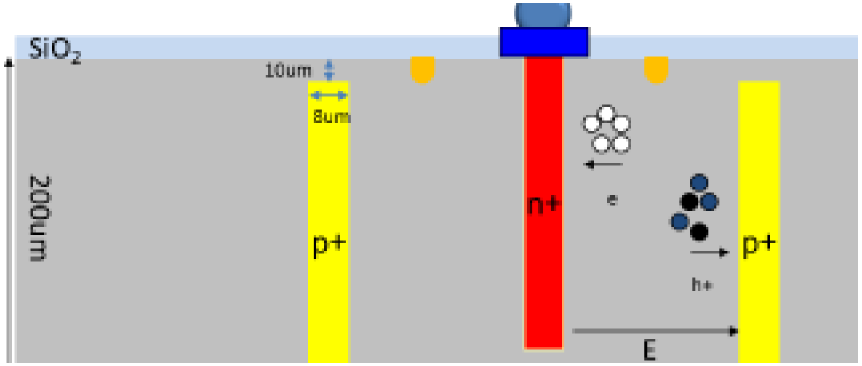
Deliverable	Responsible Group	Month due
D7.5 Wafer Layout MPW	CSIC	M30 (OCT 2017)

Milestone	Responsible Group	Month due
MS87 MPW runs completion	CSIC	M42 (OCT 2018)

3D production at FBK starting 1st QT of 2017
3D production at CNM beginning this week.

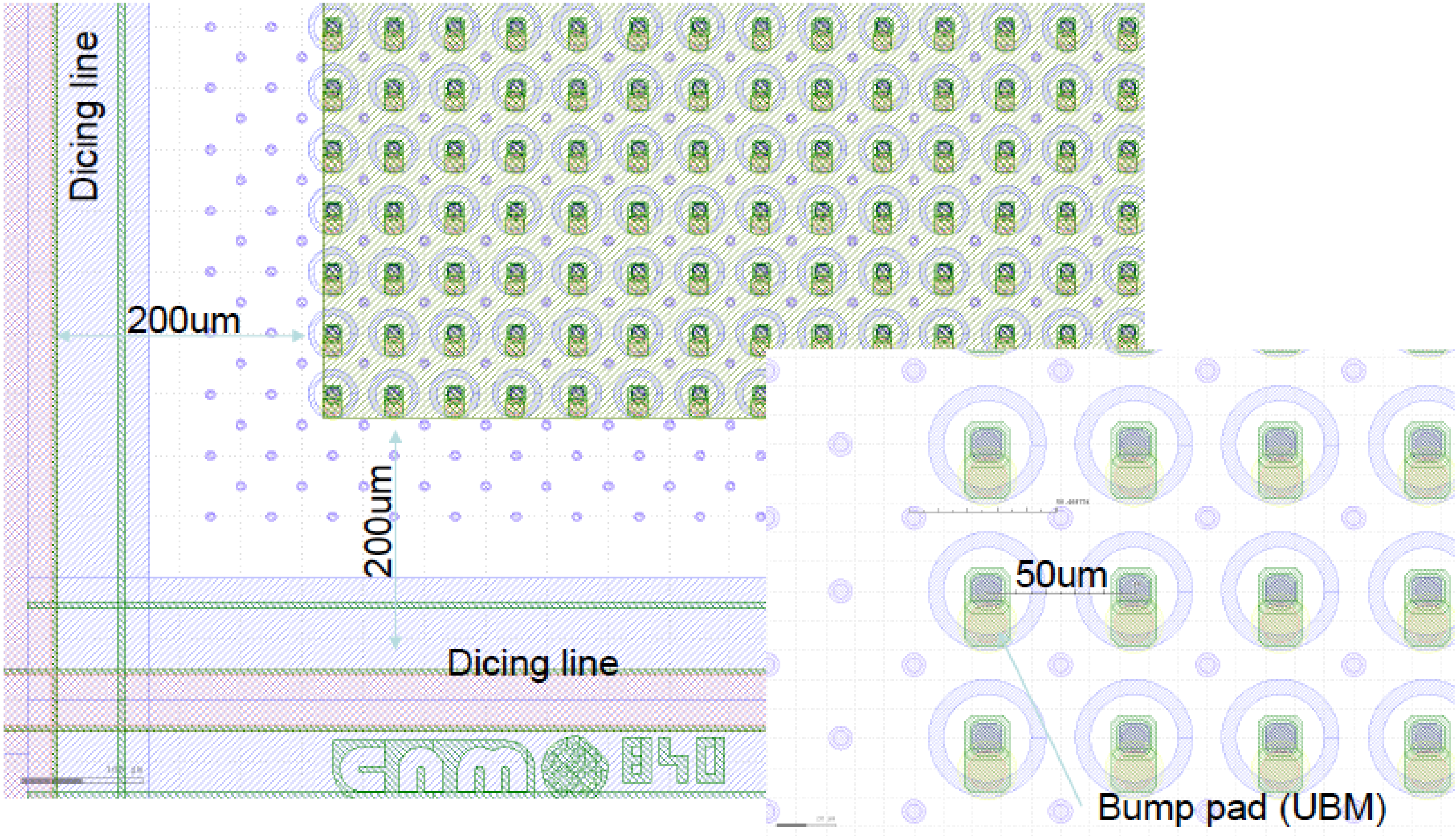
In the second half of 2017 → trying to achieve MS87 ahead of time
Active edge production at FBK
LGAD production at CNM

WP7 3D production at CNM

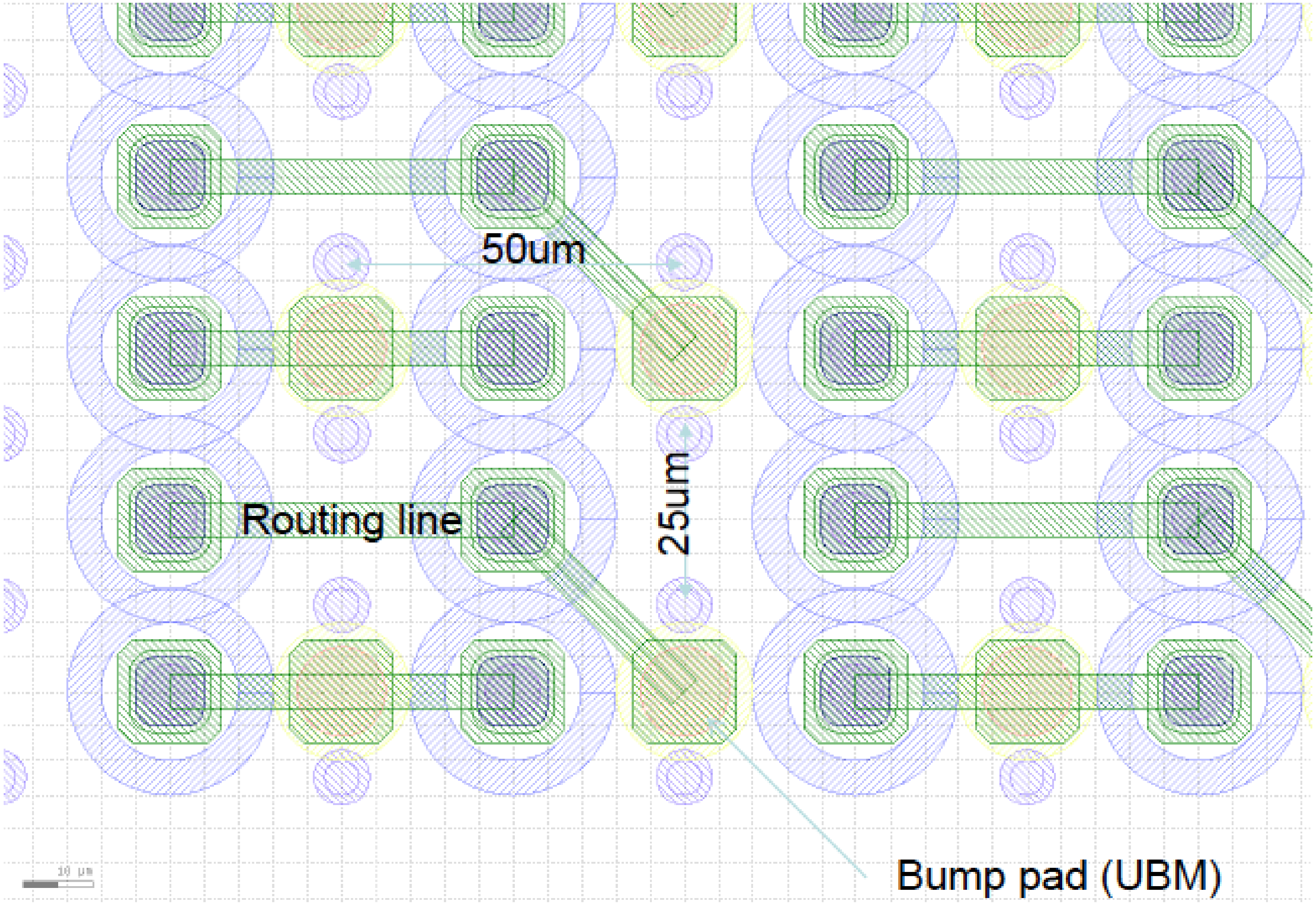


- 4” 200 μm thick wafers with double sided technology (developed and adopted for IBL), production started and due in Q4 2017
- Hole diameter 8 μm
- Mainly RD53 chip compatible sensors (pitch 50x50 μm^2):
  - 10 RD53 50x50um^2 1E
  - 6 RD53 25x100um^2 1E
  - 4 RD53 25x100um^2 2E
- Temporary metal for Quality Assurance before UBM and flip-chipping

3D at CNM: 50x50 μm^2 cells



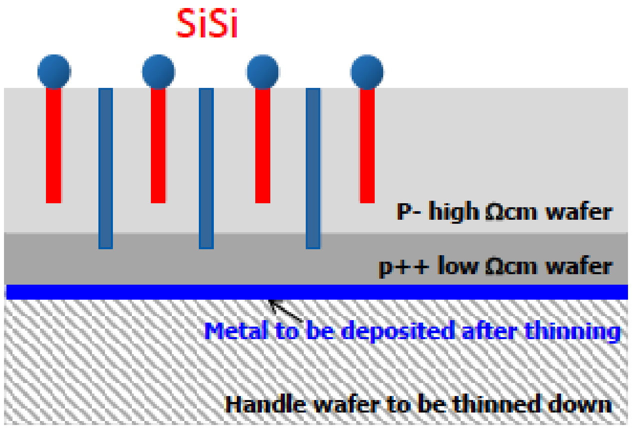
3D at CNM: 25x100 μm^2 cells

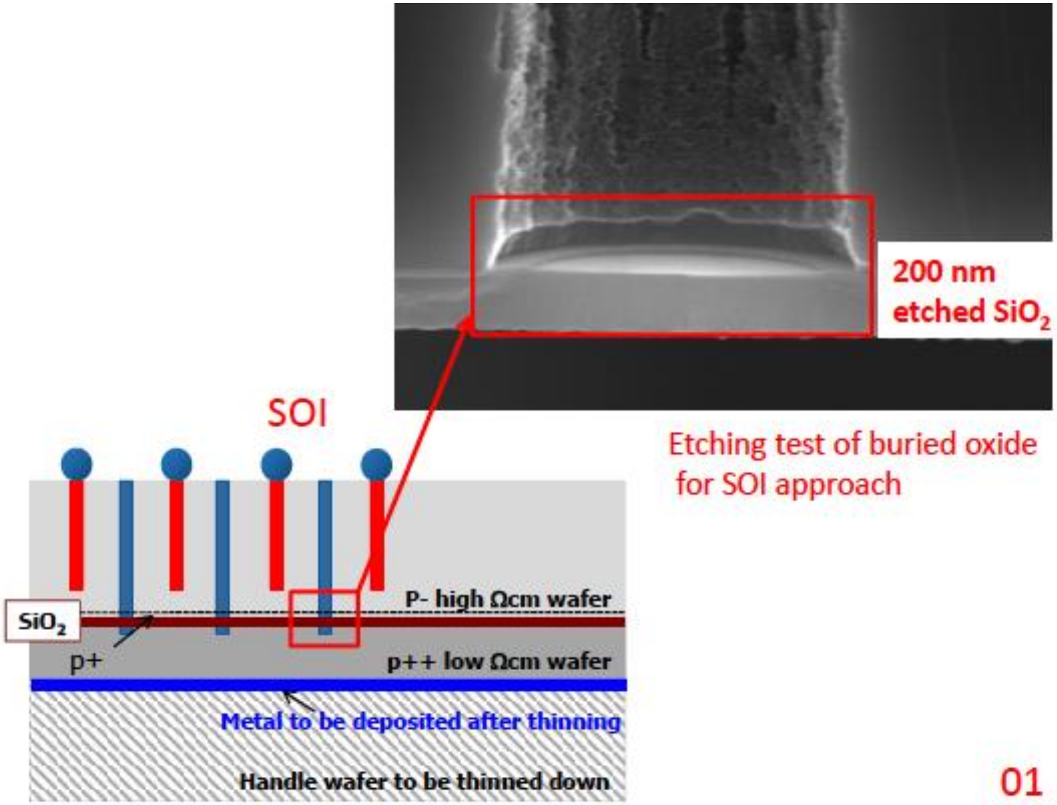


3D sensors at FBK

Single-sided process

- “Thin” active layer (130 μm): Si-Si or SOI
- Ohmic columns depth > active layer
- Junction columns depth < active layer
- Column diameter ~ 5 um
- Holes partially filled with poly
- Very slim edge (100 μm)

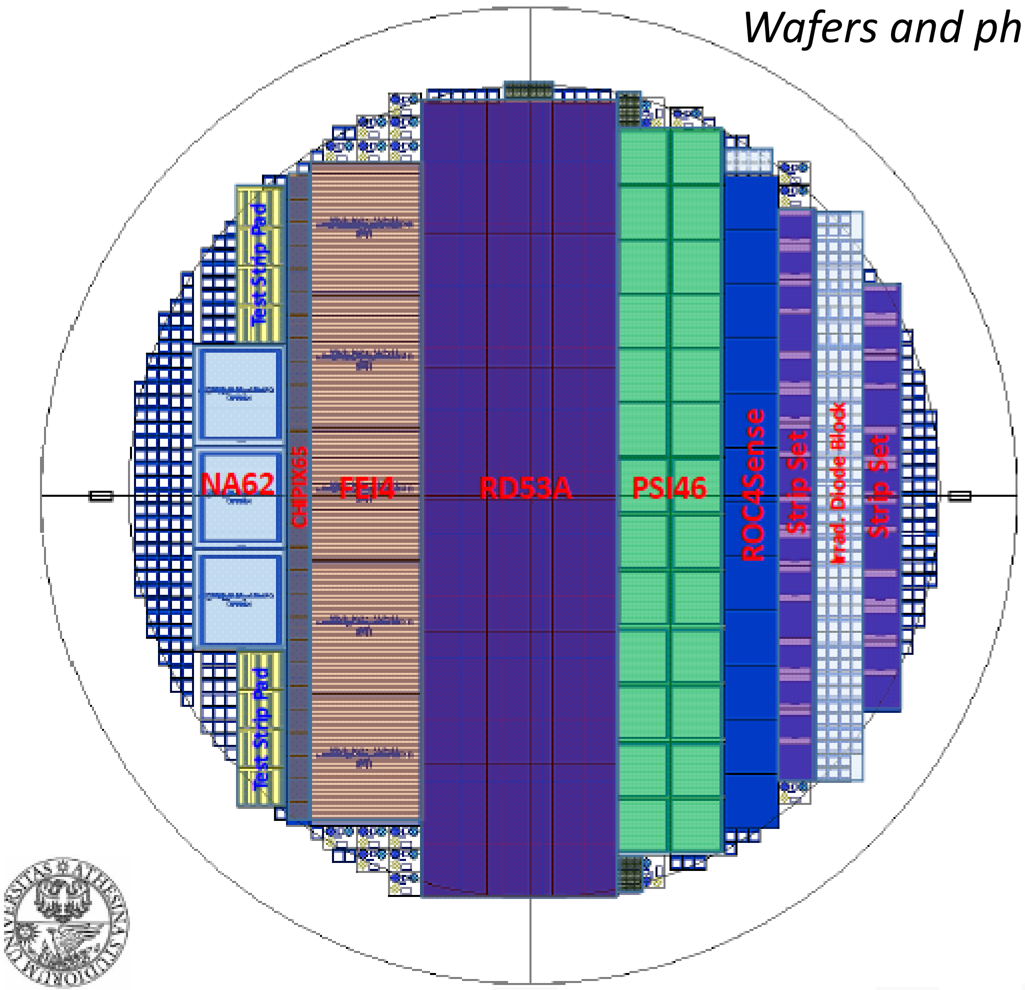




Etching test of buried oxide for SOI approach

WP7 3D production at FBK

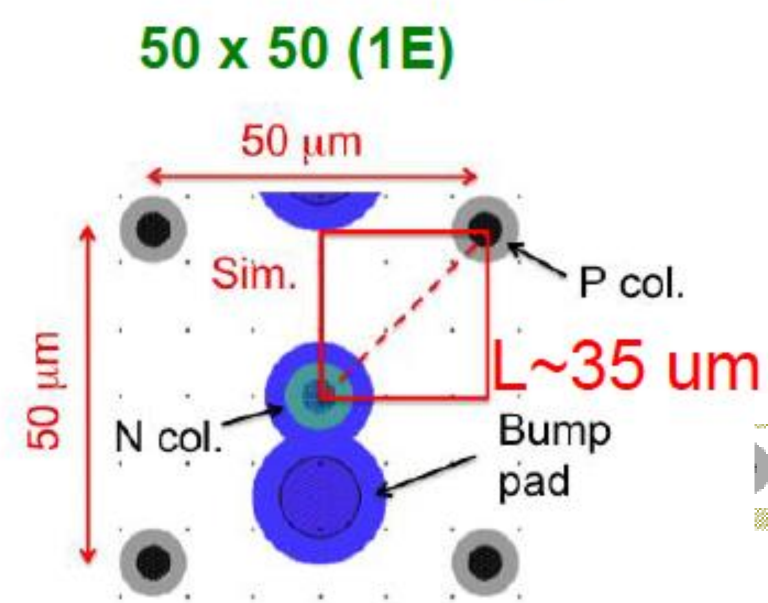
Wafers and photolitographic masks supplied by INFN



This wafer includes several improved designs as per earned experience from the first production at FBK.

- Aside conventional FEI4 and PSI46 complaint pixel sensors, the state of art RD53A and ROC4Sense compatible designs are introduced.

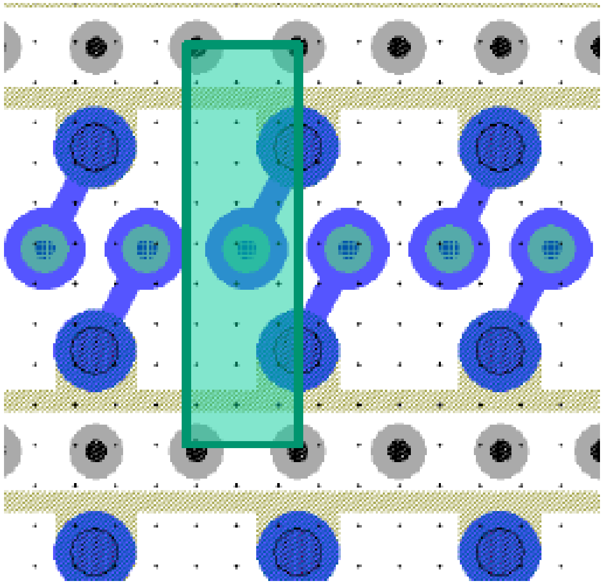
RD53 sensors - FBK

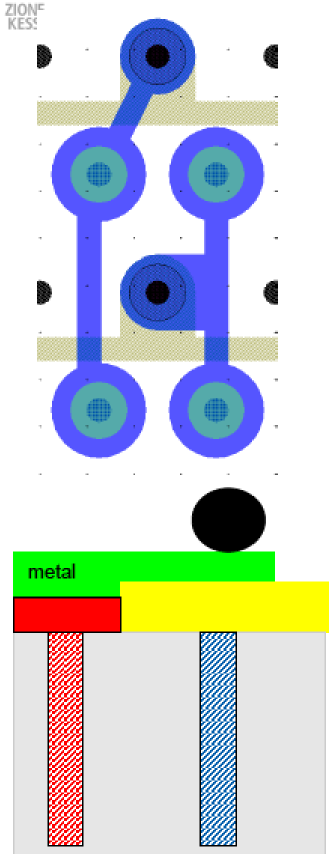


50x50 μm^2 can be designed with relaxed distances between bump and columns

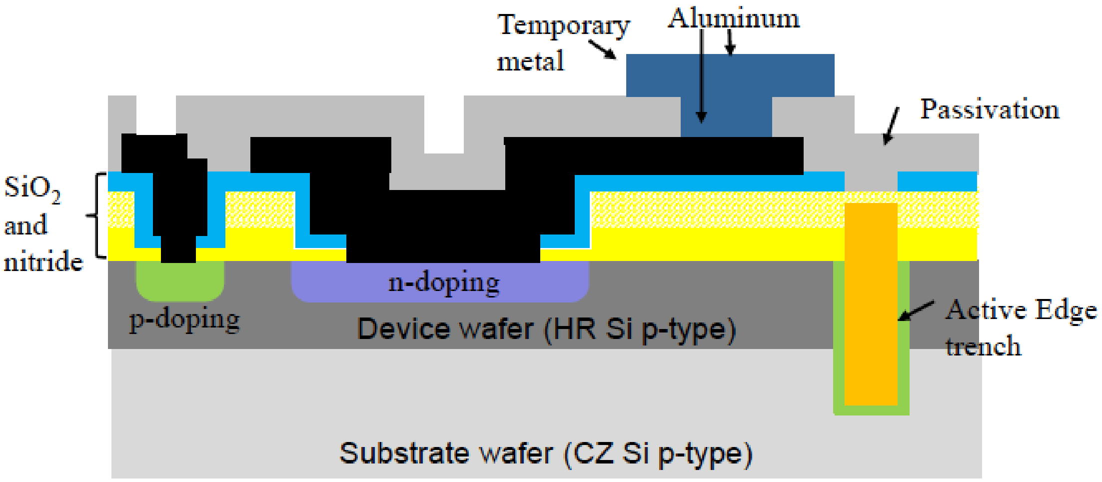
25x100 μm^2 can be difficult in 2E configuration:

- Place bumps on ohmic column
- Study radiation hardness of 1E configuration

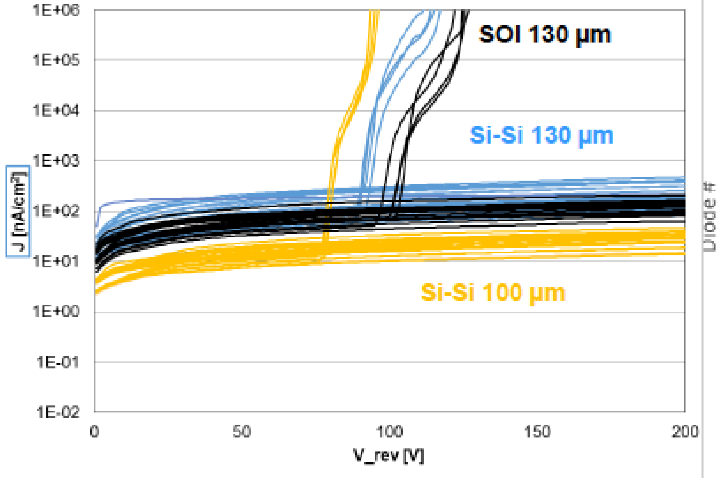


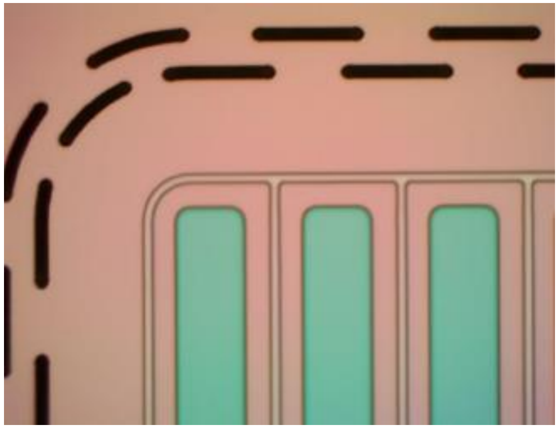


Active edge planar sensors- FBK



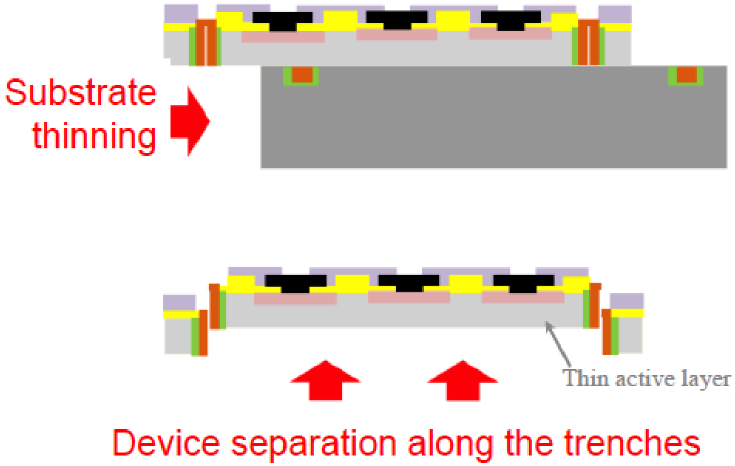
- 12 wafers on Si-Si and SOI material
- Staggered trenches
- Wafers now at IZM for interconnection

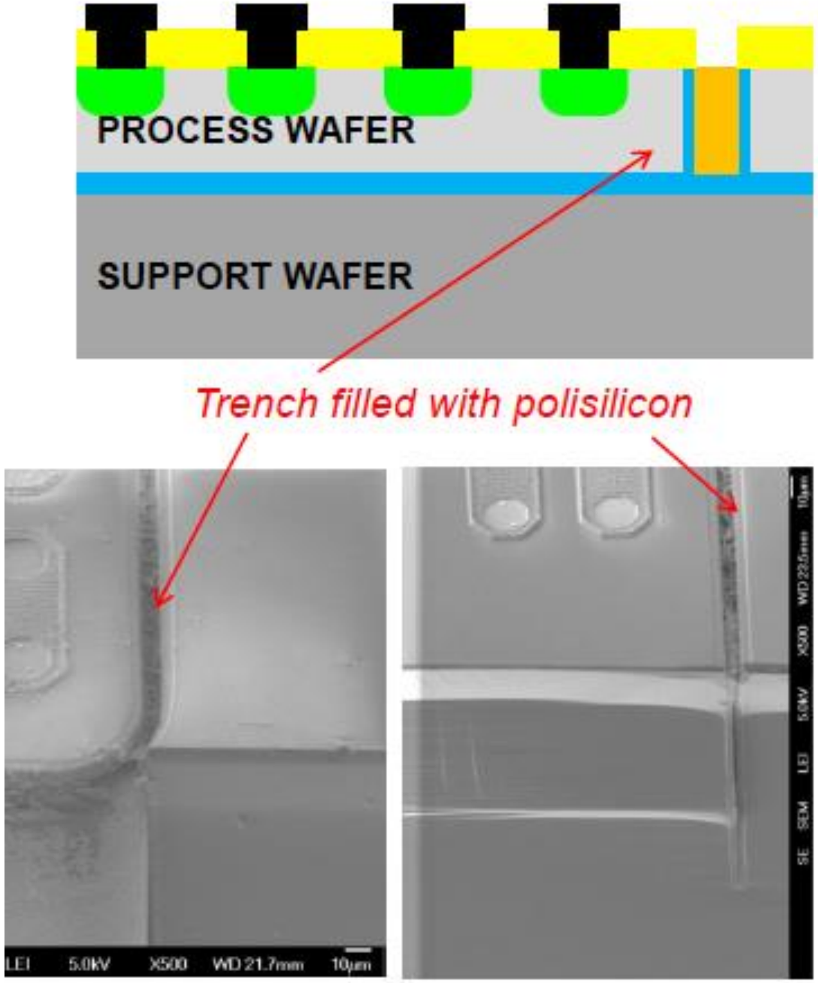




WP7 Edgeless production at FBK

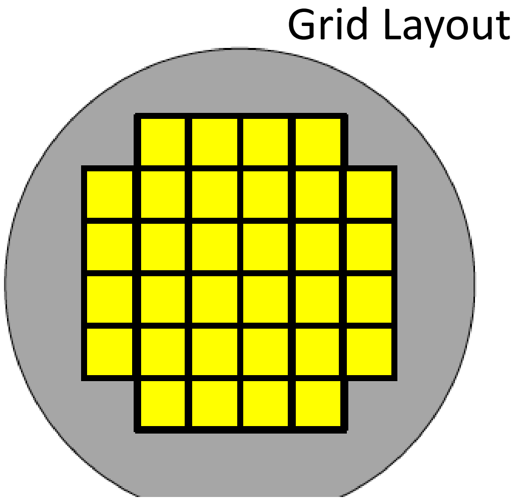
- Continuous trenches - Width < 10 um
- SOI (preferred) or Si-Si wafers with 100 and 130 µm thickness
- Poly-silicon filling
- Substrates thinning leads to structure separation

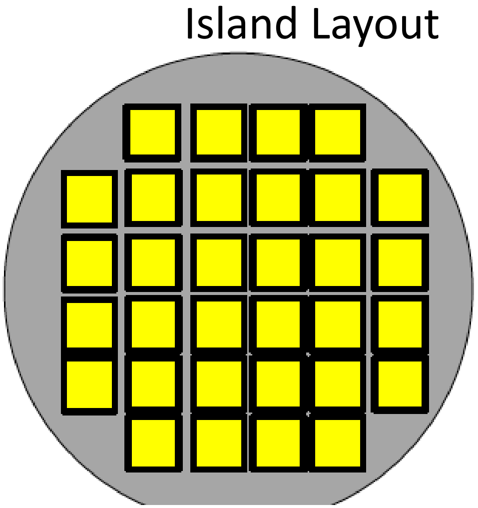


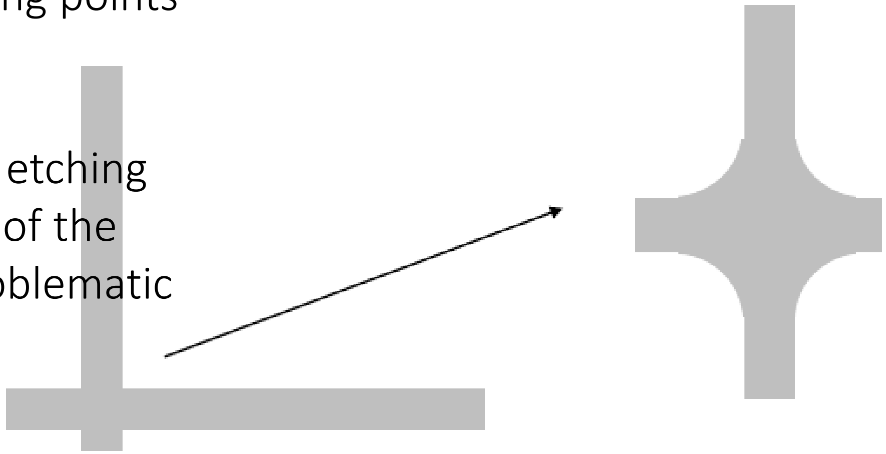


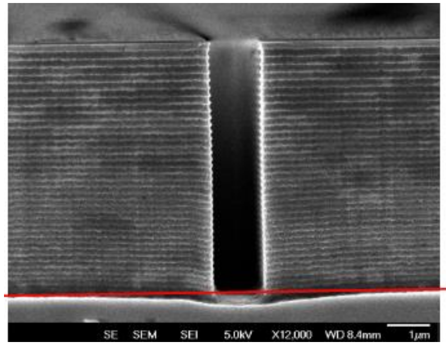
WP7 Edgeless production at FBK

- Choice of “grid” or “island” layout
- Grid layout probably easier to make the structures separate from each other during carrier thinning
- Island layout helps to avoid problems at the crossing points between trenches
- Local increase of DRIE etching rate and enlargement of the trench that is then problematic to fill


Grid Layout

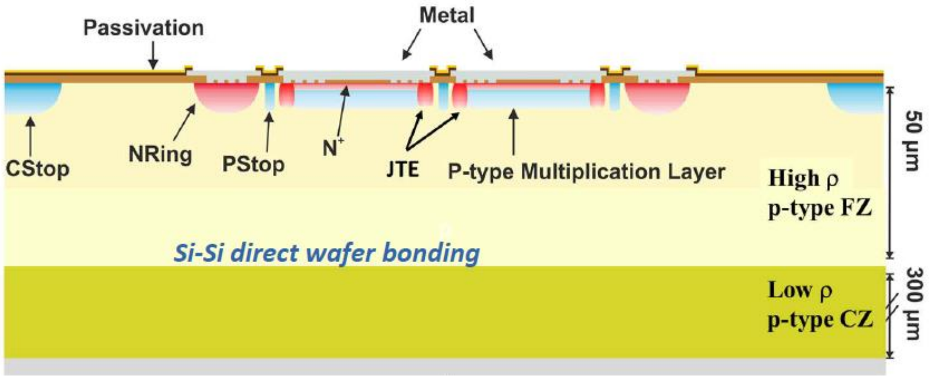

Island Layout

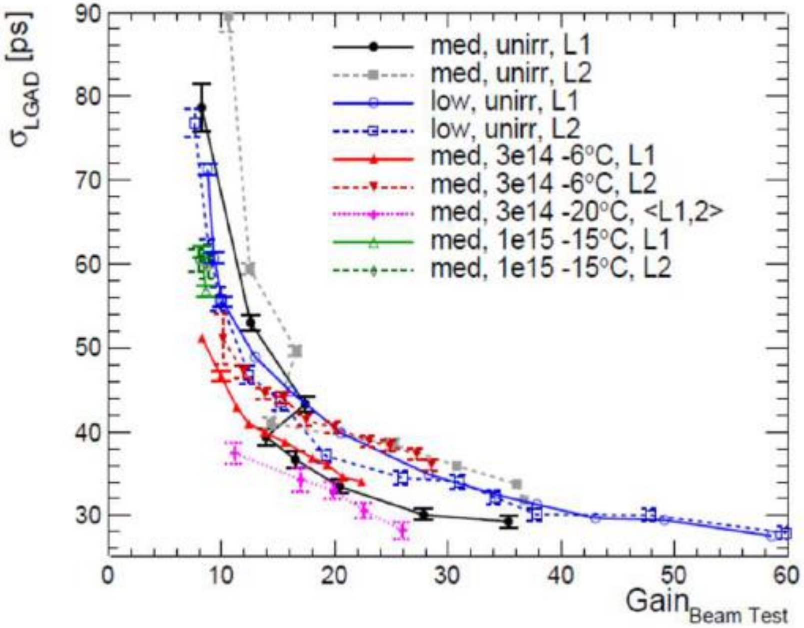




LGAD sensors for timing

- Example of LGAD structure for ATLAS HGTD applications





Previous studies demonstrated the LGAD gain reduction when fluence increases.

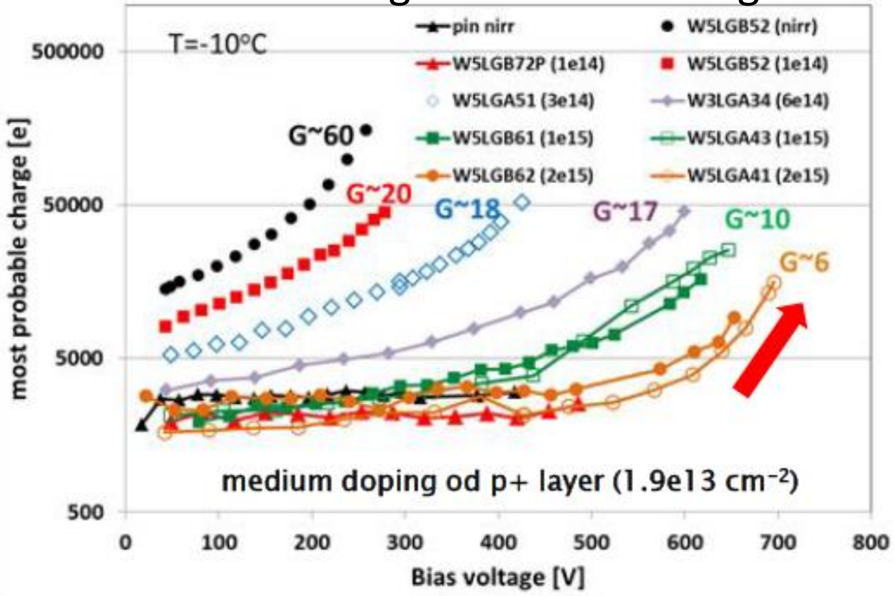
- There is no gain for fluences higher than $2{\cdot}10^{15}$ n_{eq} /cm^2

- Gain degradation described by acceptor removal mechanism → electrical deactivation of the Boron dopant and reduction of the multiplication layer electric field due to the trapping of thermal carriers in radiation induced traps

- Several mitigation strategies: thinner bulk works, Gallium doping does not improve

WP7 LGAD production at CNM

G. Kramberger Trento meeting 2017

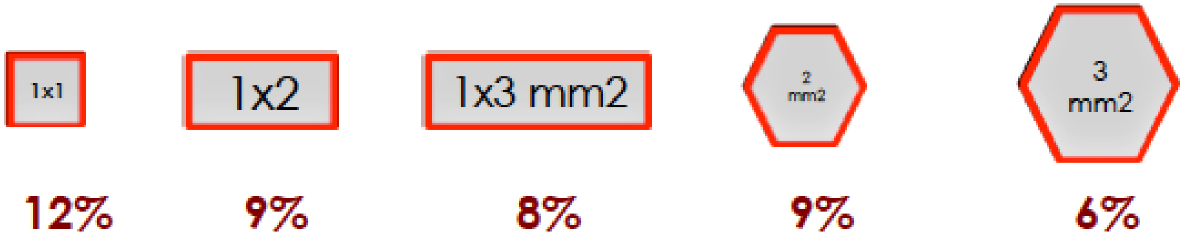


- At 2e15 the LGAD charge collection is very similar to pin diodes
- Gain coming from multiplication effects in the bulk (impact ionization) become important
- Common WP7 production aims to investigate thinner bulks to enhance the multiplication effects after irradiation (higher fields in thinner sensors)
  - 50 um active thickness as reference
  - Thickness around 30 um to investigate possible improvements in radiation hardness → precise target thickness to be determined with simulation at CNM

WP7 LGAD production at CNM

- Insert matrix of diodes: with various sizes 1x1 mm^2, 2x2 mm^2 pads to study edge termination.
- Reduce feature size of p-stop and JTE in the inter-pad region to reach >95% area where multiplication can take place

With present design 30 um width with no signal multiplication in the inter-pad region



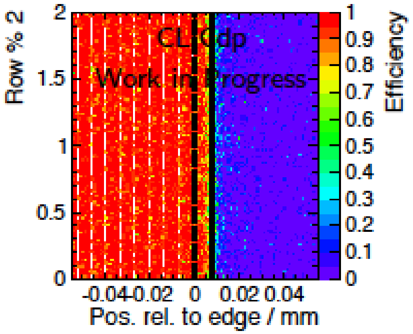
- Insert long/short strips to investigate the feasibility of achieving an ultra low material budget tracking + timing

Results of prototype characterization

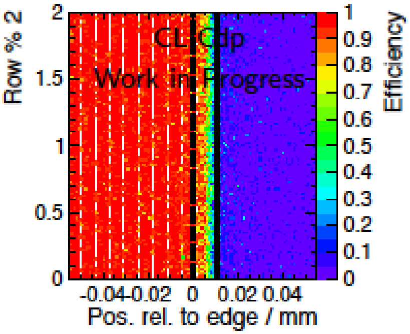
Planar sensors with active edges for CLIC

Timepix3 assemblies (55x55 um^2 pixel cells)

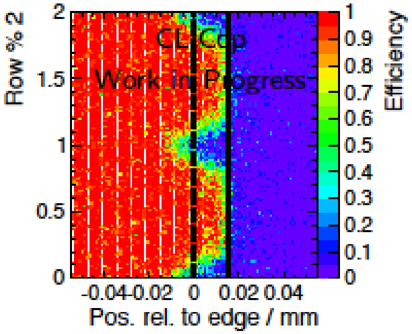
- 50 µm thick, 20-noGR



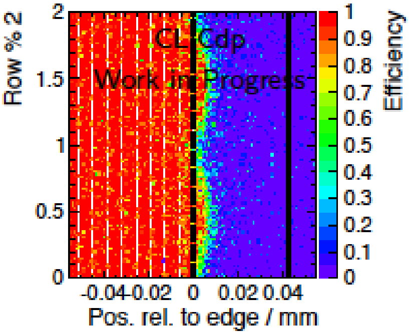
- 50 µm thick, 23-floatGR



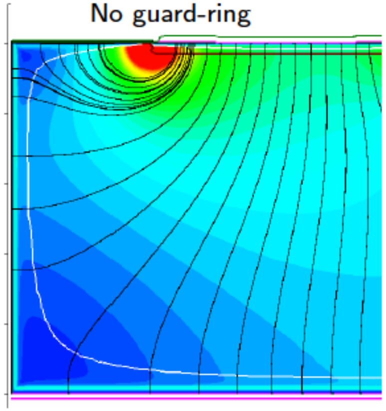
- 50 µm thick, 28-groundGR

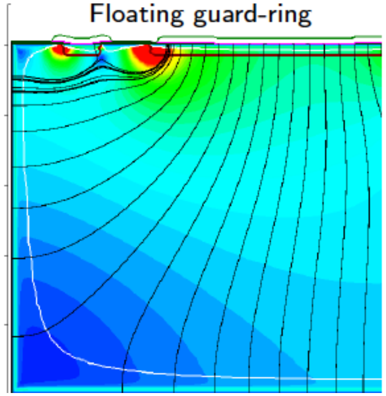


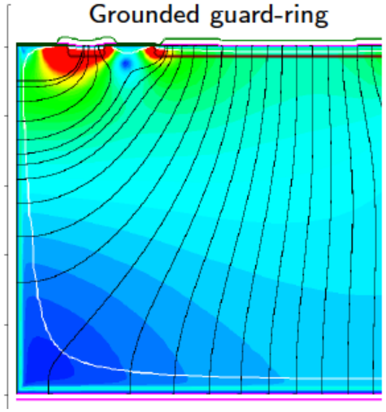
- 50 µm thick, 55-groundGR



50 um thickness
20 um edge

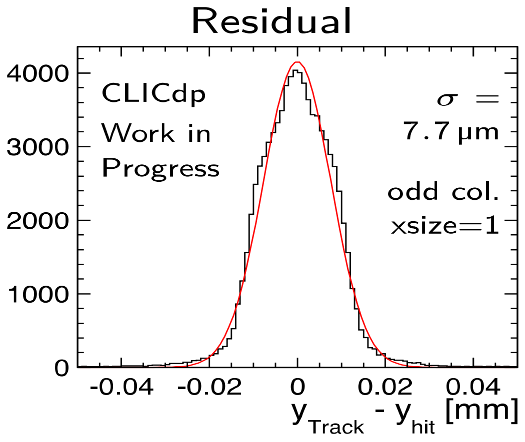


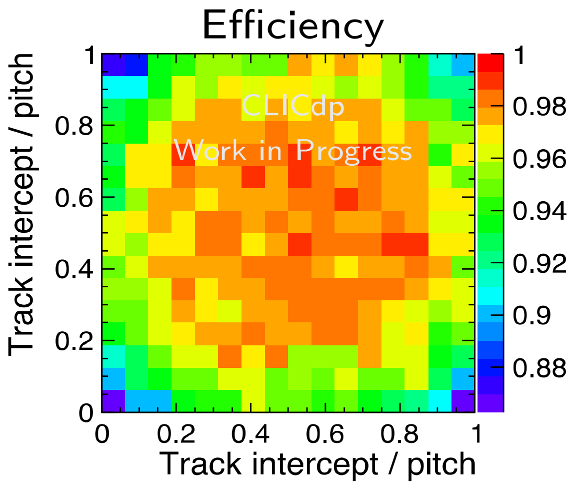


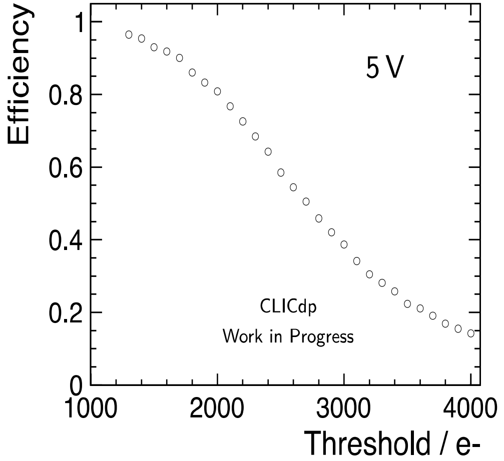


Planar sensors with active edges for CLIC

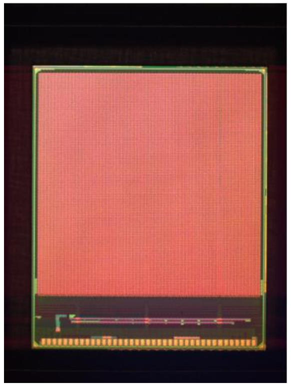
- 50 um thin ADVACAM sensors with active edges assembled to CLICpix chip (25x25 μm^2)

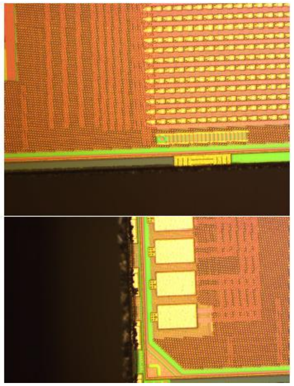






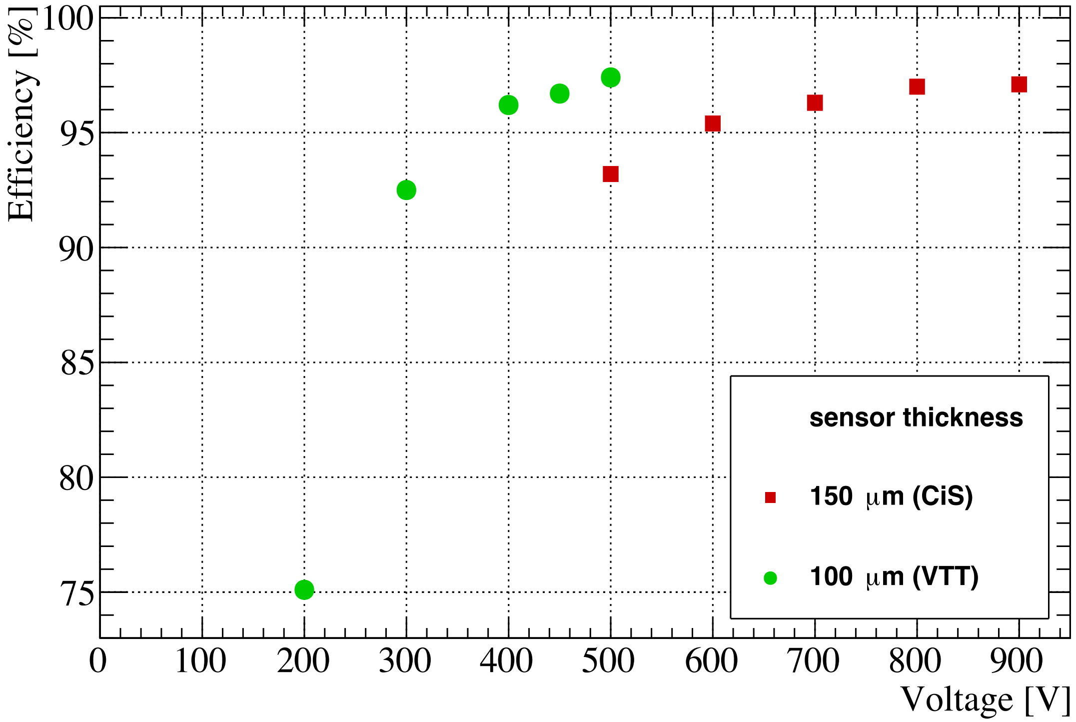
- Expected resolution achieved close to digital one because most of the clusters are 1-hit
- Fast decrease of the efficiency with the threshold
- Lower threshold expected with new chip CLICpix2, 128x128 matrix, 25 um pitch





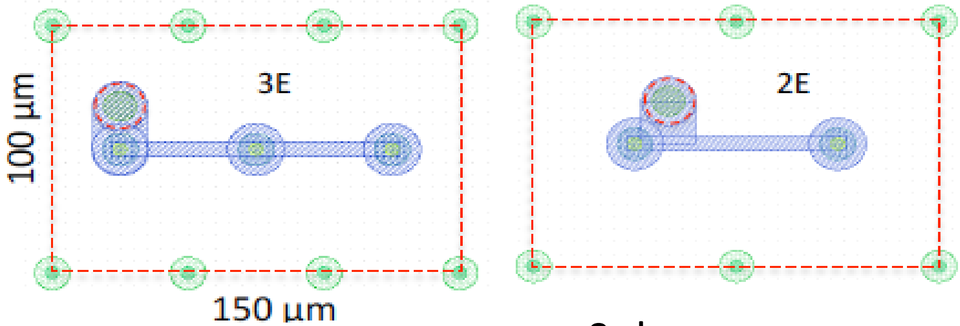
Thin planar sensors after irradiation

- Comparison of hit efficiencies after an irradiation to 1x10^{16} n_{eq}/cm^2 shows an earlier hit efficiency saturation for the module with 100 µm thick sensor compared to the CIS module with a 150 µm thick sensor.



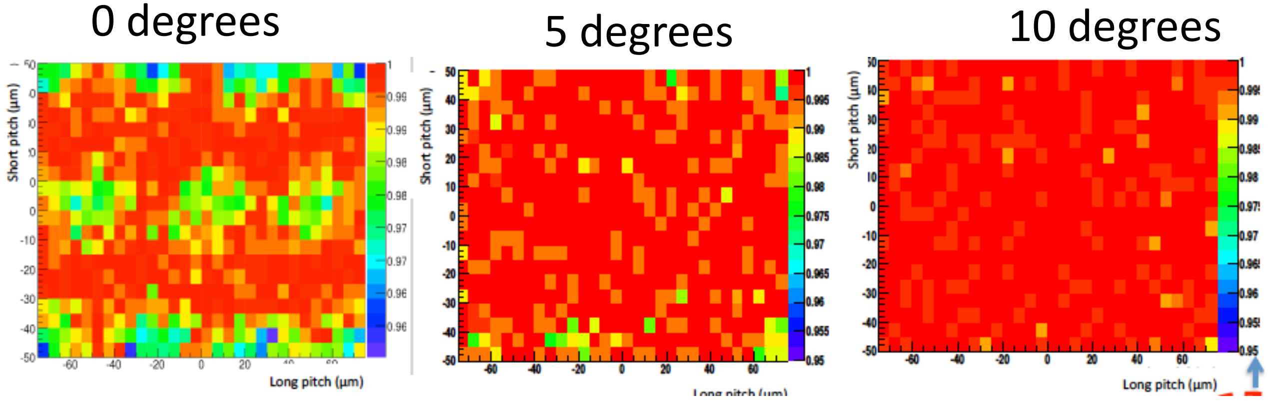
- Lower operation bias voltages at high fluence results in lower power dissipation and help to relax the requirements on the cooling system

Thin 3D sensors evaluation



- 3D 130 µm thin sensors with 2E and 3E configuration – FBK production

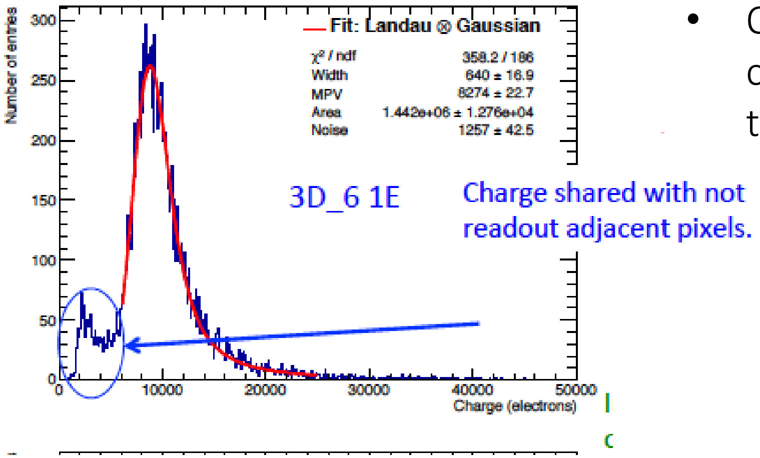
- Hit efficiency of 3D 130 µm thin sensors with 3E configuration
- Interconnected to CMS pixel chip PSI46dig
- 30V bias voltage



Angle (degrees)	Efficiency 3E	Efficiency 2E
0	99.27%	99.45%
5	99.77%	99.85%
10	99.88%	99.87%
max Δ Efficiency	0.62%	0.43%

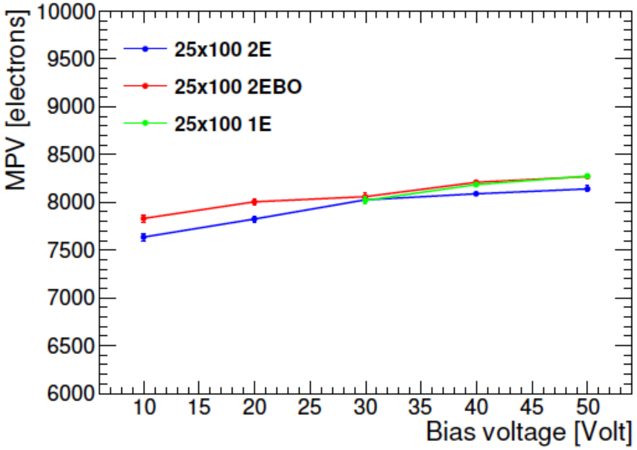
3D sensors: small pitch 25x100 μm^2

- 3D 130 μm thin sensors
- Interconnected to CMS pixel chip PSI46dig

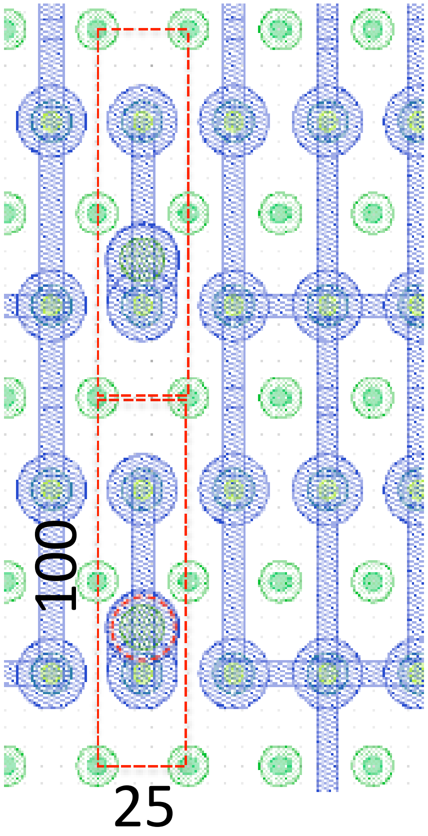


3D_6 1E

Charge shared with not readout adjacent pixels.



- Only one out of 6 columns is read-out while the others are grounded

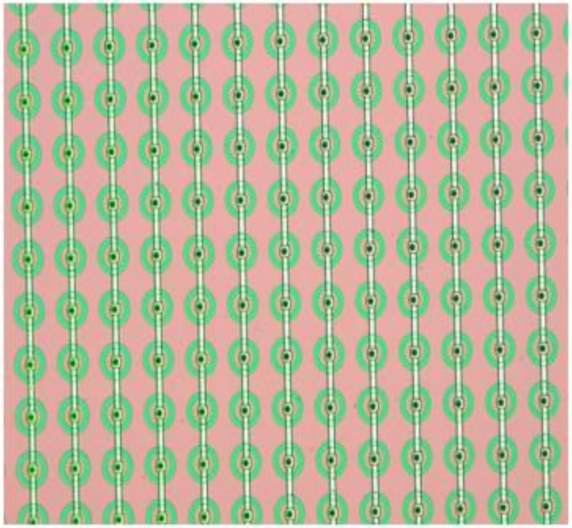


- No striking differences among the three 25μm pitch 3D prototypes, all of them behaving well

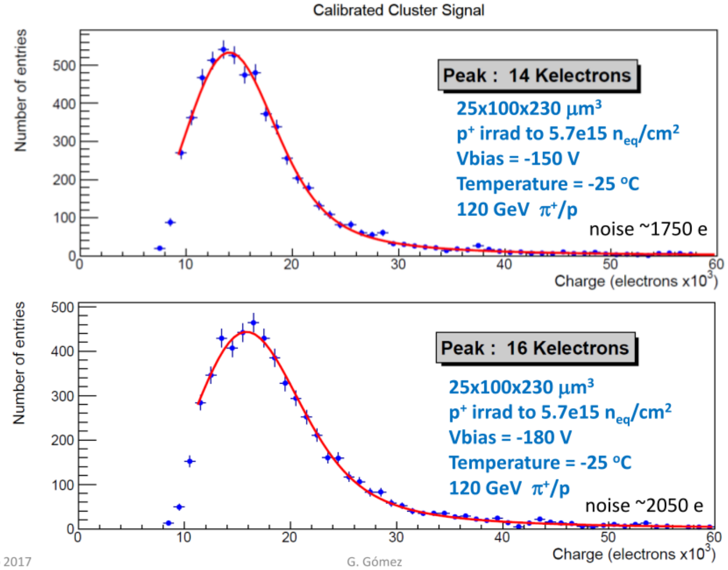
3D strips with 50x50 μm^2 cells

- 3D 50x50 μm^2 pixel cells produced at CNM where the junction columns are shorted through a metal line

- Read-out through the Beetle chip



Φ = 5.7e15 n_{eq}/cm^2, 3D 25x100x230 μm^3, -25°C, -150V and -180V, π/p beam



Trento 2017 G. Gómez

Very high CCE at 5.7e15 already at moderate bias voltages

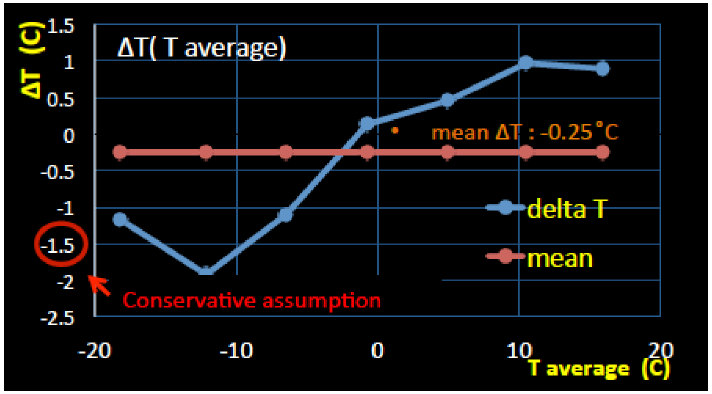
Sensor Geometry	Operating Conditions	Fluence (protons) (n_{eq}/cm^2)	Charge (electrons x 10^3)	CCE* (%)
3D 50 x 50 x 230 μm^3	-25 V, 22 °C	0	17	100
3D 25 x 100 x 230 μm^3	-30 V, -25 °C	0	17	100
3D 25 x 100 x 230 μm^3	-150 V, -25 °C	5.7×10^{15}	14	82
3D 25 x 100 x 230 μm^3	-180 V, -25 °C	5.7×10^{15}	16	94

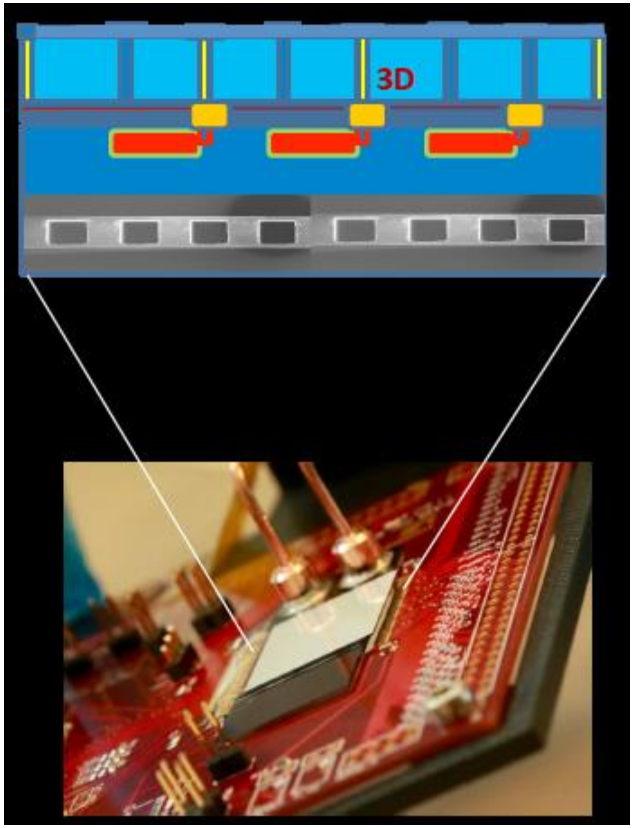
*** CCE with respect to non-irradiated sensor**

3D sensors with μ-channel cooling

Cross activity with WP9

- CNM 3D sensor from CNM IBL qualification batch
- FE-I4A: thinned to 100um at IZM
- Si-Si micro-channels designed by CERN PH-DT, produced by PH-DT in EPFL CMi cleanroom, direct bonding CSEM





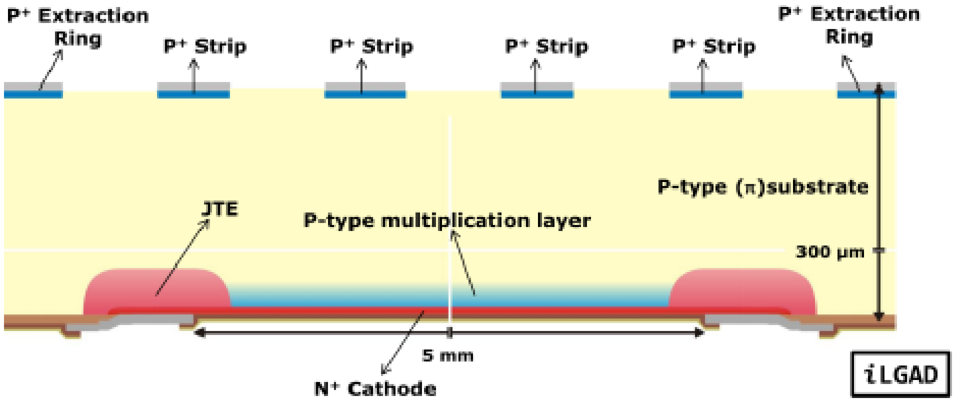
Thermal Figure of Merit= ΔT . A / Power =

4 K cm^2/ W for example ITK studies ~ 13 K cm^2/ W

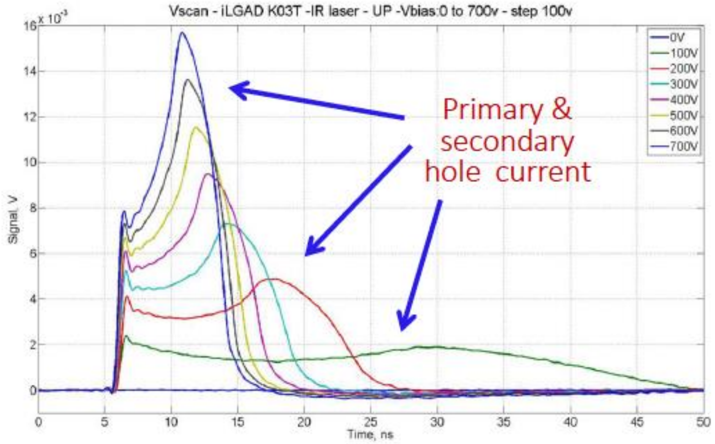
p-in-p LGAD strips – Inverted LGADs

- P-in-p LGADs with segmented cathod, hole read-out

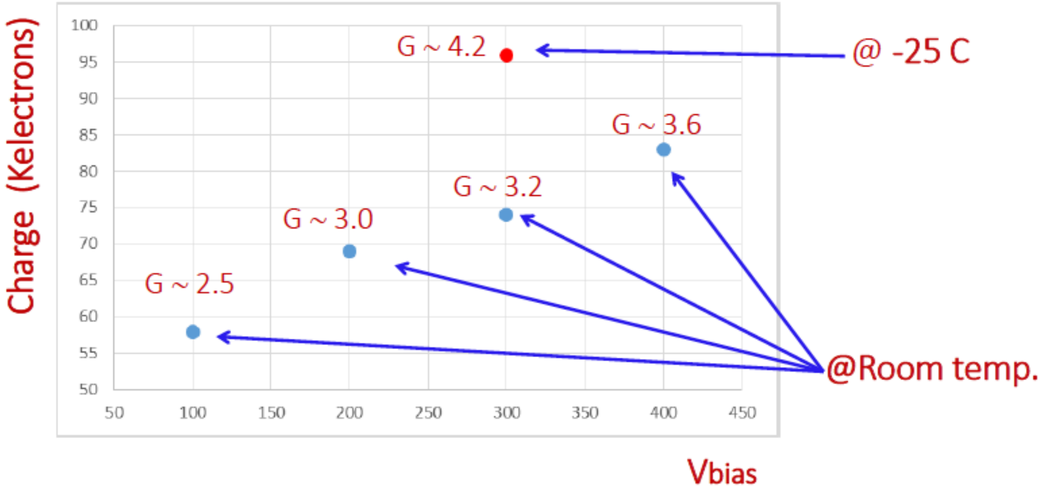
- DC-strip with 160 um pitch



- Gain capability of strip devices demonstrated with Infrared Laser Transient Current



Results from WP7 test-beam: at -25C a S/N value of 90 has been achieved



Simulation activities

The Perugia Model

Develop a TCAD model for the study of radiation damage effect in silicon detectors valid up to the particle fluence expected at the end of HL-LHC operations in the inner layers of vertex detectors at HL-LHC (ATLAS and CMS)

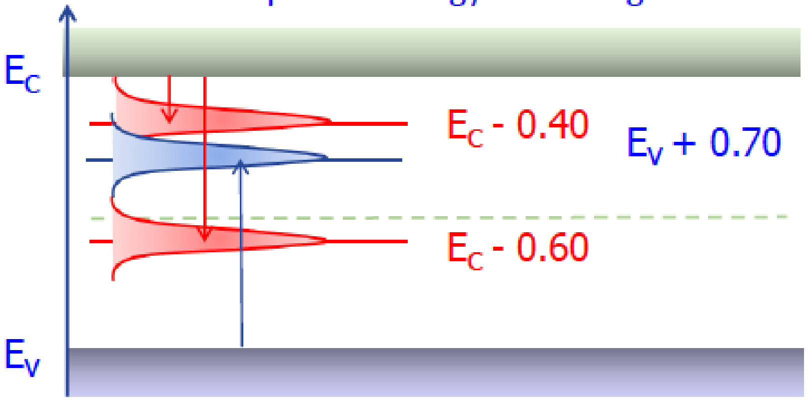
Update on the TCAD surface damage model

Interstrip resistance
Gated Control diode

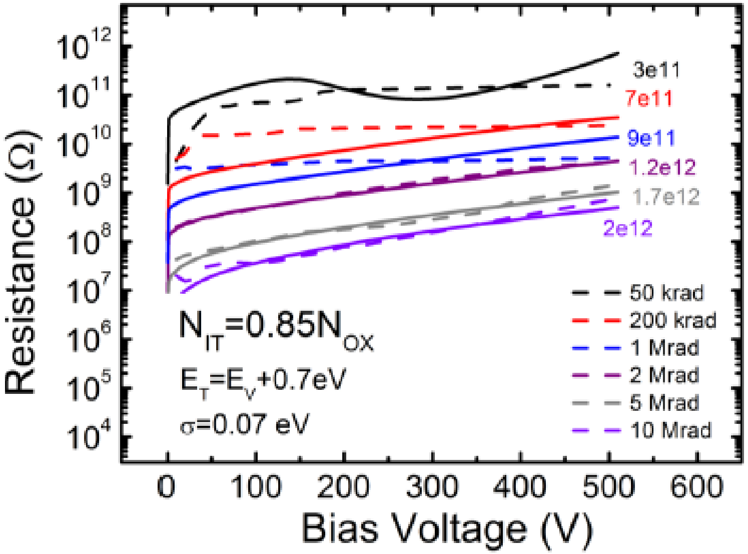
Simulation vs Measurements for Interstrip res.

Gaussian modelling of the interface state energy

- Interface trap state energy modelling

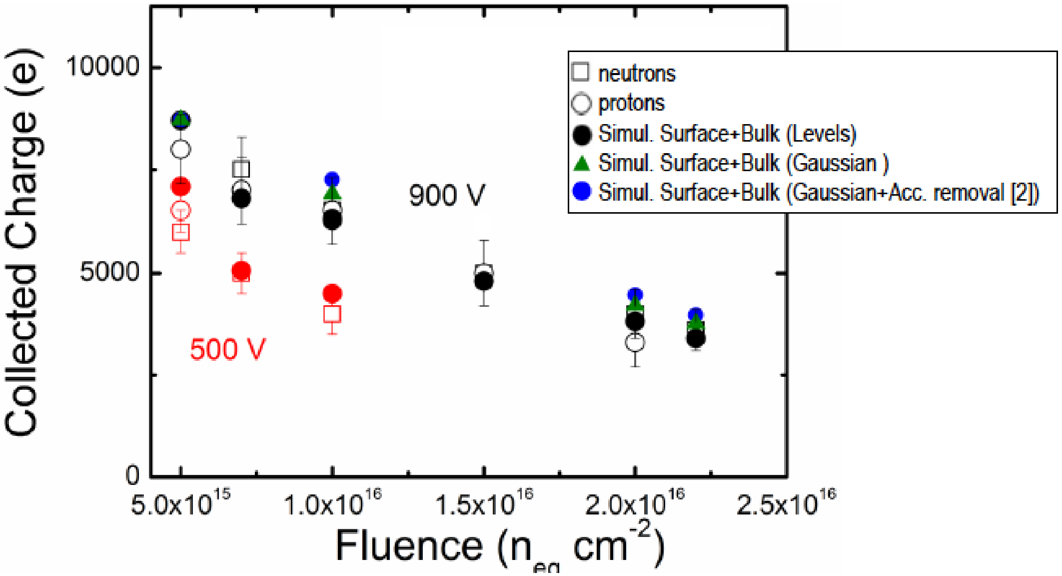


Gaussian Distribution

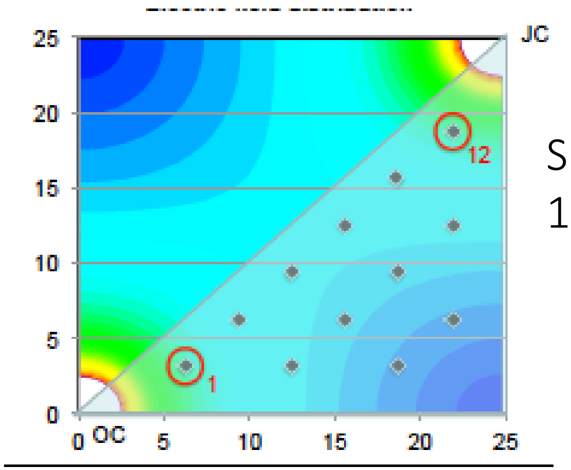


The Perugia Model

Nice agreement with charge collection results obtained on irradiated strips

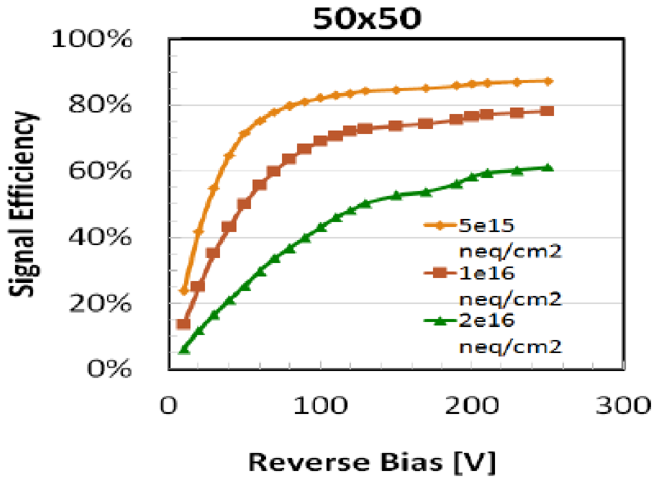


Perugia model applied to study 3D charge collection properties after irradiation -



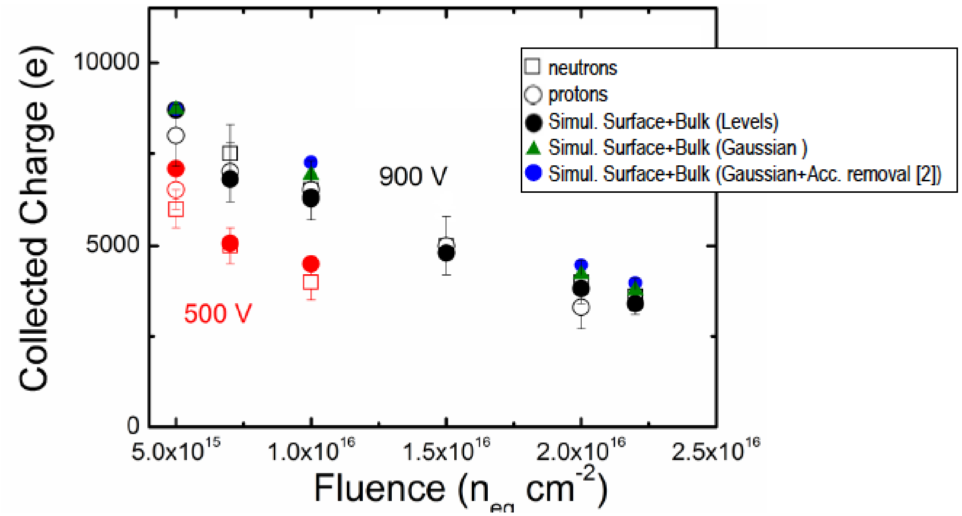
Simplified domain (~2d)

1 um thick slice (1/4 or 1/8 pixel)

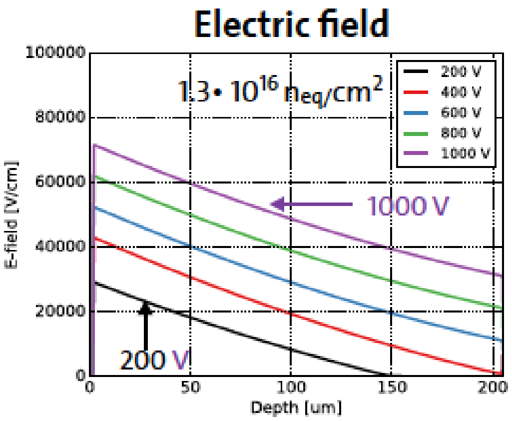


The Perugia Model

Nice agreement with charge collection results obtained on irradiated strips



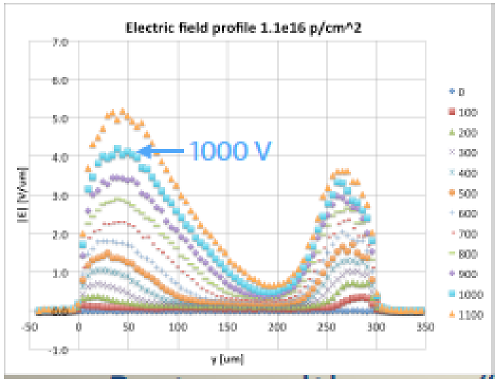
.. Some possible features to be checked and evaluated in the future:



No double junction!

Edge-TCT measurements

(M. Mikuž: Tredi,Paris, FEB 2016)



Simulation outlook

- At the moment the Perugia model is the only one available in our community where a systematic tuning is being performed with charge collection data above 1e15

- In order to perform a systematic comparison among different models for implementing radiation damage in TCAD simulations a larger set of data on charge collection for segmented devices (strip + pixels) should be compiled – try to start this effort in WP7 collecting results from R&D activities carried out in the framework of ATLAS and CMS

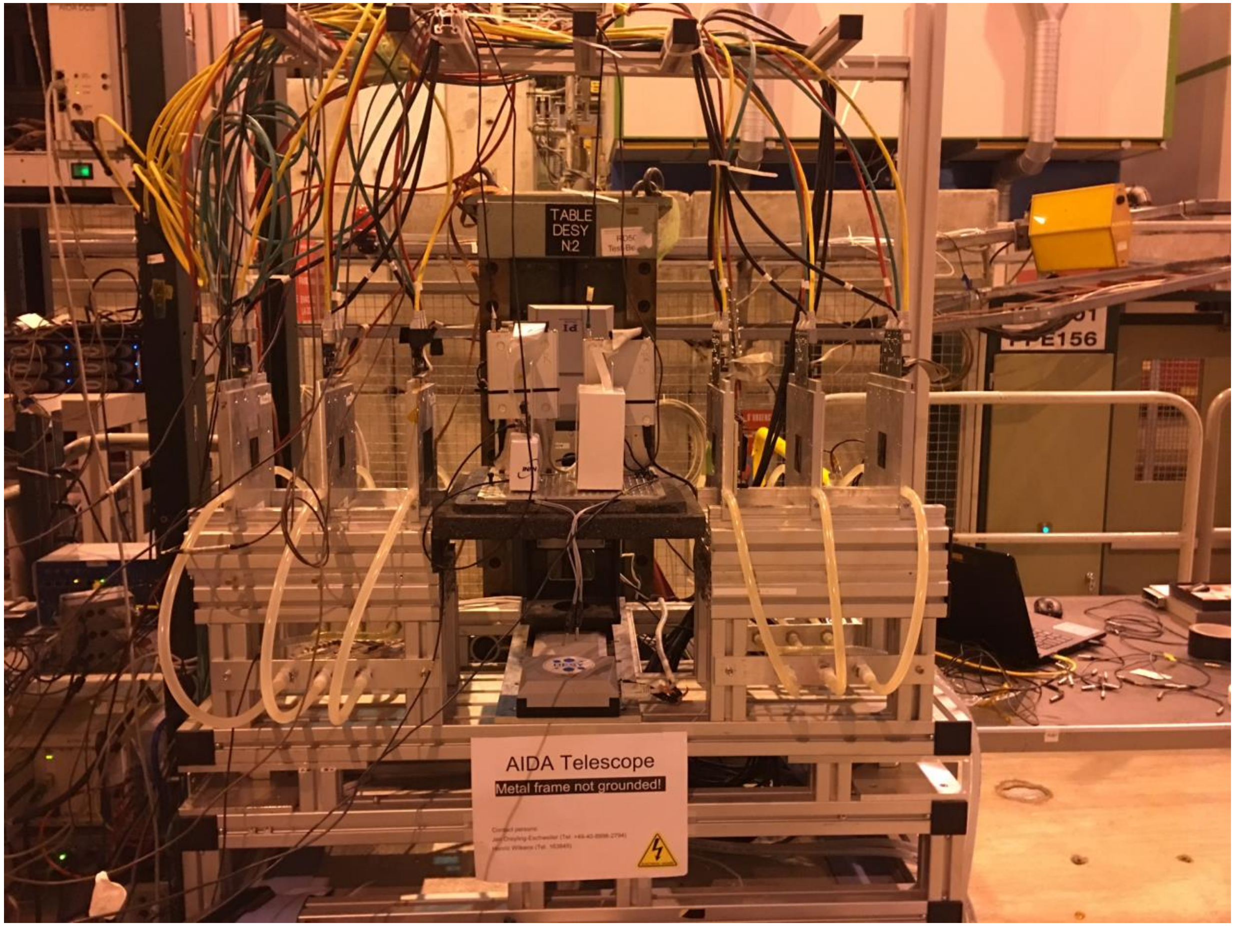
- The deliverable on the TCAD model is foreseen for the end of the project, enough time to check and refine tunings of the TCAD models

WP7 test-beam 2017

We got one week of test-beam awarded at CERN-SPS in H6 (both H6A and H6B areas)

17-24 May

- Cooling box and two telescopes available
- Open to all groups participating to WP7



Conclusions and Outlook

WP7 activities have entered the most important phase of our activities

- Knowledge acquired through simulation activities and preliminary characterization of devices has been injected into the design and organization of common sensor runs

  - Work done across ATLAS, CMS, CLIC communities → sharing of information and optimization of resources

- All deliverables and milestones on time, trying to advance the completion of common runs in such a way that enough time is available for a complete characterization of the devices before the end of the project