Second Annual Meeting
WP4 Status Report

Christophe de la Taille (CNRS/IN2P3)
Valerio Re (INFN/Univ. Bergamo)

LPNHE, Paris, April 7, 2017

WP4: microelectronics and interconnections

- WP Coordinators: Christophe de la Taille, Valerio Re

- Goal : provide chips and interconnections to detectors developed by other WPs

- Task 1: Scientific coordination (CNRS-OMEGA, INFN-UNIBG)
- Task 2 : 65 nm chips for trackers (CERN)
  - Fine pitch, low power, advanced digital processing
- Task 3 : SiGe 130nm for calorimeters/gaseous (IN2P3)
  - Highly integrated charge and time measurement
- Task 4 : interconnections between 65 nm chips and pixel sensors (INFN)
  - TSVs in 65 nm CMOS wafers, bonding of 65 nm chips to sensors, exploration of fine pitch bonding processes

AIDA WP4 milestones

MS4.1	Architectural review of deliverable chips in 65nm run	M14 (accomplished)
MS4.2	**Final design review of 65nm**	**M30 (October 2017)**
MS4.3	Test report of deliverable D4.1	M46 (February 2019)
MS4.4	**Selection of SiGe foundry**	**M14 (accomplished)**
MS4.5	**Final design review of deliverable chips in SiGe run**	**M30 (October 2017)**
MS4.6	Test report of deliverable D4.2	M46
MS4.7	**Selection of TSV process**	**M14 (accomplished)**
MS4.8	**Final design review of deliverable D4.3 (TSV in 65nm)**	**M30 (October 2017)**
MS4.9	Test report of deliverable D4.3	M46

Thursday 06 April 2017

WP4 Micro-electronics and interconnections: Micro-electronics and interconnections - **Amphi Charpak (09:00-10:30)**

    -Conveners: Valerio Re; Christophe De La Taille; Valerio Re

time	[id] title	presenter
09:00	[386] Introduction	RE, Valerio
09:10	[375] Design and submission of the RD53A chip	GAIONI, Luigi GAIONI, Luigi
09:30	[376] AIDA/RD53 activities in Perugia	MARCONI, Sara MARCONI, sara
09:45	[377] The CHIPIX65 demonstrator chip	DEMARIA, Lino
10:00	[378] Update on CPPM activities towards development in 65nm	ROZANOV, Alexandre MENOUNI, Mohsine
10:15	[379] Update on 65nm developments in Bonn	KRUEGER, Hans

WP4 Micro-electronics and interconnections: Micro-electronics and interconnections - **Amphi Charpak (11:00-12:30)**

    -Conveners: Valerio Re; Christophe De La Taille; Valerio Re

time	[id] title	presenter
11:00	[380] A high precision TDC for CMS MG-RPC in TSMC130n	MATHEZ, Herve
11:15	[381] developments at OMEGA and DESY/Heidelberg	SEGUIN-MOREAU, Nathalie
11:30	[382] developments at AGH Krakow	IDZIK, Marek
11:45	[383] discussion on 130 nm WP4.3	
12:00	[384] TSV developments at UBonn	HUEGGING, Fabian HUEGGING, Fabian
12:15	[385] TSV developments in Glasgow	BATES, Richard BATES, Richard

• Deliverable chips in 65 nm

- This work is carried out in the frame of the CERN RD53 international R&D program developing a first generation of pixel readout chip prototypes for ATLAS and CMS at HL-LHC

- Develop expertise on TSMC 65 nm CMOS selected by CERN for HEP

- Two small size prototypes were fabricated and are available for testing with sensors

- A large-scale prototype will be submitted May 2017 in an engineering run

- This will deliver full wafers for the interconnection with pixel sensors (task 4.4)

65 nm CMOS radiation hardness studies

- The 65 nm process qualified for 500 Mrad
  M. Menouni, CPPM
  - Limited leakage current
  - A strong drive loss for small size PMOS devices and the damage increases with the temperature
  - RD53 Front end chip (pixel environment)
    - Avoid the use of narrow or short transistors for analog design
    - Corner Models developed for 200 Mrad and 500 Mrad and used to characterize digital cells
    - DRAD chip designed by CERN group indicates which digital libraries can be used
    - The temperature effect can be avoided and delayed by keeping cold : -20°C for 5 years and keeping unbiased at room temp for few months

- SEU tolerant latches for pixel and global configurations were designed and tested

- A new prototype designed to test the effect of the DNW on the SEU tolerance and will be used to test and qualify the Monitoring block, temperature and irradiation sensors as it is implemented in the RD53A chip

Small-medium size 65 nm CMOS prototypes

- Two different chips with a 64x64 50 μm x 50 μm pixel matrix (about 16 mm^2) with different architectures for the analog front-end and the digital readout, different techniques for digital-to-analog isolation,…

- FE65_P2 (Bonn, LBNL), submitted end of September 2015, delivered by the foundry in December 2015 and successfully tested by UBONN with good results. FE65-P2 chips were connected to pixel sensors and the resulting modules were tested in a beam at CERN and SLAC

- CHIPIX65 demonstrator (INFN): submitted July 2016, delivered by the foundry at the end of September 2016. This chip is also fully functional, and tests gave very good results in terms of noise and threshold dispersion. The CHIPIX65 prototype will be soon connected to 3D and planar pixel sensors.

CHIPIX65 demonstrator

Lino Demaria, INFN Torino
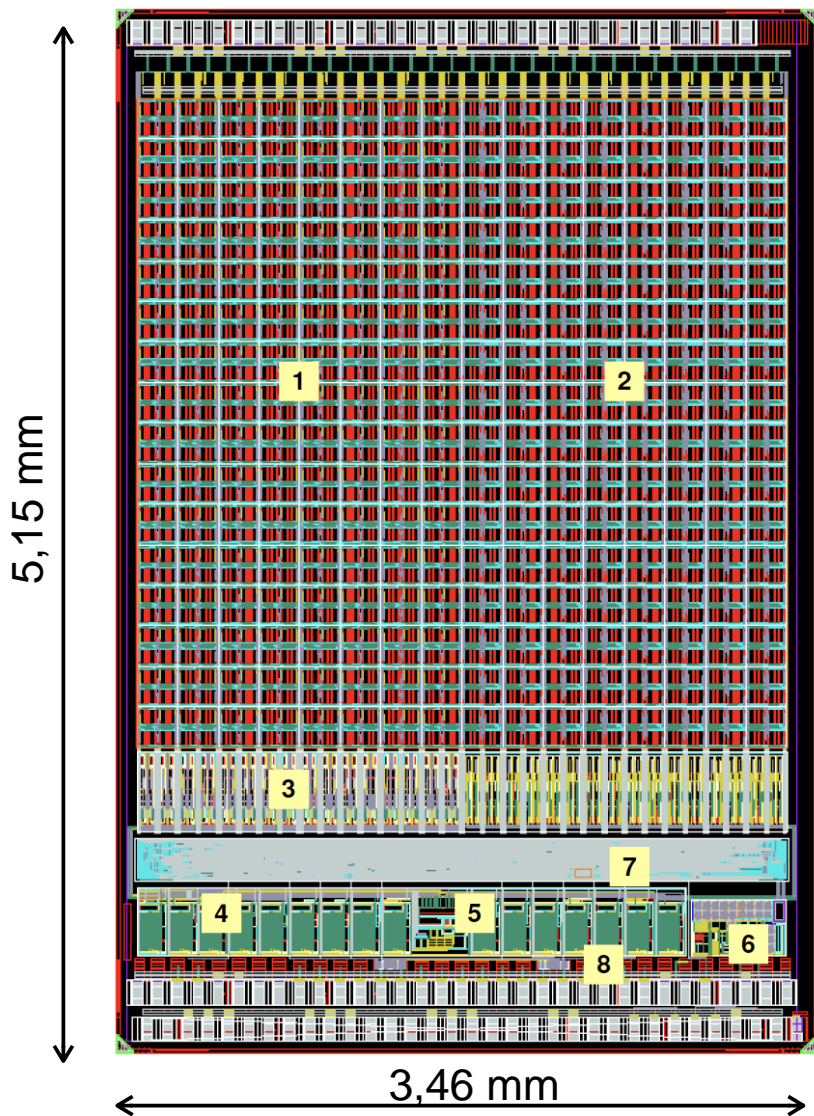
1) (32x64) pixels with Synchronous FE architecture

2) (32x64) pixels with Asynchronous FE architecture

3) replicated Bias Cells with current mirrors

4) 10-bit biasing DACs

5) Bandgap voltage reference

6) 12-bit monitoring ADC

7) readout/configuration digital block and High-speed Serializer at the chip periphery

8) SLVS transmitters/receivers and I/O cells

submitted: 5/7/2016
Arrived: 26/9/2016

5,15 mm

3,46 mm

Threshold and noise performance at 600 Mrad

- Synchronous and asynchronous front-end are both working fine, with good threshold dispersion and noise, even after exposure to 600 Mrad TID at - 20 °C

- Next: bump bonding to sensors (planar and 3D)
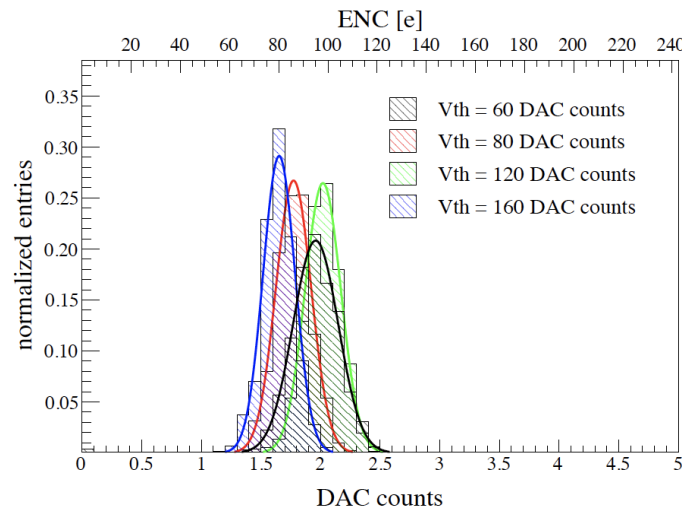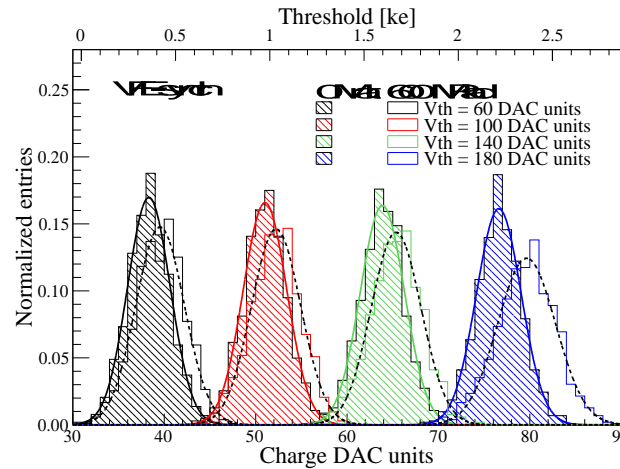
- Low threshold possible, **250-300e-** for bare chip
- The **auto-zeroing** is working well

- The measurements have been repeated after a TID = 600 Mrad has been reached with X-ray irradiation at -20°C with the chip in working conditions. **The irradiated chip is still fully operational**

- For thresholds below 1 ke-, which is the region of interest, the increase of the dispersion with radiation is below 10%
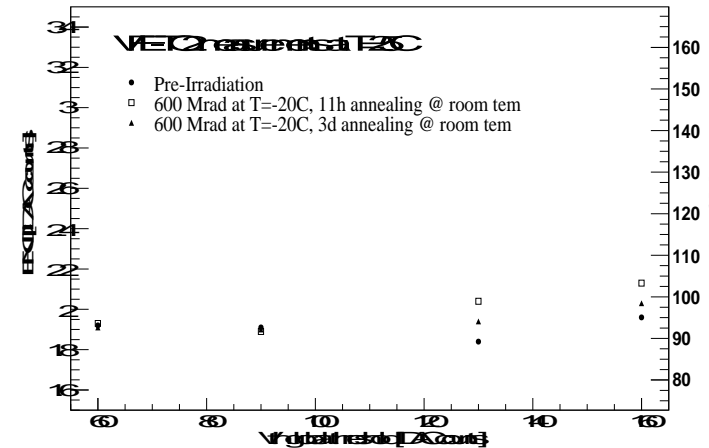
- ENC ~ 90e- : very low noise performance despite digital activities

Submission of large-scale 65 nm chip RD53A

- Full design review (with external experts) at CERN in December 2016.

- The review was successful: reviewer's recommendations provided useful guidelines towards the submission of the chip

- Submission is scheduled at the end of May 2017

RD53A - Large Scale prototype

- **The efforts of the RD53 collaboration are leading to the submission of the RD53A chip**

- **400 x 192 pixel, 50um x 50um pixel, 20mm x11.8mm chip**

- **Goal: demonstrate in a large format IC**

  - suitability of **65nm technology** (including radiation tolerance)

  - **high hit rate**: 3 GHz/cm^2

  - **trigger rate**: 1 MHz

  - **Low threshold operation** with chosen **isolation** strategy and **power distribution**

- **Not intended to be a production chip**

  - will contain design variations for testing purposes (with **3 different versions of the analog very front-end**)

  - wafer scale production will enable prototyping of bump bonding assembly with realistic sensors in new technology

- **Final design almost ready**

- **Submission: May 31, 2017**

CMS MPA

CMS SSA

24 mm

20.0 mm X 11.8 mm

Available for RD53 or other project

32 mm

Luigi Gaioni, INFN Pavia, Univ. Bergamo
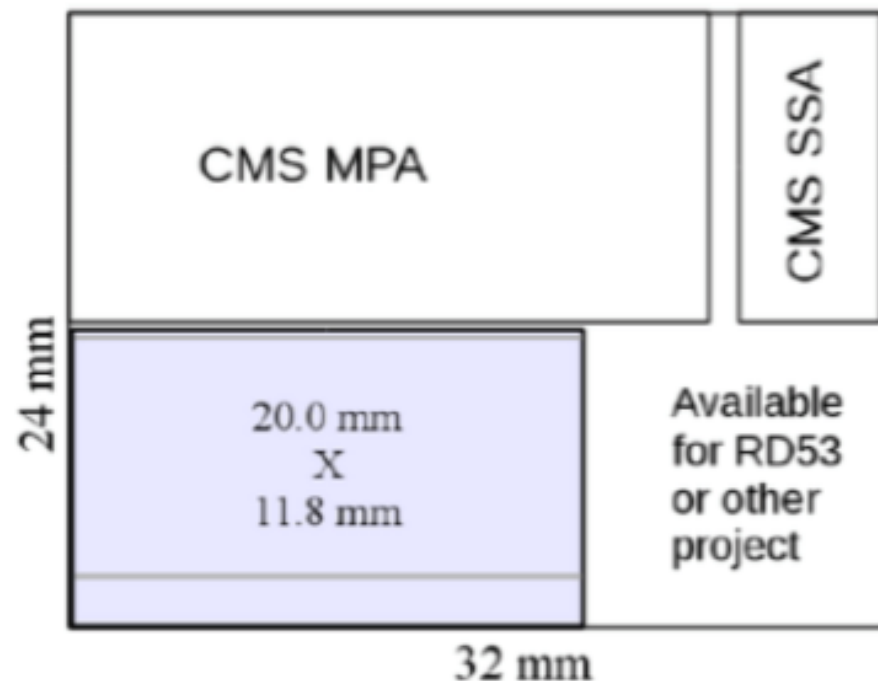
RD53A main specifications

From the Spec. document   http://cds.cern.ch/record/2113263

- **Hit rate:** up to 3 GHz/cm^2 (75 kHz pixel hit rate)
- **Detector capacitance**: < 100 fF (200 fF for the edge pixels)
- **Detector leakage**: 10 nA (20 nA for the edge pixels)
- **Trigger rate**: max 1 MHz
- **Trigger latency**: 12.5 us
- **Low threshold**: 600 e- → severe requirements on noise and dispersion
- **Min. in-time overdrive**: < 600e-
- **Noise occupancy**: < 10^{-6} (in a 25ns interval)
- **Hit loss @ max hit rate**: 1%
- **Radiation tolerance**: 500 Mrad @ -15° C
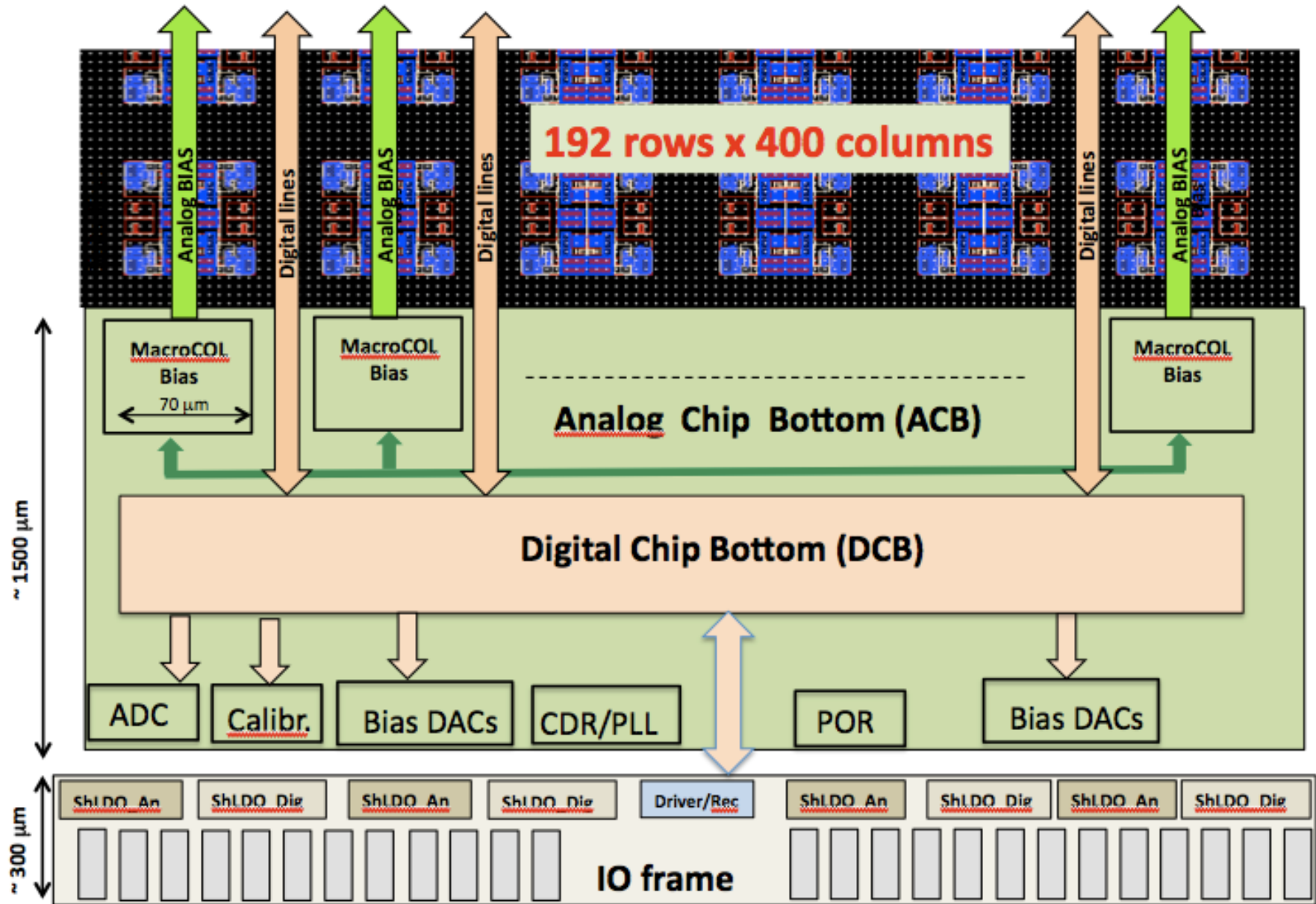
RD53A Pixel floorplan

- 50% Analog Front End (AFE) - 50% Digital cells

A "quad"

Digital logic

AFE

35   15
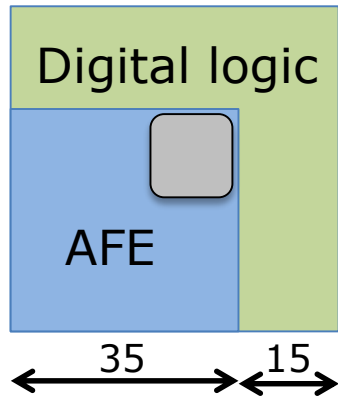
The "analog island"
concept
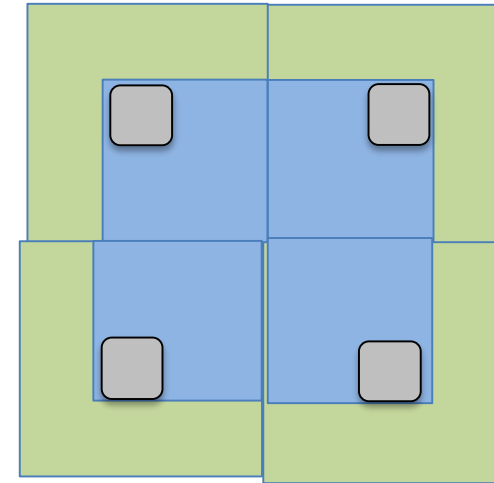
- The pixel matrix is built up of **8x8 pixel cores** → 16 analog islands (quads) embedded in a flat digital synthesized sea

- A pixel core can be simulated at transistor level with analog simulator

- All cores (for each FE flavour) are identical → Hierarchical verifications
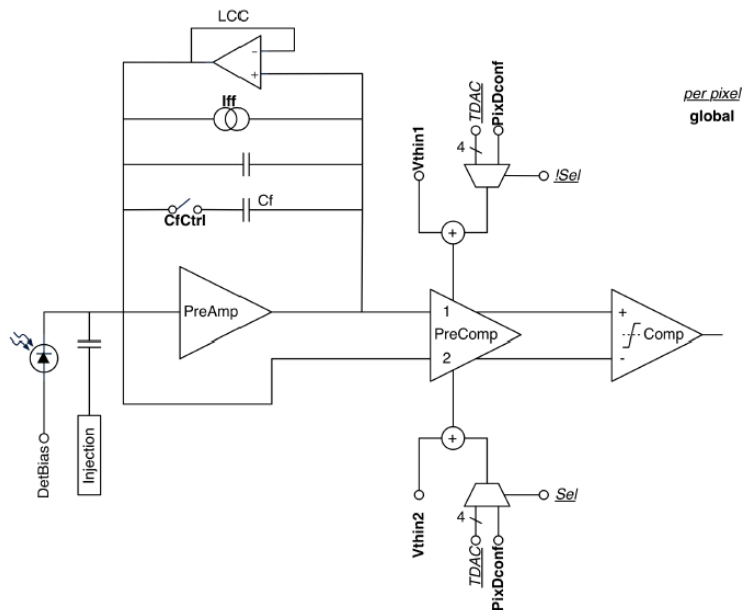
Analog front-ends

Synchronous AFE
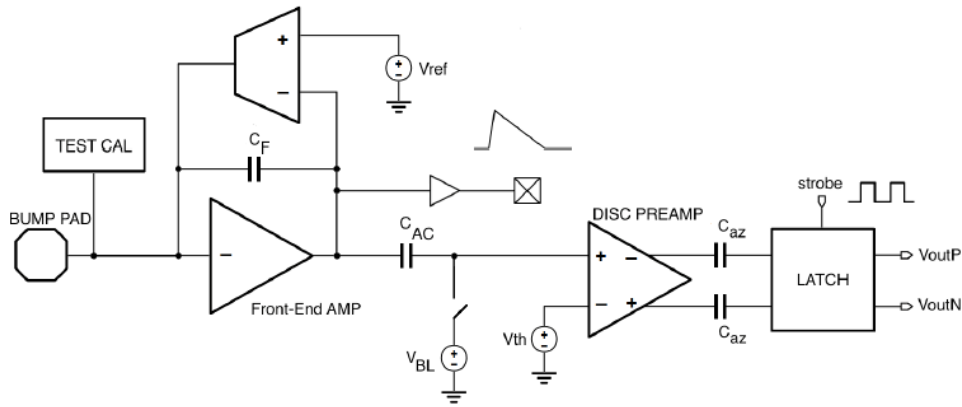
Linear AFE
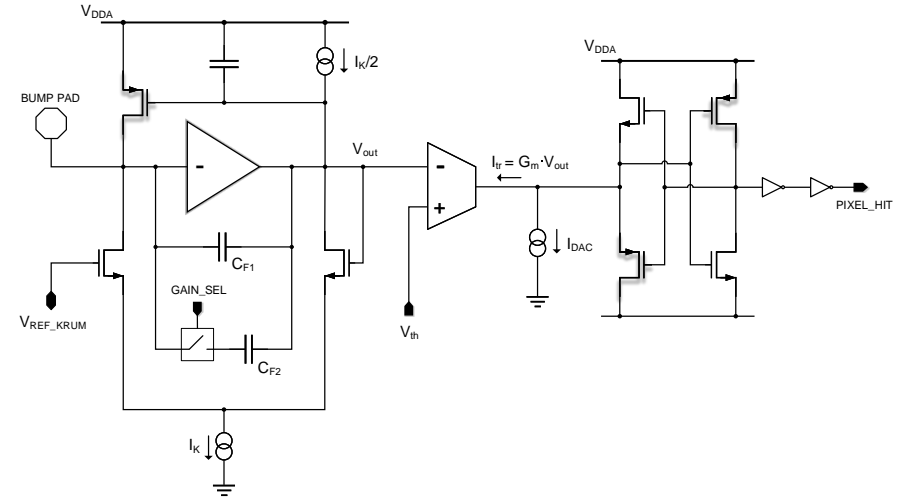
Differential AFE

- **3 different version** of the analog FE (AFE) will be integrated in RD53A

- Three **design reviews** (the last one in March 28, 2017) have been carried out for the AFEs.

- **Final verifications** of the AFEs on-going

Simulation and verification of the digital architecture

**Sara Marconi,
INFN Perugia**

- **Verification Environment** for **PIXel** chips (*VEPIX53*) for:

  - **Modularity**, **reusability** of same testbench:

    o different tests

    o multiple design stages

    o different designs/design blocks
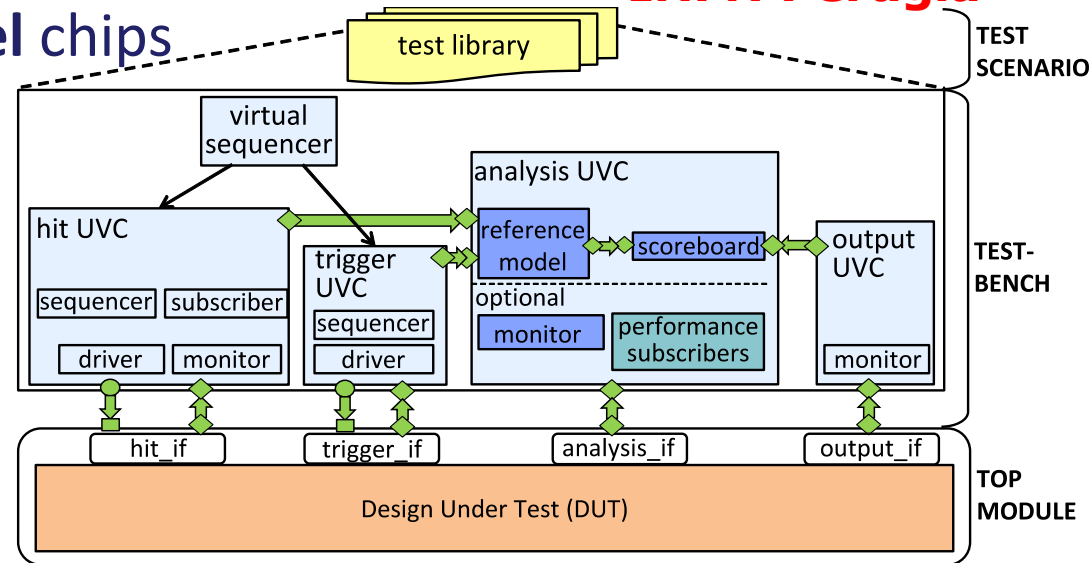
In this presentation, **focus on SEUs for the pixel array logic**

- Based on estimated cross-section ($5 \cdot 10^{-14}$ cm^2):

  - **protection** strategy is **needed for pixel configuration** latches

    o ~ 1% pixels already affected after 20s of operation

    → hardening by cell design, special latches (CPPM, Marsiglia) and/or re-freshing configuration

  - **finite state machine protection not required if capable of recovering automatically**

    o to be proven with simulations under operating conditions

  - no protection is needed for hit data during trigger latency

    o corruption probability during latency < 10^{-8}

Pixel array logic organization

- **Basic layout unit**: 8x8 digital Pixel Core → synthesized as one digital circuit
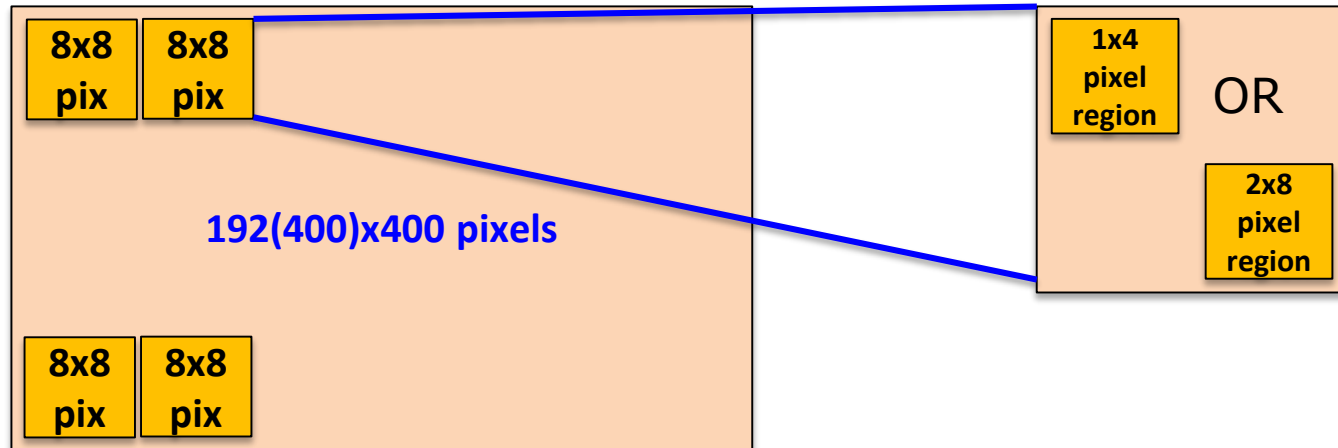
- One Pixel Core contains multiple Pixel Regions and some additional arbitration and clock logic

- Pixel Regions share most of logic and trigger latency buffering

Distributed Buffering Architecture (FE65_P2 based):
- distributed TOT storage

Centralized Buffering Architecture (CHIPIX65 based (4x4)):
- centralized TOT storage
- Integrated with Synch FE

Architecture optimization and comparison by means of the VEPIX53

- **1st architecture:** *distributed 1x4 pixel region*

  - Logic resources shared in PR composed of 1x4 pixels

  - Distributed buffering (i.e. hit storage) scheme

    o shared timestamp memory

    o distributed memory for charge information (4-bit ToT = Time Over Threshold)
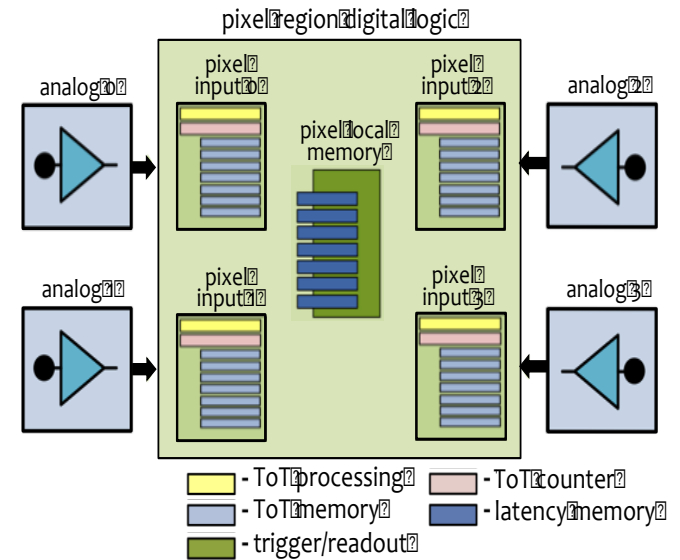
- **2nd architecture:** *centralized 2x8 pixel region*

  - Logic resources shared in PR composed of 2x8 pixels

  - Centralized buffering scheme

    o shared timestamp

    o shared ToT information

  - Data stored in buffer are reduced
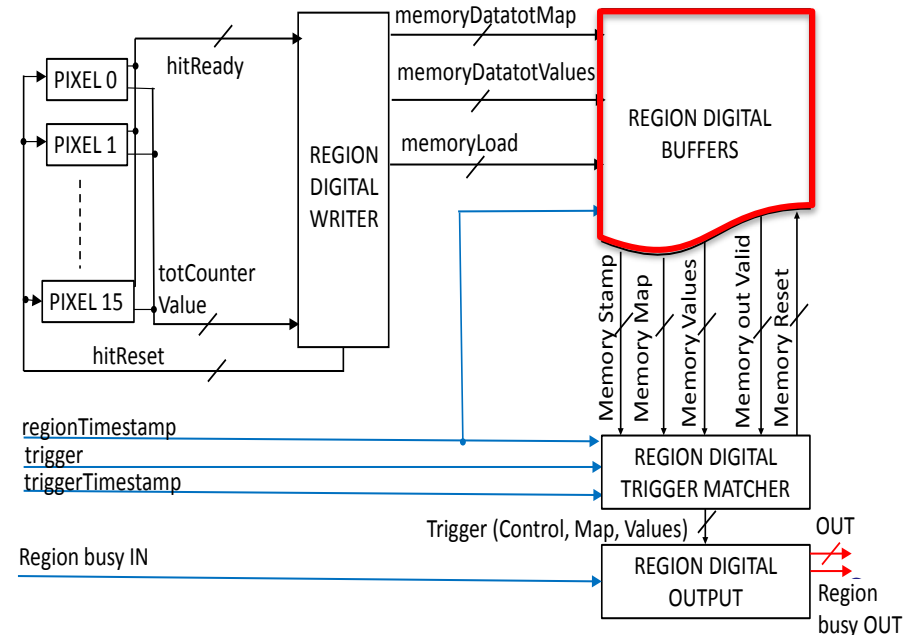
Submission status

- **Analog Front-ends:**

  - Synchronous & Linear AFEs: final version ready → integrated with CORE

  - Differential AFE: final version ready → integration with CORE on going

- **Analog Chip Bottom (ACB)**: assembly ready (RD53 IP blocks). Simulation with analog and mixed-signal simulator ongoing

- **Digital**: RTL ready, verifications on-going

- **Shunt-LDO**: 2A version of Shunt-LDO submitted on 19th Oct. 2016

  - Test of prototypes just started and looks promising

  - Irradiation campaign carried out

  - Simulation of full power system ShLDO-Bandgap-POR ongoing

  - Integration in IO Frame: almost done

- **IO Frame**: bottom PADs frame almost ready → 199 PADs with 100um pitch; passivation opening: 58um x 86 um; TSV Compatible. Top PAD frame (test and monitoring) assembly on-going.

WP4.3 : SiGe 130 nm

(CNRS-IPNL, CNRS-OMEGA, DESY, AGH-UST)

- Select best SiGe 130/180 nm process for high speed/high dynamic range ASIC design to upgrade current SiGe 350 nm AMS process MS22 M14

- Deliver SPIROC3 SiPM readout for calorimeter readout of WP14
- Deliver RPC high timing readout chip for WP13
- D4.2 M36 resp CNRS (OMEGA)

- Share expertise within SiGe HEP community

- Studies for LHC run 2, ILC…

SiGe processes evaluation

- 130 nm SiGe processes evaluated
  - Tower Jazz design kit not supplied
  - ST Micro 130 nm SiGe

- Evaluation on different test vehicles
  - ATLAS LAr upgrade
  - CMS HGCAL
  - ATLAS HGTD high speed timing
  - CMS muon RPCs high speed timing

- No significant improvement compared to regular CMOS
  - Better transconductance hindered by Rbb'

- Decision to choose TSMC 130 nm CMOS
  - Qualified by CERN for high radiation environment
  - Wider community (see examples next slides)

Ωmega

- Fabrication and test of 800 SPIROC2E and SKIROC2_CMS in SiGe 0,35
  - Will equip large scale prototypes of WP14

- Move to TSMC130nm for HL-LHC and AIDA2020

- 4 chips submitted in MPW 130nm (May&Dec 2016)
  - LAUROC : Liquid Argon Upgrade Read Out Chip (ATLAS)
  - HGCAL TV1 : Test Vehicle 1 for CMS HGCAL
  - ALTIROC : Atlas Lgad Timing ROC for ATLAS HGTD
  - HGCAL TV2 : test vehicle 2 for CMS HGCAL
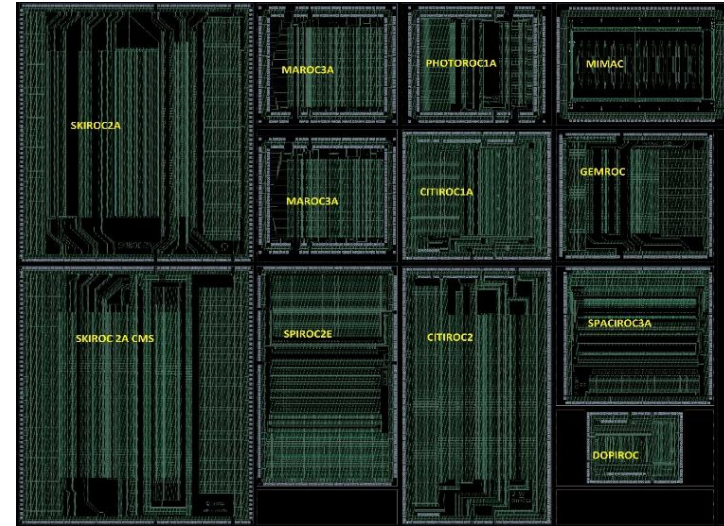
Nathalie Seguin-Moreau, OMEGA

Test Vehicle 1: TSMC130 nm

- Various PA, shapers, discris, no digital part
- Submitted in may 2016, received in august 2016
- Many measurements performed on the different configurations: good analog perf (noise, linearity)
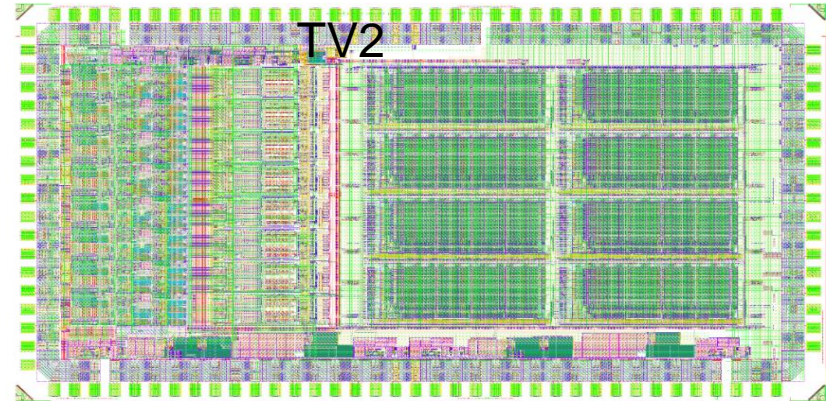
Test Vehicle 2: TSMC130nm

- TV2 groups 8*analog channels + ADC + 32x512 RAM (CERN)
- TV2 submitted in December 2016 (HGCAL milestone) and received at the end of March 2017. Tests should begin in May 2017

HGROCv1: TSMC130nm, under design, submission next June

- 32 channel ASIC
- Complete channel (analog+digital): FE+TOT/TOA+ TDC+RAM+ serialiser, transmiitter …
- Partners: Saclay (TDC for TOA), CERN, Imperial College (TDC for TOT) ….
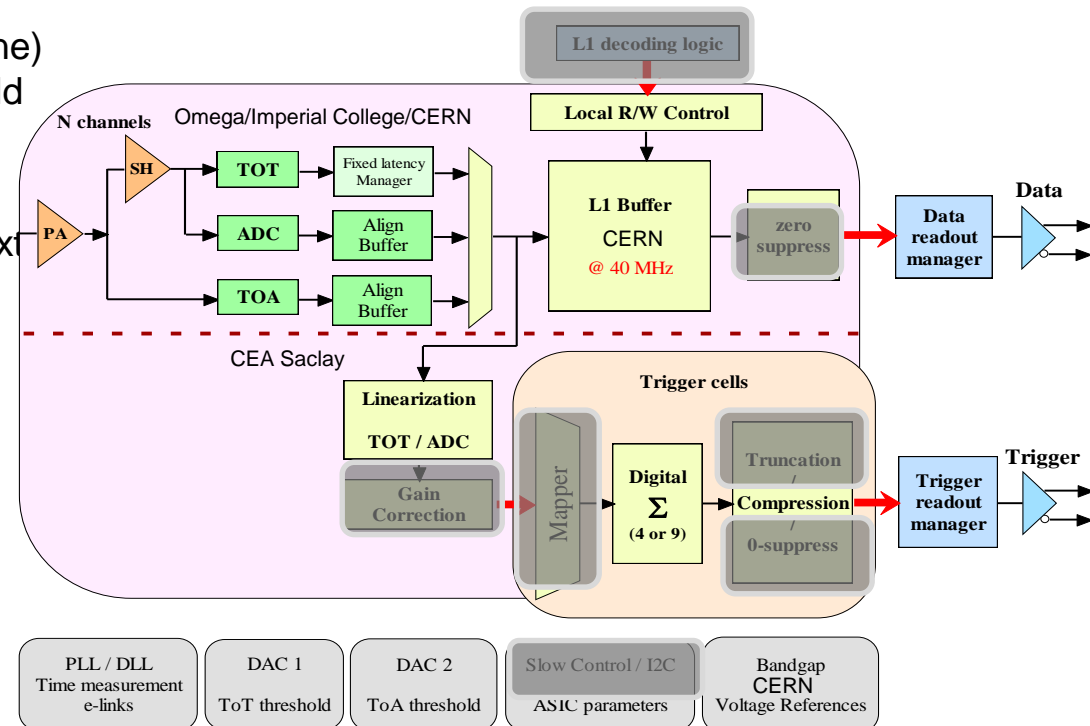
- LAUROC (TSMC 130nm) is a new innovative line-terminating preamp (25 or 50 Ω) featuring "electronically cooled" resistance (<10 Ω)

- 8 analog channels (Preamps mainly): Submitted in May 2016, received in August 2016

- Good testbench performance (input impedance and linearity)

- But excessive noise compared to simulations
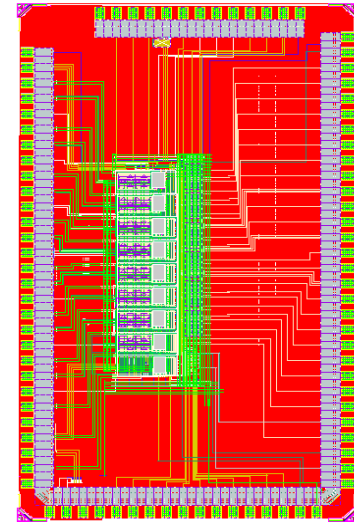
Linearity : High and low gain

High gain (0-1-mA)

Low gain (1-10 mA)

±0.5%
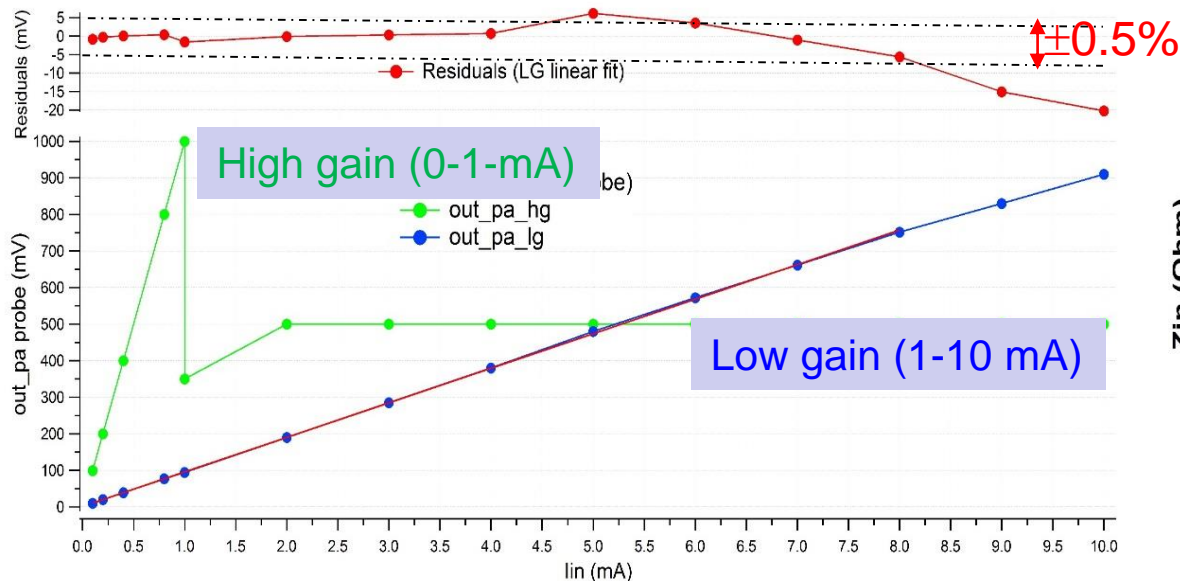
Zin vs Input current
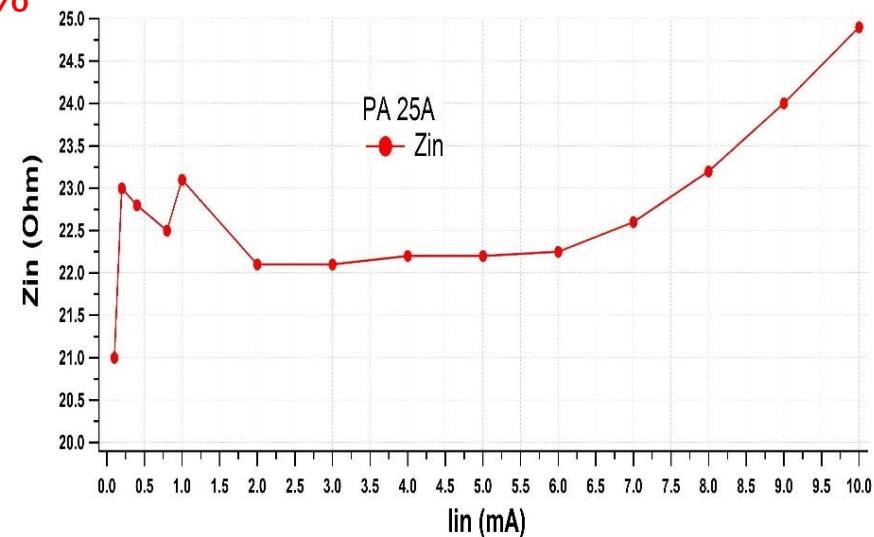
- ALTIROC = ATLAS LGAD Timing ROC
  - Submission of a chip (TSMC130 nm) in December 2016 (MPW CERN/IMEC), received at the end of March 2017
  - 20 ps timing measurement with LGAD sensors for ATLAS HGTD
  - Test chip bondable to sensors of 1x1 mm² and 2x2 mm²
  - Integrates 8 channels with High speed preamp (1 GHz) + TOT + Constant Fraction Discriminator (20 ps)
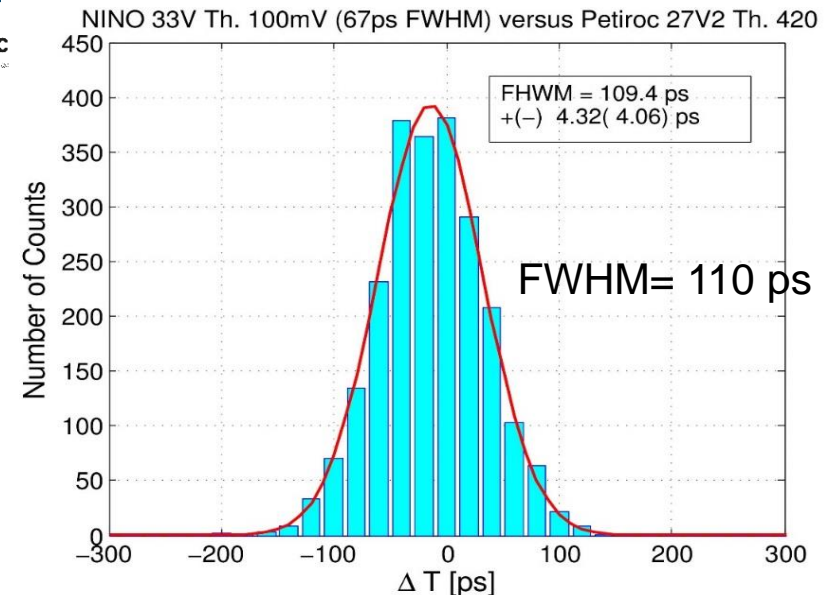 - Tests should start in May 2017
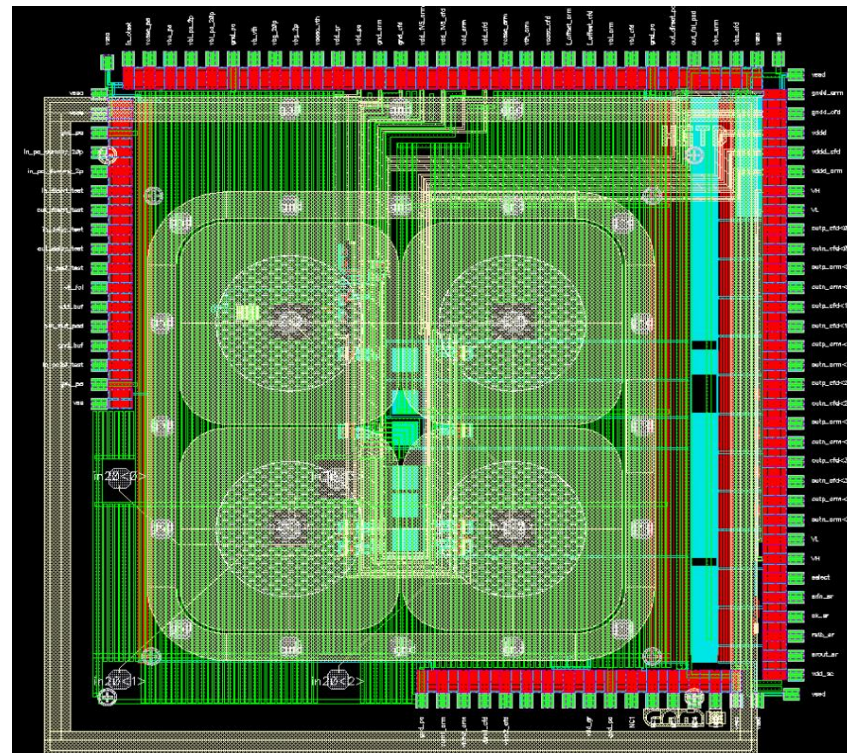
- Will evolve to 400 ch chip
  - With internal TDC (Collaboration with SLAC)
  - Bump bonded to sensor

Ωmega
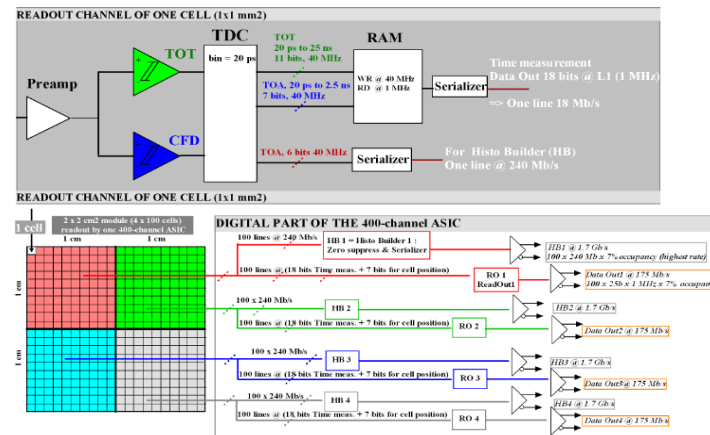
- PETIROC2A features high speed time and charge measurement (AMS 0,35µm SiGe)
  - 32 channels braodband amplifiers+discriminators
  - G = 25 BW = 0.9 GHz GBW = 20 GHz
  - Minimum Threshold <1 mV
  - Low power : 6 mW/ch
  - 10 ps jitter in analog operation (external TDC)
 - 50 – 90 ps with internal TDC (synchronous/asynchronous)
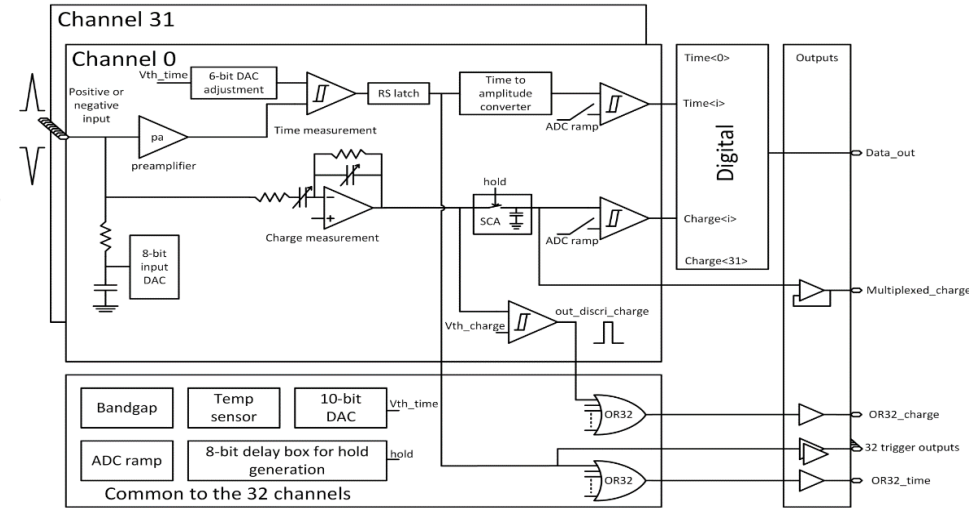
- Submission of PETIROC3 in TSMC 130 nm in 2017
  - High speed preamp + discriminator
  - TDC from IPNL Lyon
  - Milestone for AIDA 2020 project WP13

weeroc

NINO 33V Th. 100mV (67ps FWHM) versus Petiroc 27V2 Th. 420

FHWM = 109.4 ps +(−) 4.32(4.06) ps

FWHM= 110 ps

Number of Counts

Δ T [ps]

© S. Gundacker (CERN)

A High Precision TDC for CMS MG-RPC : Vernier Ring Oscillator based TDC CRONOTIC (Cms Rpc muON detectOr Tdc IC)

Electronics for Multi-Gap CMS-GRPC Detectors

- PETIROC ASIC : 32-channel, high bandwidth preamp (GBWP> 10 GHz), <3 mW/ch, dual time and charge measurement (160 fC-400 pC) vey fast and low-jitter < 25 ps rms
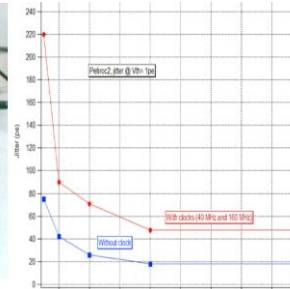

**Hervé Mathez, IPNL Lyon**

Requirements for the TDC ASIC development

- LSB < 20 ps, adjustable

- RMS Resolution < 2 ps, including all noise types other than the quantization noise

- Dead time < 1µs

- The RPC output signal frequency is ~1 kHz (ie. the real dynamic range ~1 ms)

- The TDC dynamic range measurement : from 1 ns to 3 ns depending on :

  - Gate unity rms Jitter , TDC reference clock frequency and the frequency of the Ring Oscillators

  - Low power consumption (the total power (FEE+TDC) < 3 mW/channel)

TDC ASIC for fast timing with RPC multigap detectors, processing signals from the PETIROC chip

Global Floor Plan of the TDC
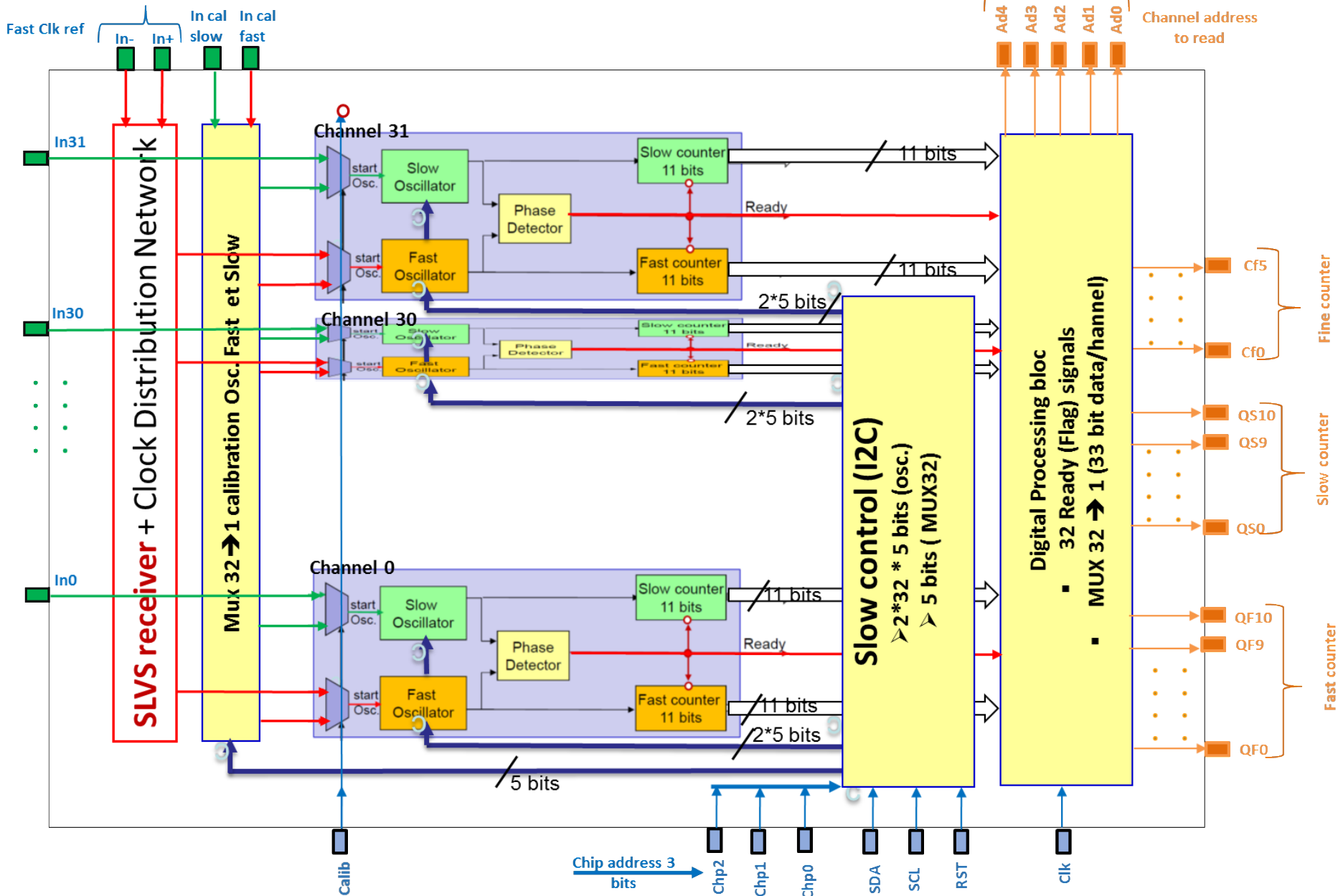
Layout of the submitted ASIC : CRONOTIC
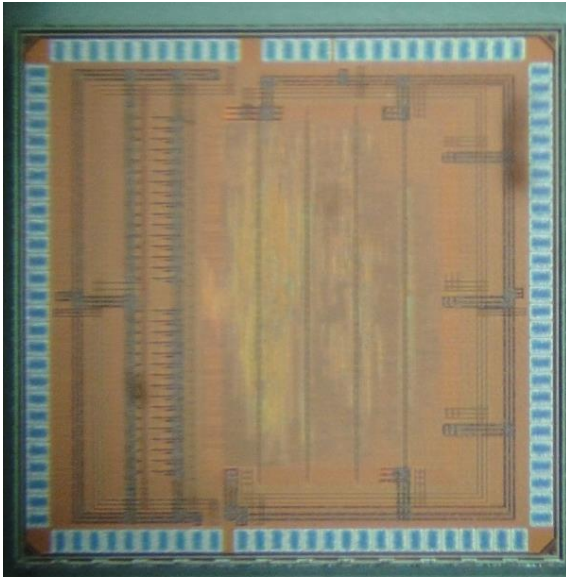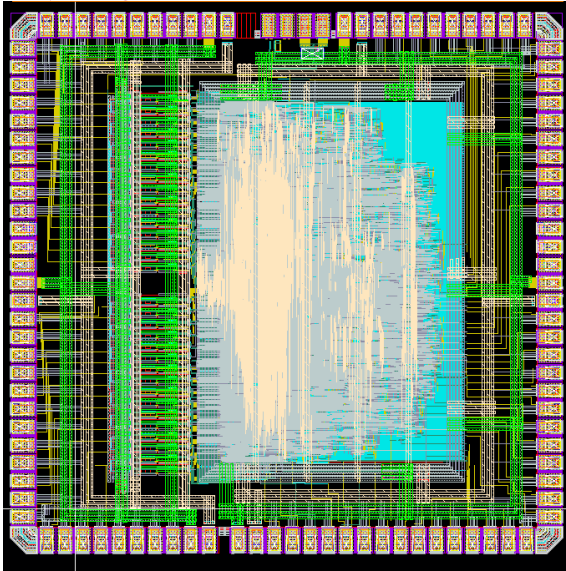
Credit : M. Dahoumane

- TSMC 130 nm process

- Triple-voting rad-hard digital

- Dimensions :

  - 2,400 x 2,450 mm^2

- Submitted Nov 2nd 2016

- ASIC returned from fab by end of January

- Packaging is done (CQFP 128)

- Test board must be designed, it started by beginning of March

Developments in TSMC 130 nm

In last years we have developed for ILC/CLIC – FLAME ASIC and for LHCb – SALT ASIC many blocks:

- Ultra-low power SAR ADCs: 6-bit (up to 100MSps), 10-bit (up to 50MSps), 12-bit (not tested yet)
- PLLs (for clk generation), multi-phase PLL (for serialization), DLLs (for sampling time setting)
- SLVS I/O, SST driver
- Bandgap and temperature sensor
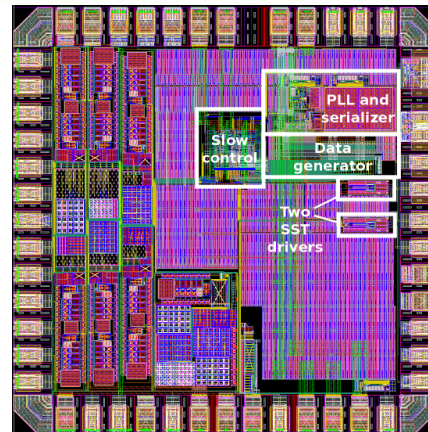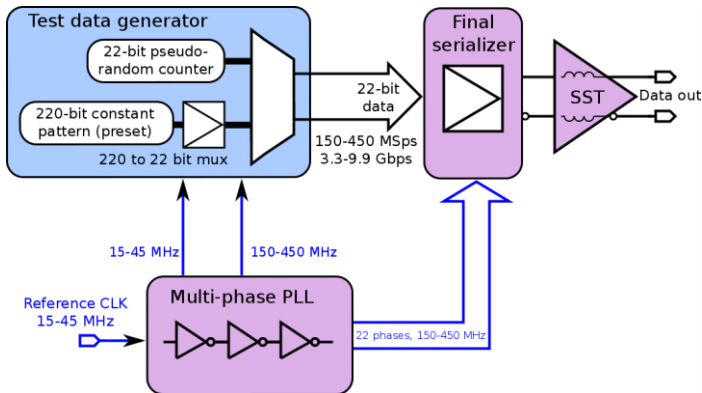- DACs, opamps, etc...

**Marek Idzik,
AGH Krakow**

FLAME readout for ILC in CMOS 130 nm
8-channel FLAME ver.0 prototype

Prototype FLAME channel

FE&ADC < 2mW
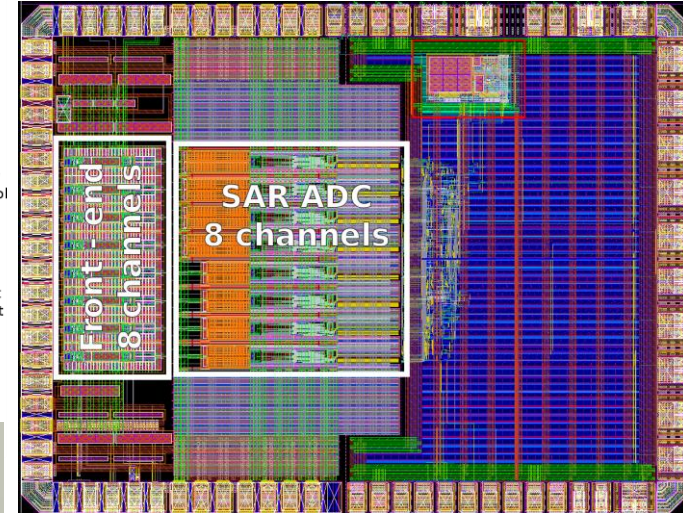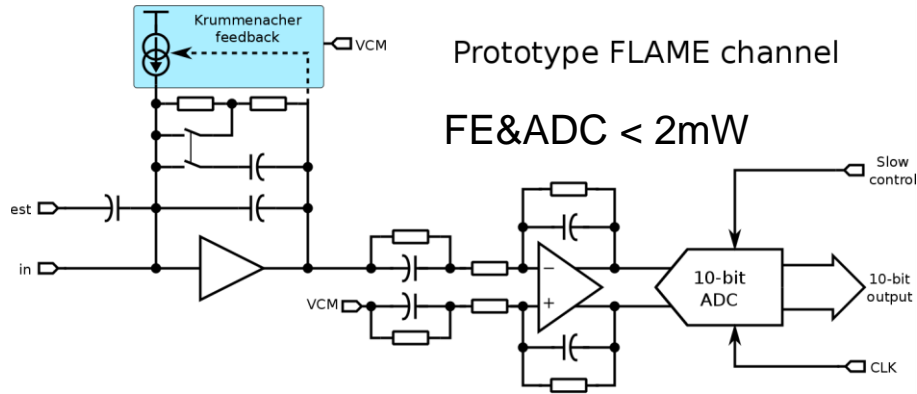
2600 μm x 2000 μm

High Speed Serializer&Transmitter prototype in TSMC CMOS 130nm

1250 μm x 1250 μm

FLAME serializer prototype:
- Ultra low power, low jitter multi-phase PLL
- 22b → 1b serializer with fast SST driver (3.3 – 9.9 Gbps)

Eye diagram at 5Gbps

Task 4.4 Interconnections and TSVs

(CERN, INFN-GE, INFN-PV, INFN-PG, CNRS-CPPM, CNRS-LAL, MPG-MPP, UBONN, UNIGLA)

- Produce through-silicon vias on wafers from Task 4.2
- Connect chips with TSVs to detectors from WP7
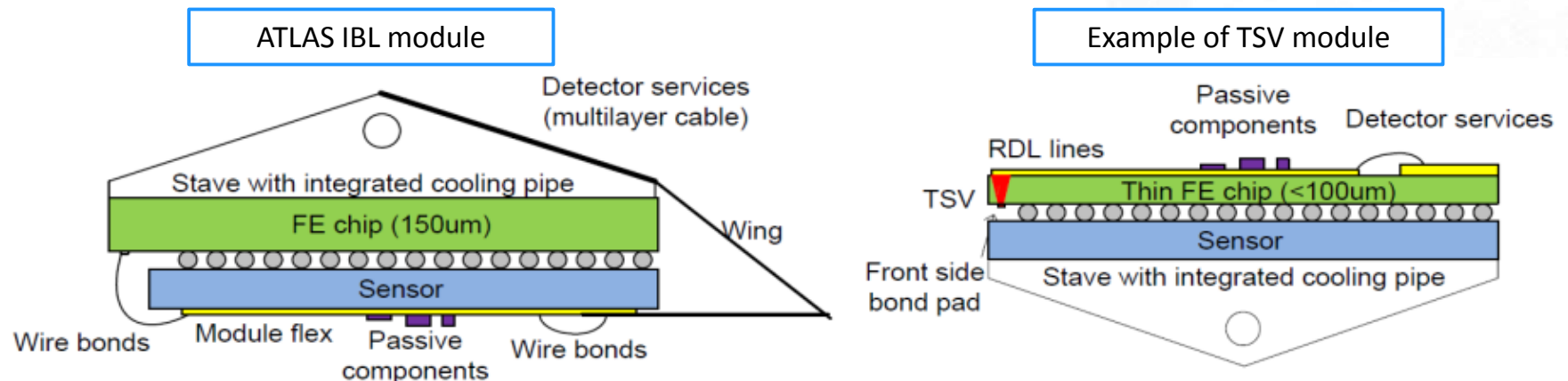- Test radiation hardness of interconnections

Candidate processes for TSV

WP4 groups are currently working with two different technology providers for Through-Silicon Vias in 130 nm CMOS FE-I4 pixel readout chips:

- IZM (via last tapered TSVs) **(Bonn)**

- CEA-LETI (via last TSVs + RDL + direct wafer-to-wafer bonding) **(Glasgow)**

Results are available. Plans are to extend this study to 65 nm CMOS wafers from the RD53 engineering run.

- Modules with TSV can be used for the outermost detector layers at the HL-LHC to provide full detector coverage over the large area

ATLAS IBL module

Detector services (multilayer cable)
Stave with integrated cooling pipe
FE chip (150um)
Sensor
Wing
Wire bonds   Module flex   Passive components   Wire bonds

Example of TSV module

Passive components   Detector services
RDL lines
TSV   Thin FE chip (<100um)
Sensor
Front side bond pad   Stave with integrated cooling pipe

Goals of TSV processing

- Test processes for peripheral TSVs on the 130 nm FEI4 chip, and apply them to the 65 nm RD53A chip
  - Allow for 4 side buttable modules
  - Enable wafer-to-wafer assembly
  - Remove wirebonds for greater module robustness

- The RD53A chip will be designed so that it is "TSV enabled" (i.e., compliant with TSV design rules); this involves the peripheral bonding pad regions

- **MS4.7 Selection of TSV process M14 (June 2016) was accomplished: both processes (IZM and CEA-LETI) were selected for the following stages of WP4**

TSVs and RDLs with ATLAS FEI4 FE chips: CEA-LETI process

- Project started with CEA Leti on TSV-last process in FE-I4 chips
  - Connect chip M1 metal layer from front to back of chip via TSVs
- Front side processing with either UBM only or bumps
  - UBM only → solder on sensors
  - Bumps → UBM on sensor

Richard Bates, Glasgow

- Back side processing RDL
  - Specific FE-i4 layout for laser soldering, same specs as Medipix
  - Pad layout to compensate thermal stressed during re-flow after flip-chip (demonstrated to work in previous project between Glasgow and LETI)
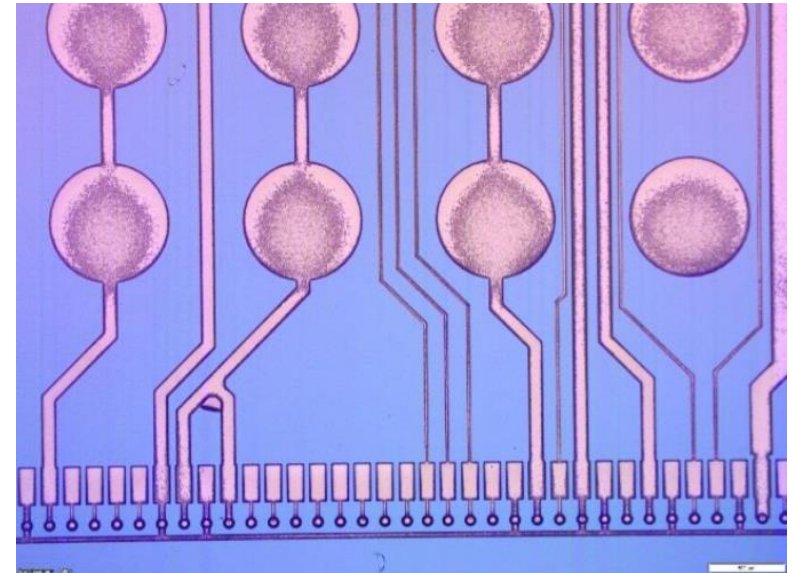
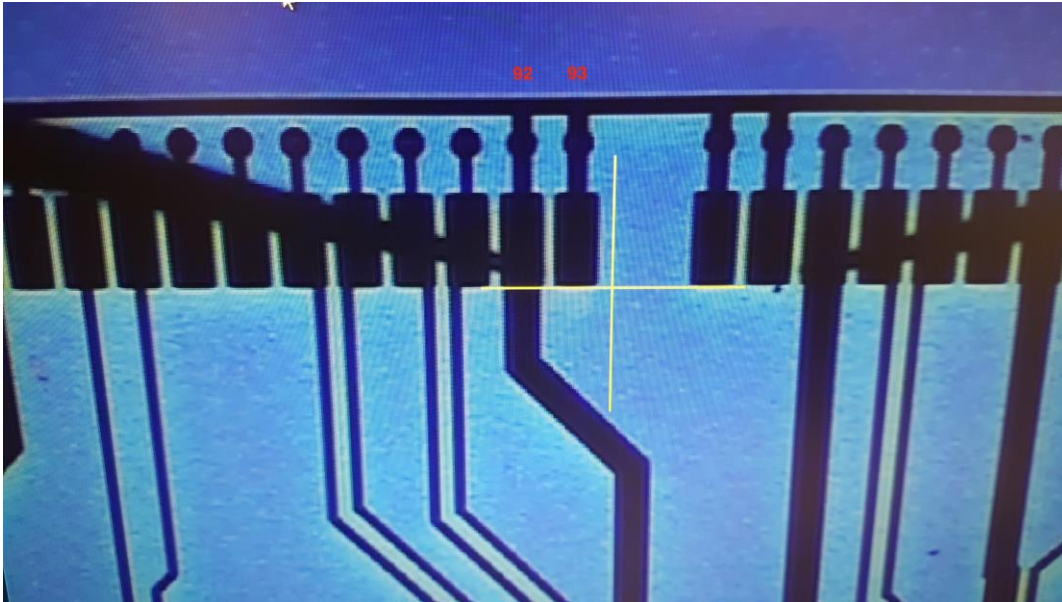# TSV etched through silicon down to M1

60 μm
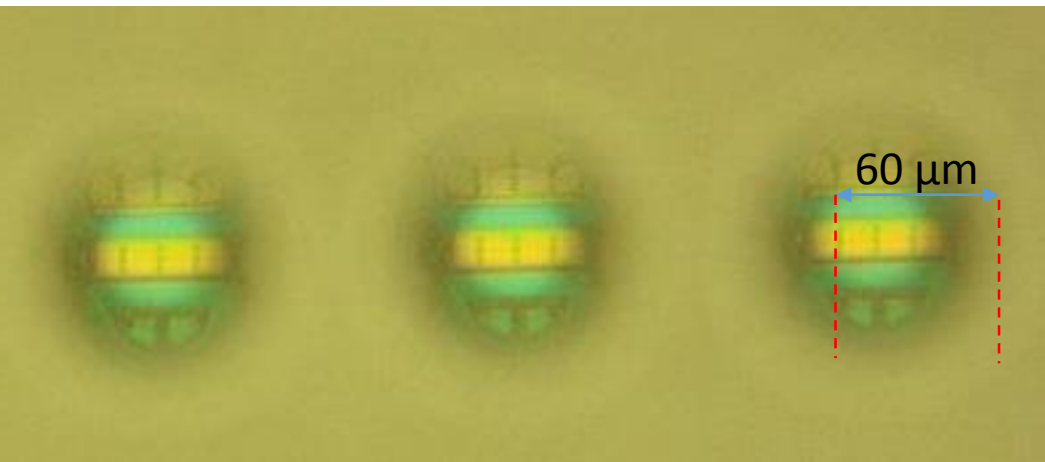
- TSV lined using full wafer Silicon Oxide & Silicon Nitride deposition
- Etch back full wafer to open the oxide/nitride on the bottom of the TSV
- Damascene process to fill with copper

RDL processing

- Excessive copper applied
  - Aim was to reduce TSV resistance
  - 6-8 μm requested c.f. standard thickness < 5 μm
- Caused delamination of large RDL laser solder pads
  - Pulling away underlying oxide layer as well
  - 1 of the 3 wafers not so bad and useable for module building
- TSV contact on front side metal :

low and repeatable contact between 2 ground TSVs

  - 6 Ohm including RDL line and probe resistance

- Wafer level testing started Jan 2017
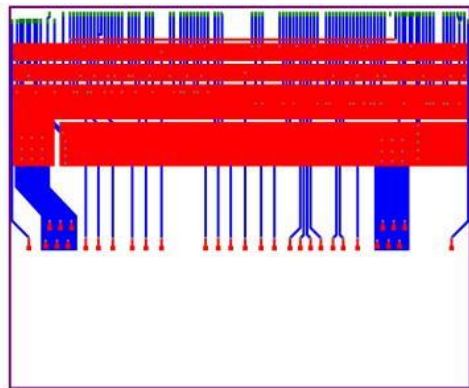
- Soon realised that there was an RDL error

- VDDD line connected to GND bus
  - Error during translation of RDL design to wafer design software
  - Chip not testable
- Probed all power lines and currents reasonable
  - TSVs connected to M1 and isolated from wafer
- Wafers retuned to LETI for FIB
  - Only central die edited due to FIB reach
  - Error corrected
  - Tested on probe – no shorts!

Second run of wafers being processed at CEA LETI
- Front side with Solder bumps
- Front side processing finished
- Bumps inspected and appear perfect
- Ready for transfer to support wafer for backside processing
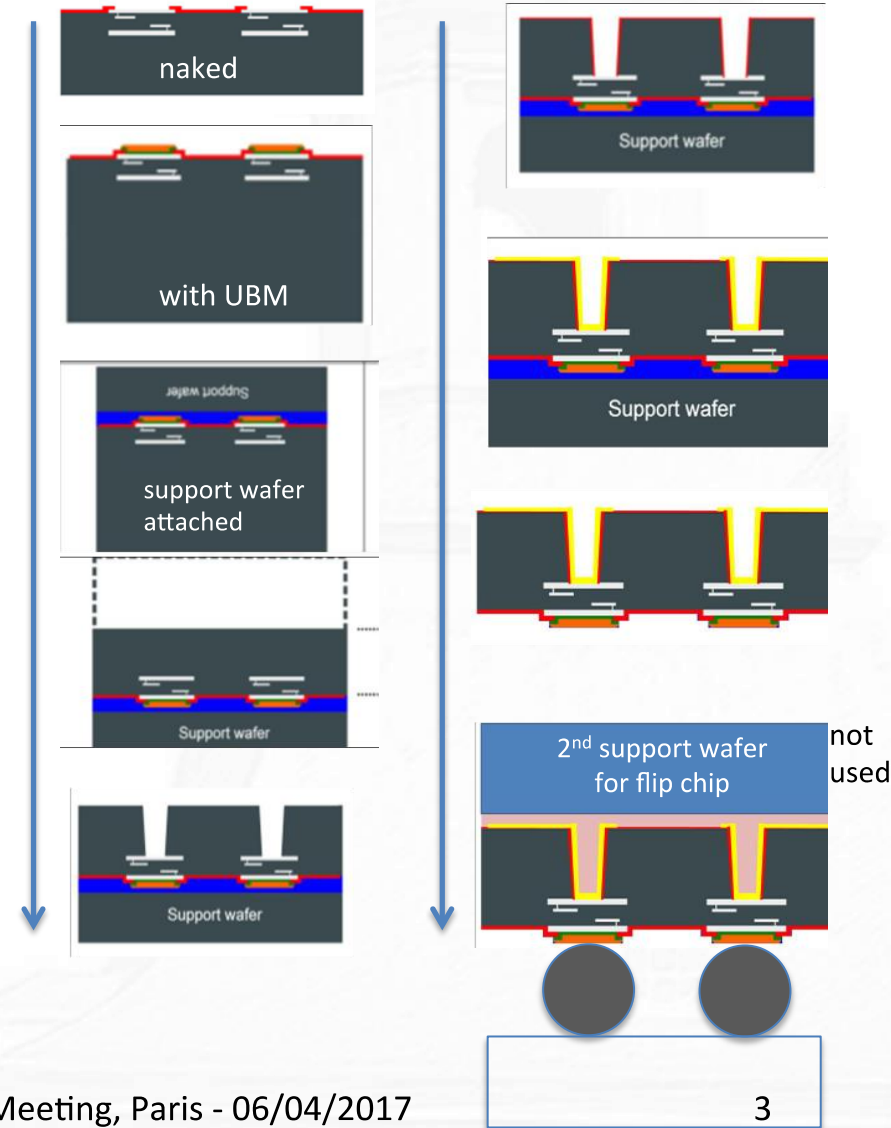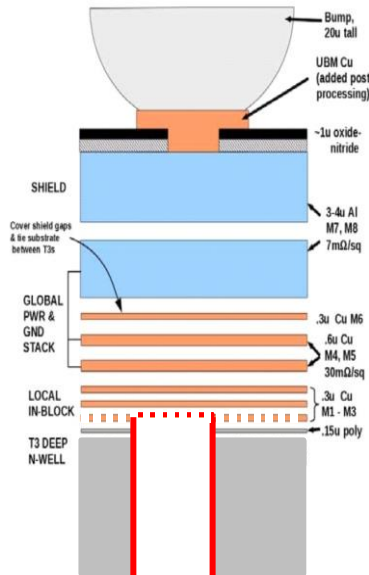
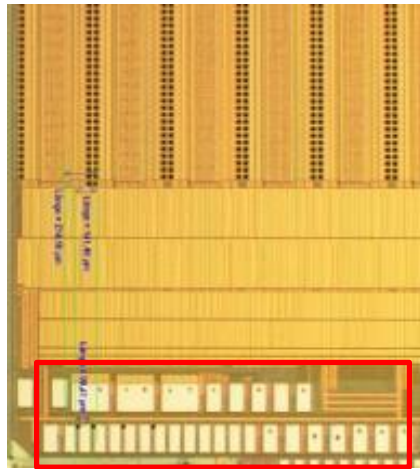# TSV modules using FE-I4 (ATLAS IBL chip): 160µm thick, 2 x 2 cm²

- use straight vias with aspect **raKo 3.5 : 1**

Goal: demonstration of **TSV/RDL processing together with solder bump bonding method** on 8" FE-I4 wafers thinned to 160µm (3 wafer pilot run)
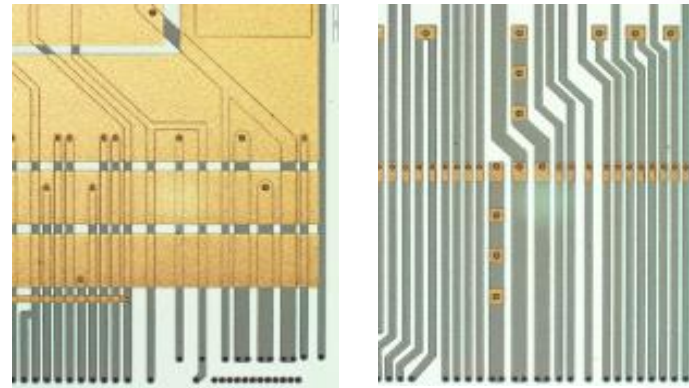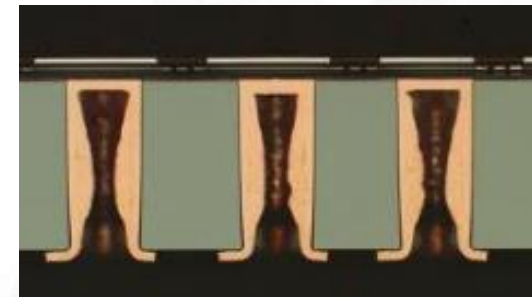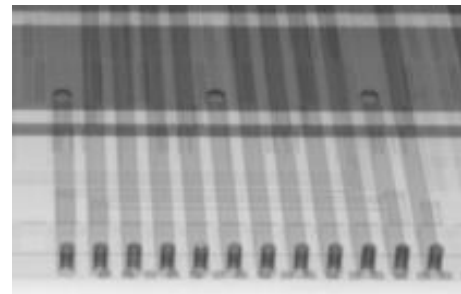

2-layer RDL

naked

with UBM

support wafer attached

Support wafer

Support wafer

Support wafer

2nd support wafer for flip chip

not used

ATLAS FE-I4 TSV Run: Status

Two designs of Backside RDL and pad metallisation

- Wire bond pad area for TSV contact

- Via from backside

- Liner filled TSV

ATLAS FE-I4B with Cu-filled TSV (x-ray and cross section)

- UBM on ATLAS FE-I4 wafer
- TSV formation on ATLAS FE-I4 wafer
- Functional test of ATLAS TSV chips
- Samples for module assembly available?
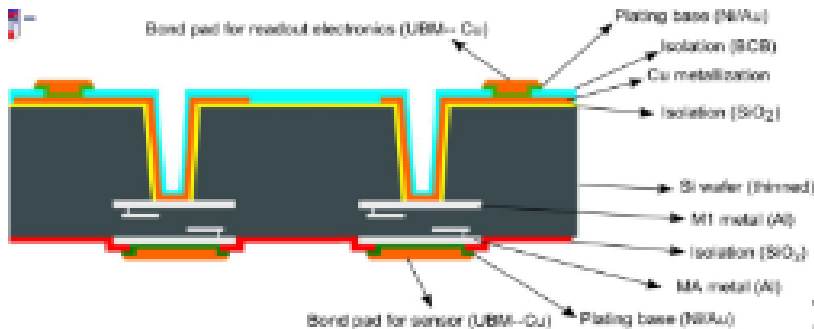
TSV schematical cross section

All pictures courtesy of Fraunhofer IZM, Berlin.

## TSV modules using FE-I4 (ATLAS IBL chip): **160µm** thick, **2 x 2 cm²**

- use straight vias with aspect ratio **3.5 : 1**

Cu-RDL lines

Visual inspecKon:

- good round RDL layer edges (Cu and NiAu) and clear cut vias
- X-ray image shows good metal coverage over full TSV depth

Cu-filled TSVs

Electrical tests:

- yield needs improvement
- aspect ratio still challenging

TSVs

Yield of vias on 18 FE

vias ≤ 1 Ω: 49 %
mean R : 0.50 ±0.01 Ω

number of vias
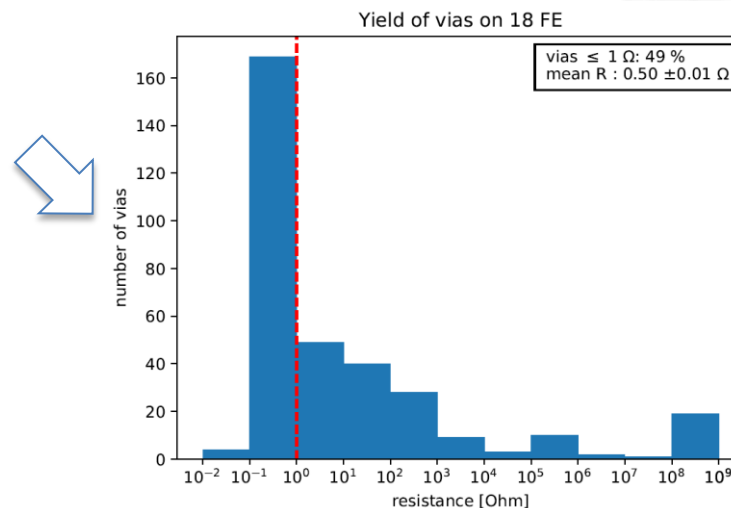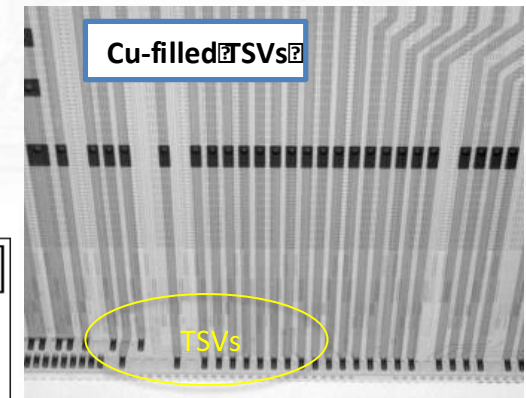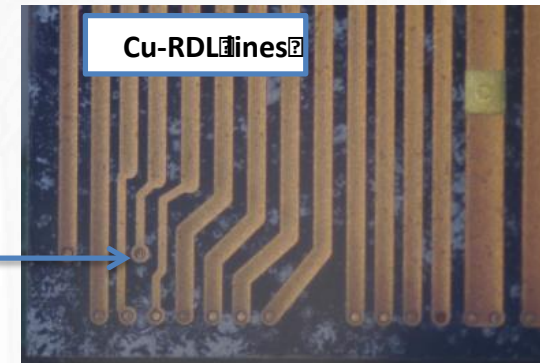
resistance [Ohm]

TSV Resistance measured on 18 FE chips

- Mean via resistance measured on FE-chips:
  - 18 modules tested
  - No correlation with TSV position on chip
  - All modules similar
- Mainly 2 effects caused the failures:
  - Insufficient copper plating due to rework
    - faulty sputtering of seed layer
    - no copper at via bottom
  - Incomplete Via etching
    - controlled optical
    - layer M1 is meshed
    - passivation layer beneath M1 needs to be etched through completely

Local distribution of via resistance on 18 FE

Postion on chip [mm]
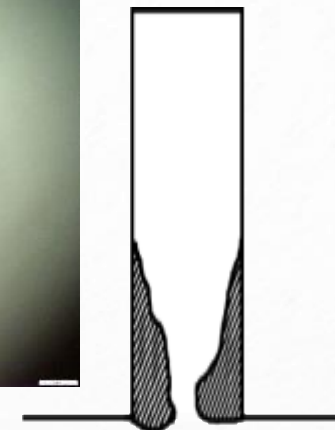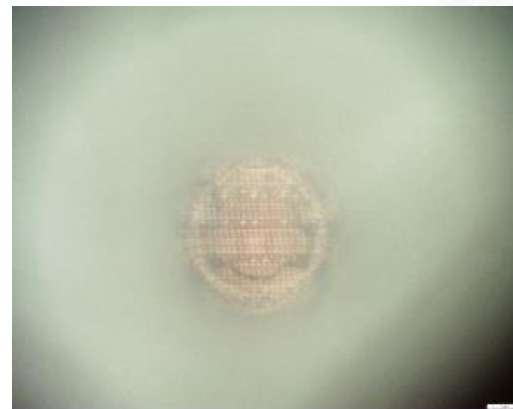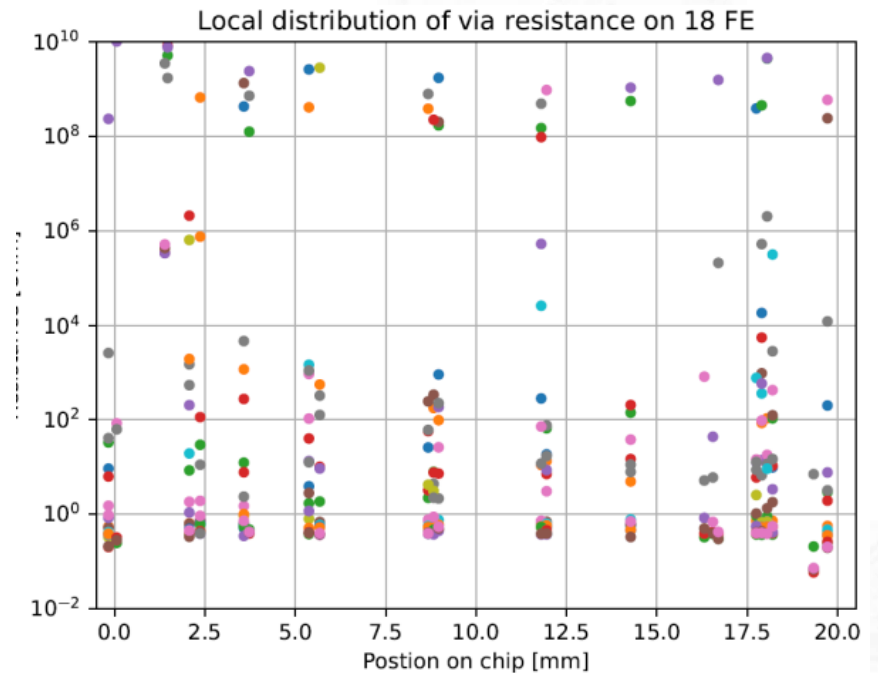
- ■ **Goal:** establish high yield TSV + RDL process for pixel modules
  - ■ straight vias through (ultra?) thinned FE-I4 wafers and chips: note **2x2 cm² chip size**
  - ■ **80 – 120 µm** thickness (to be optimized),
  - ■ aspect ratio = 2 : 1
  - ■ one handle wafer step needed
  - ■ complete development including flip-chipping process for the final pixel module

Challenges of the project

- ■ reliable TSV fabrication ... yield hoped/expected to be <u>much</u> better than for project 2
- ■ thin (o(100 µm)) wafers are <u>needed</u> for the goal of "large yield"
  challenge is the handling of large and very thin wafers/chips
- ■ surprises during flip-chipping can also be an issue

- – Long term plan: Move on with 65nm CMOS wafers from RD53
  - • check feasibility → high capacity/inductivity of TSV could have impact on high speed links

TSV compatible design of RD53A

Bonding pads in RD53A are compatible with TSV fabricated with a backside etching process .These pads have all metal layers from M3 to the actual aluminum pad. M1 and M2 were removed to reduce parasitic capacitance and optimize the performance of high-speed drivers.

This structure was checked by IZM and they think it is OK. No problems are foreseen for the CEA-LETI process as well.

Bump, 20u tall

UBM Cu (added post processing)

~2u oxide-nitride

SHIELD

4u Al M8 7mΩ/sq

Cover shield gaps & tie substrate between T3s

4u oxide

3u Cu M7 6mΩ/sq

GLOBAL PWR & GND STACK

4u oxide

.5u Al M6

1.5u oxide

.6u Cu M4, M5 30mΩ/sq .7u oxide

LOCAL IN-BLOCK

.3u Cu M1 – M3 .4u oxide

T3 DEEP N-WELL

.15u poly
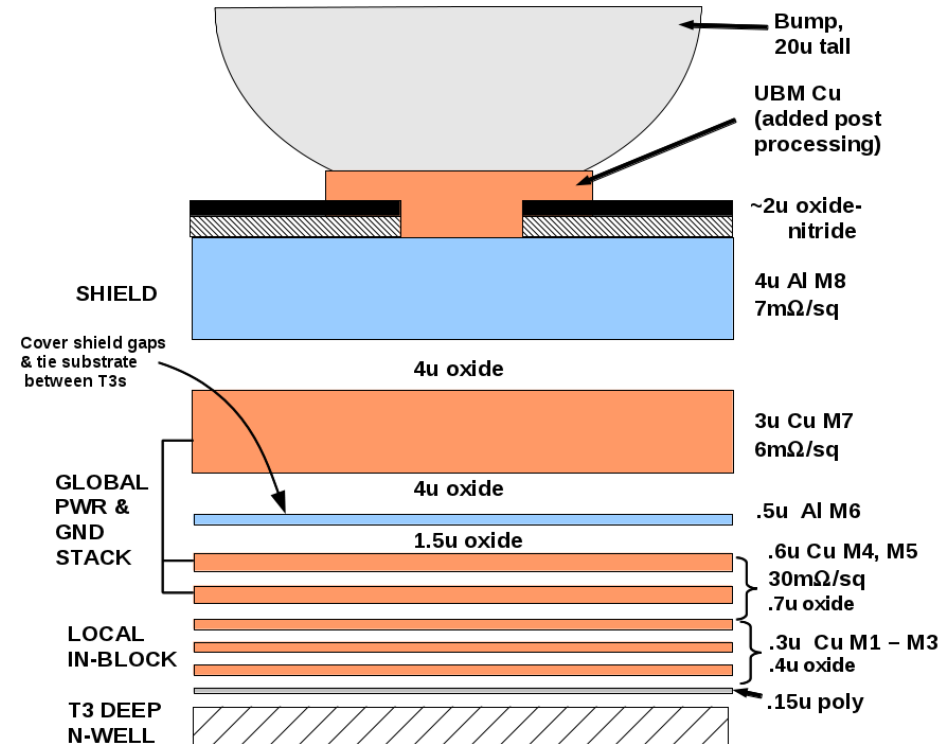
WP4 outlook

- WP4 appears to be on track with respect to the 2017 milestones (MS4.8: TSV design review in 65 nm chip; possible delay will depend on how we define the meaning of this milestone)

- Pixel readout chip prototypes in 65 nm CMOS are available for testing sensors from WP7

- Thanks to synergies with RD53 (65 nm CMOS engineering run), also longer term schedule looks reasonable

AIDA WP4 deliverables

- D4.1 CMOS 65 nm engineering run *(availability of the run with the "ATLAS/CMS" and CLICPIX pixel chips)*   (CERN)

    M36 (April 30, 2018)

- D4.2 BICMOS SiGe engineering run *(availability of run with SiPM calorimeter-WP14 and gas detectors-WP13 chips)* (CNRS)

    M36 (April 30, 2018)

- D4.3 Through Silicon Vias production *(fabrication of TSV in wafers of deliverable 4.1)* (INFN)

    M42 (October 31, 2018)