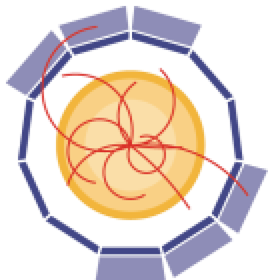
Advanced Through Silicon Vias for Pixel Detectors

WP 2 Session

F. Hügging, N. Owtscharenko, N. Wermes (U Bonn)
T. Fritzsch, O. Ehrmann, K. Zoschke (Fraunhofer IZM)



AIDA 2020

huegging@physik.uni-bonn.de

Introduction

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- Through Silicon Vias are nowadays widely used in industry for different purposes, e.g:
  - Memory chips
  - 3D integration
  - Interposers
- Usually these are dedicated, highly industrialized processes which are not accessible for other costumers
- Scope of the project is the development of a post processing TSV for a wider range of input material like:
  - Readout ICs for silicon pixel detectors
  - X-ray imager
  - IR cameras
  - Packaging of CMOS cameras

3D Integration Technology Using TSVs

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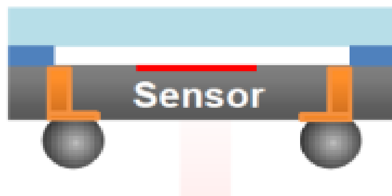
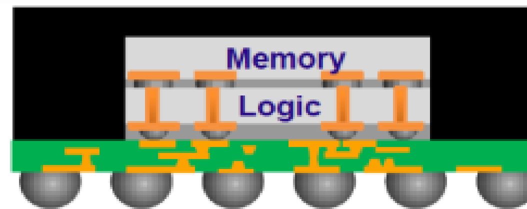
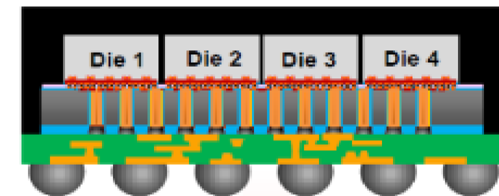
3D WLCSP

3D IC

2.5D Interposer







3D Packaging:
- **CMOS Image Sensors**
- **MEMS**

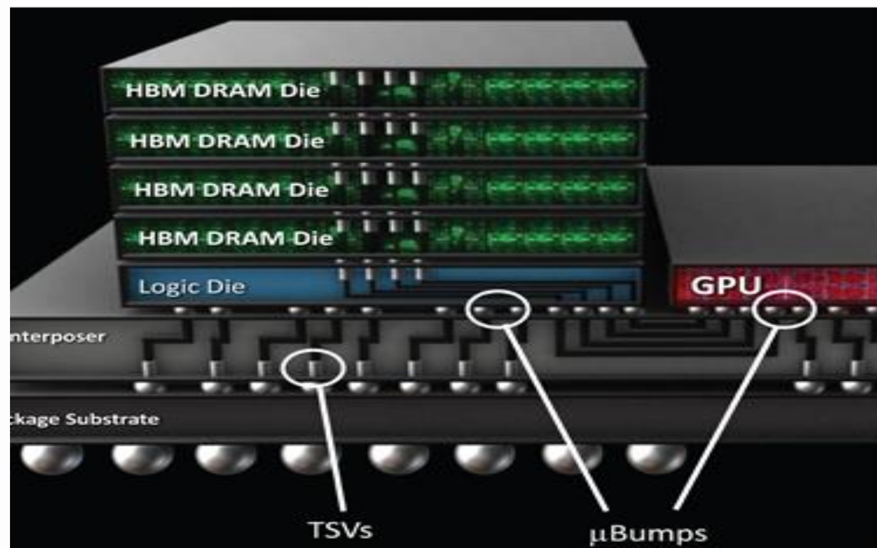
3D Chipstacking:
- **Logic & DRAM for higher bandwidth (WIDE I/O interface)**
- **Memory stacking**

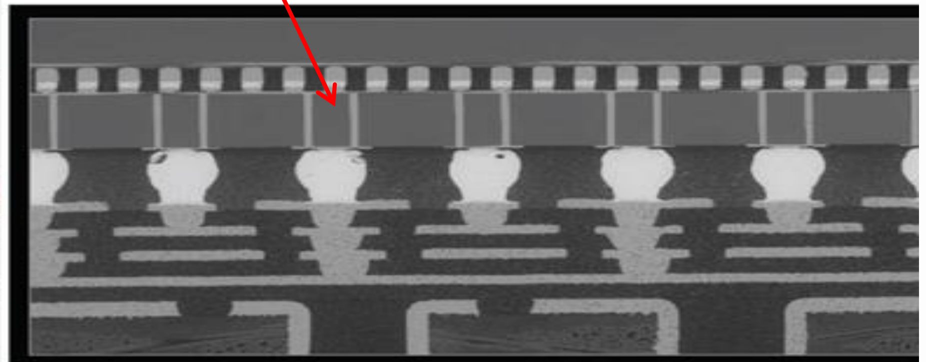
Lateral die stacking for high bandwidth:
- **Power/RF/Analog**
- **Logic & Analog**
- **Logic & Memory (GPU for Gaming)**

YOLE Développement

Yole Report 2012: 3DIC & TSV Interconnects

AMD's "Fiji" with Silicon Interposer and HBM





Source: AM

- MD has introduced its highly anticipated "Fiji" solution for the graphics market
- eatures a 595mm² logic device (ASIC) mounted in the center of a 1,011mm² Si inte
- our HBM stacks, each containing four DRAMs and a logic die, are also mounted on terposer
- here are approximately 200,000 interconnects in the module including Cu pillar icrobumps and C4 bumps
- he interposer has 65,000 TSVs with 10μm-diameter vias

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TSV landscape map

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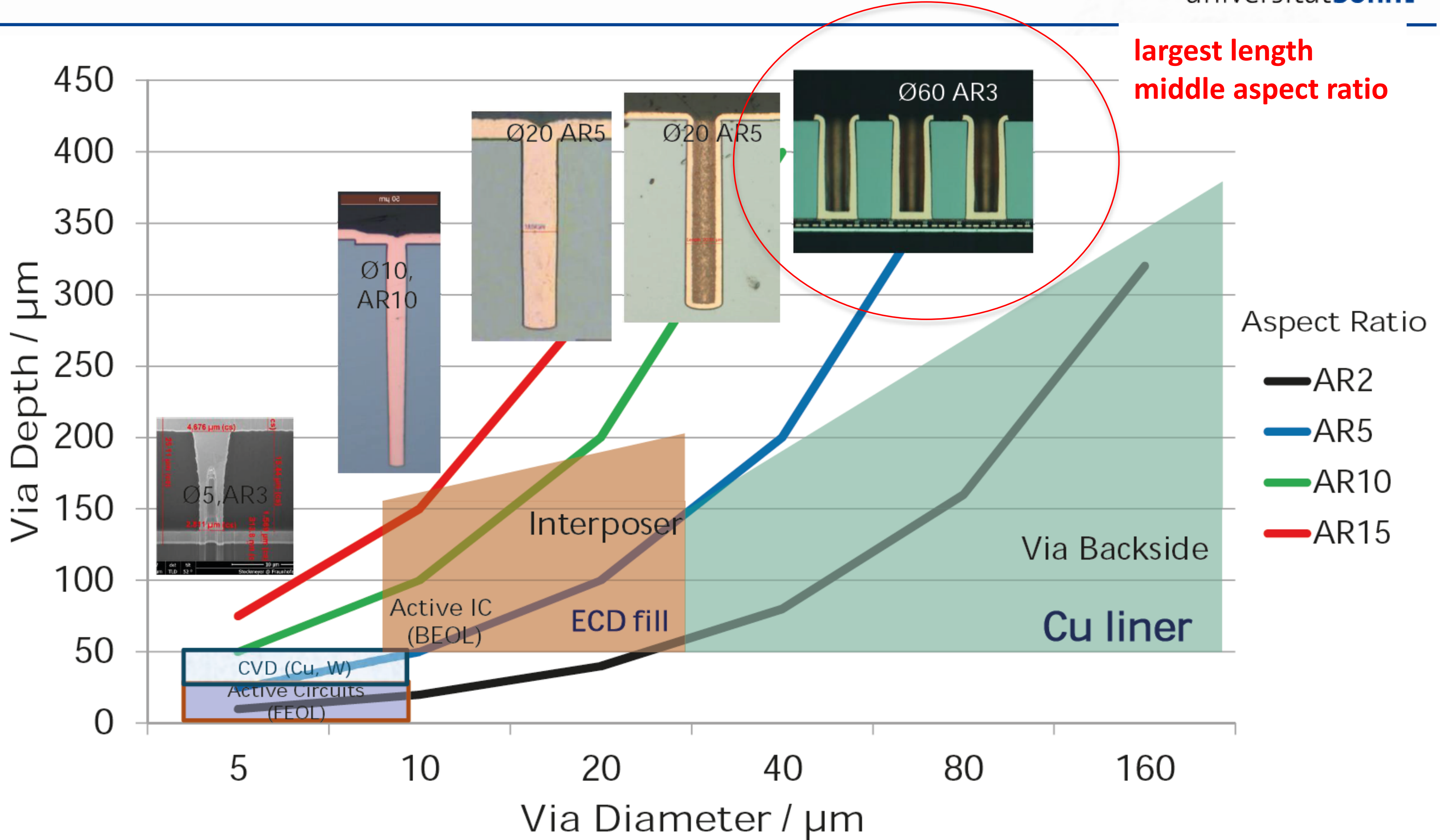

taken from T. Fritzsch, *Interposer – An enabling technology for fan-out hybrid pixel modules*, IWORID 2016, Barcelona.

Bonn-IZM TSV pixel project

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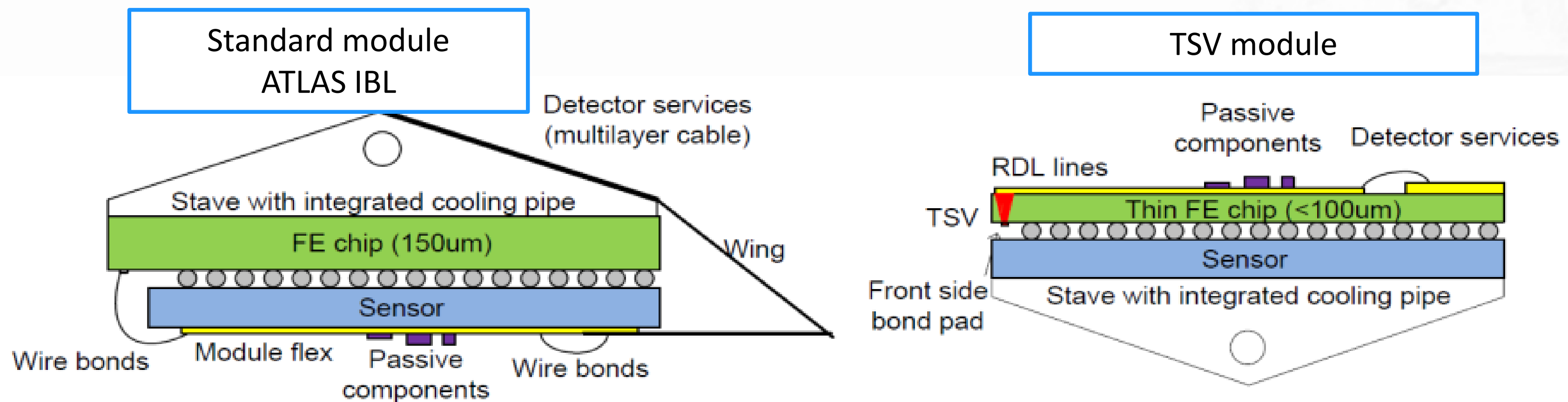
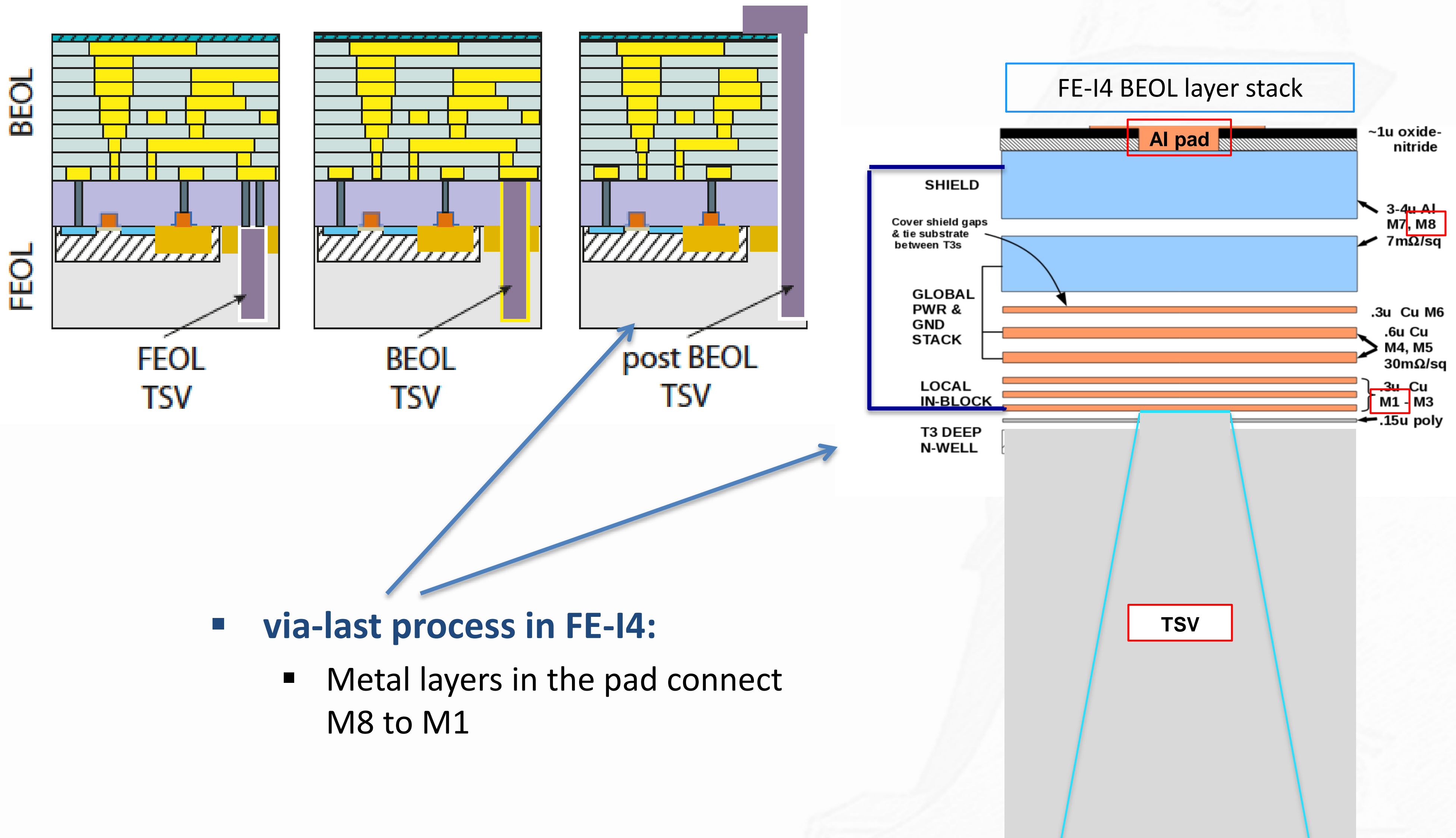


- **TSVs** + wafer thinning + aligned bonding are the key technical elements for a 3D extension of electronics integration -> eminent field of industrial research
  - denser packaging - lower power - larger I/O bandwidth - more functionality at lower cost
- Huge interest (and market) in packaging industry with fast recent advances
- **Promise** for pixel detectors -> more compact modules with active area maximization, no wire bonds, and 4-side abuttable (X-ray), use backside for wiring (RDL) → **joint interest Bonn - IZM**
- **Needs/challenges** which both partners profit from
  - large length and relatively large aspect ratio (length/diameter) TSVs with reliable fabrication yield
- Goal: **develop pixel modules for HL-LHC** employing TSVs in a via-last process (after CMOS process)

Through Silicon Via Types



- **via-last process in FE-I4:**
  - Metal layers in the pad connect M8 to M1

Bonn/IZM TSV experience

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Demonstrator single chip TSV modules built using

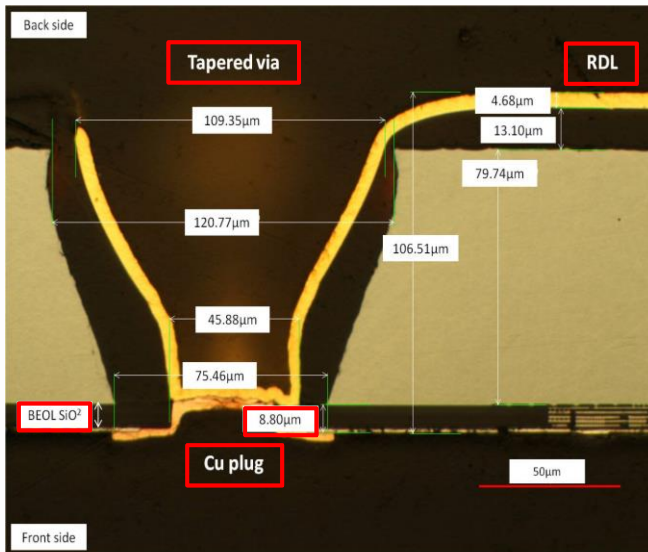
- FE-I3 ATLAS pixel readout chip 90 µm thin, 6 x 11 mm^2, with tapered profile TSVs and RDL
  Followed by solder bumping and flip chip

Journal of Instrumentation

A via last TSV process applied to ATLAS pixel detector modules: proof of principle demonstration

M Barbero[a], T Fritzsch[b], L Gonella[a], F Hügging[a], H Krüger[a], M Rothermund[b] and N Wermes[a]
Published 10 August 2012 • Journal of Instrumentation, Volume 7, August 2012

- aspect ratio 1:1
- no performance loss compared to standard modules observed



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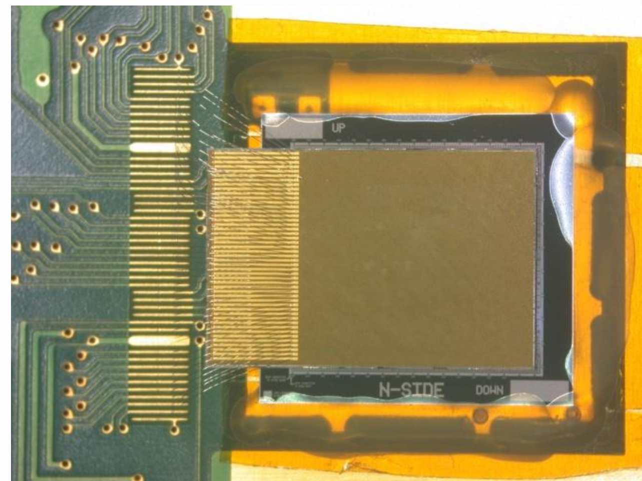
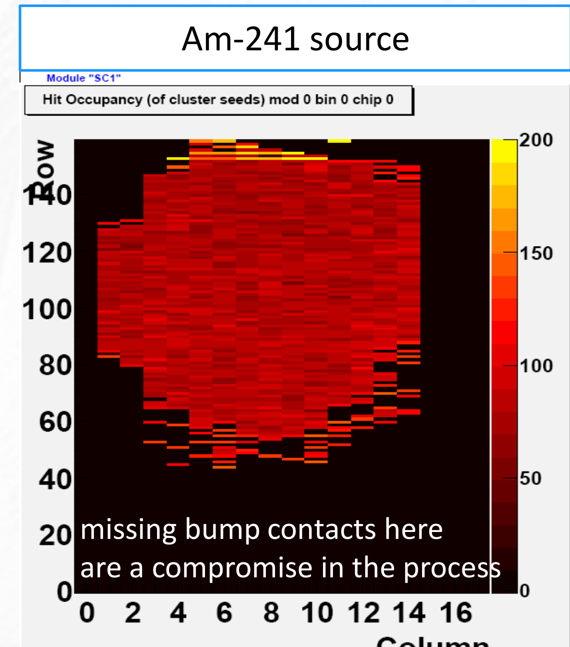
Module on board



Am-241 source



Bonn/IZM TSV experience

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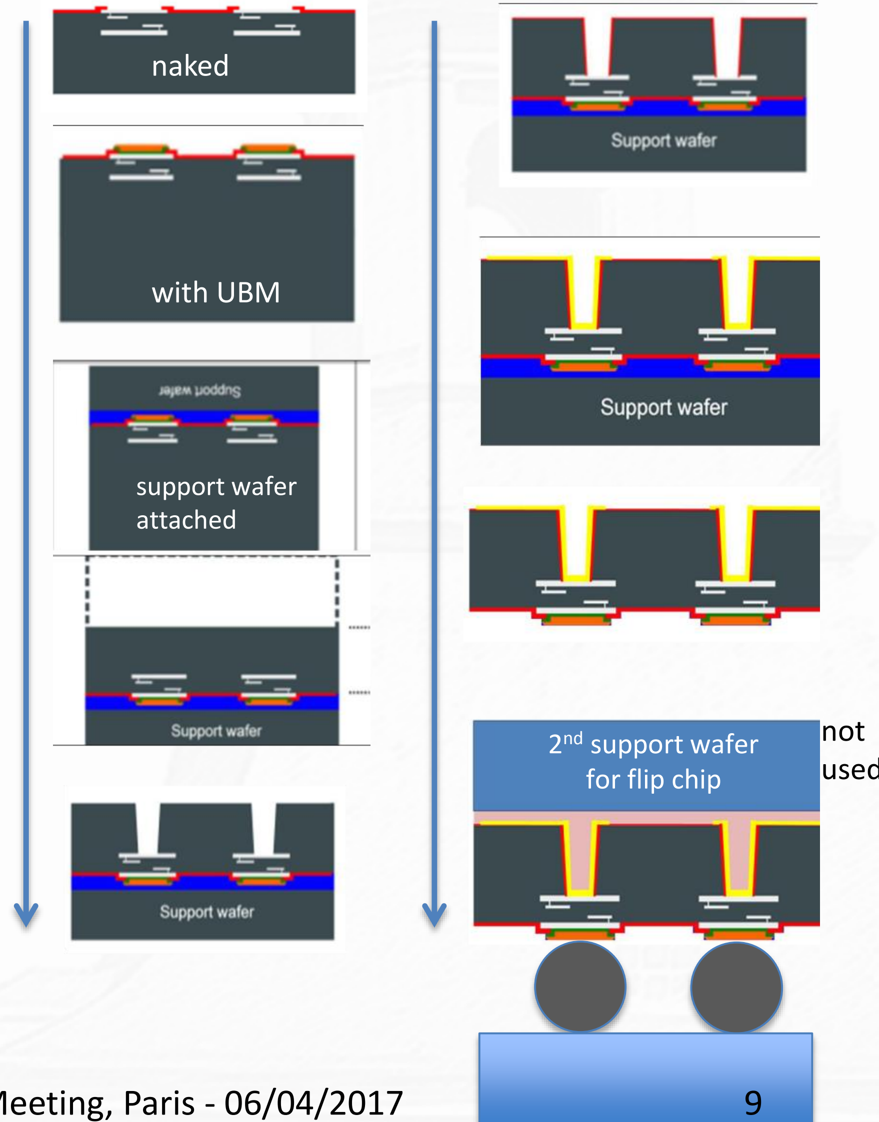
TSV modules using FE-I4 (ATLAS IBL chip): 160µm thick, 2 x 2 cm^2

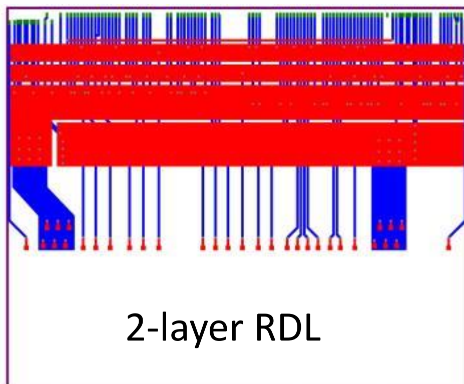
- use straight vias with aspect ratio 3.5 : 1

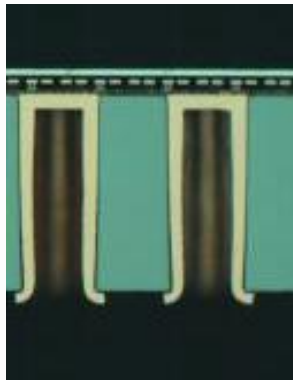
Goal: demonstration of **TSV/RDL processing together with solder bump bonding method** on 8” FE-I4 wafers thinned to 160µm (3 wafer pilot run)

Results:

- first processing attempt failed (no connection to M1)
- reworking (!), however, was successful
- yield ... not quite satisfactory







PoC project: Advanced Through Silicon Vias for Pixel Detectors

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- **Goal:** establish high yield TSV + RDL process for pixel modules
- straight vias through (ultra?) thinned FE-I4 wafers and chips: note **2x2 cm^2 chip size**
- **80 – 120 µm** thickness (to be optimized),
- aspect ratio = 2 : 1
- one handle wafer step needed
- complete development including flip-chipping process for the final pixel module

Challenges of the proposal

- reliable TSV fabrication ... yield hoped/expected to be much better than for project 2
- thin (o(100 µm)) wafers are needed for the goal of “large yield”
  challenge is the handling of large and very thin wafers/chips
- surprises during flip-chipping can also be an issue

Applications of the TSV project outside HEP

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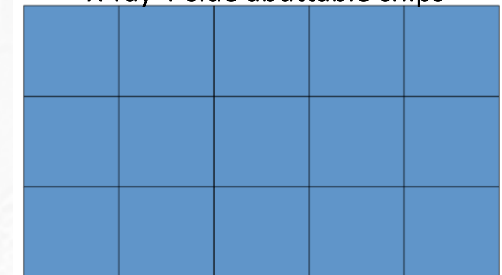
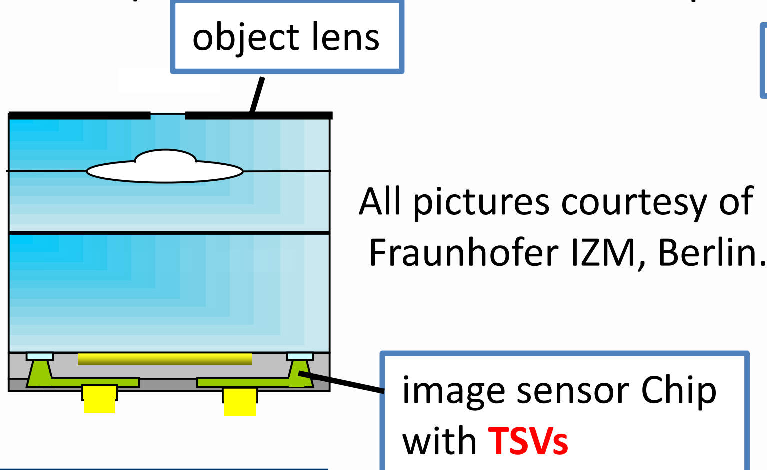
- **The approach in general**
  - Breakthrough for close to 100% yield **multi TSV/backside RDL heterogeneous integration** with high performance quality on small and medium production scales
    → benefits for many applications in CMOS tier stacking and for sensor/chip packaging applications
- **Specific applications** (beyond HL-LHC) in development with IZM



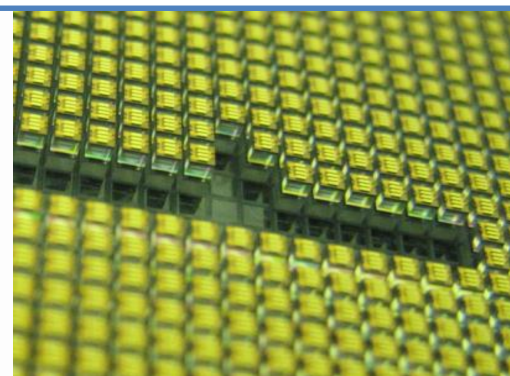
1) 4-side abuttable **X-ray sensors** (a la Medipix)

2) Backside processed (front side contact free) **light and IR sensors**

3) CMOS camera wafer level packaging with backside contacts → used in **endoscopy** (medical)



All pictures courtesy of Fraunhofer IZM, Berlin.



TSV Project Implementation Plan

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- WP1:
  - Process optimization for very thin (80-120 µm) readout wafers
- WP 2:
  - Design optimization of the TSV and RDL layers
- WP 3:
  - TSV run with optimized RDL design on FE-I4 wafer batch incl. electrical tests
- WP4:
  - Optimization of bumping and flip-chip using (ultra?) thin TSV chips to sensors
- WP 5:
  - Characterization of TSV chip sensor assemblies

Through Silicon Via (TSV) Formation – Basic Process Steps

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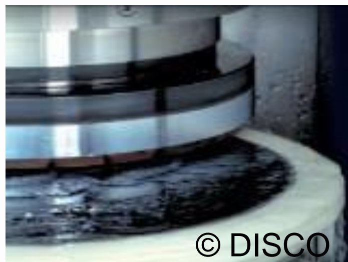
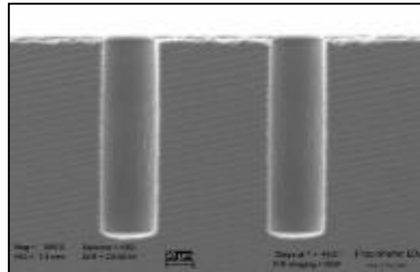
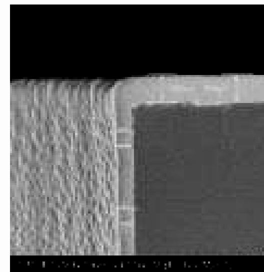
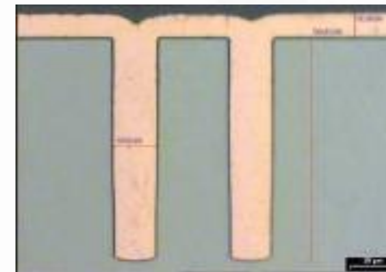
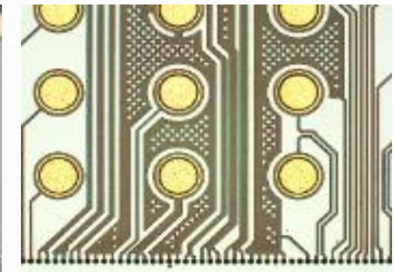
1. Wafer Thinning: Grinding, Wet Etching, DRIE
2. TSV Si-etching: DRIE BOSCH Process
3. TSV-Insulation: TEOS, PE-CVD, SA-CVD, Polymer
4. Adhesion-/Barrier-/Seed-Layer: Ti (TiW, TiN, Ta(N)) / Cu HI-PVD
5. Via filling: ECD Cu bottom up filling, liner filling
6. RDL / UBM pad metallization



All pictures courtesy of Fraunhofer IZM, Berlin.

TSV Via Backside – Via Last Process

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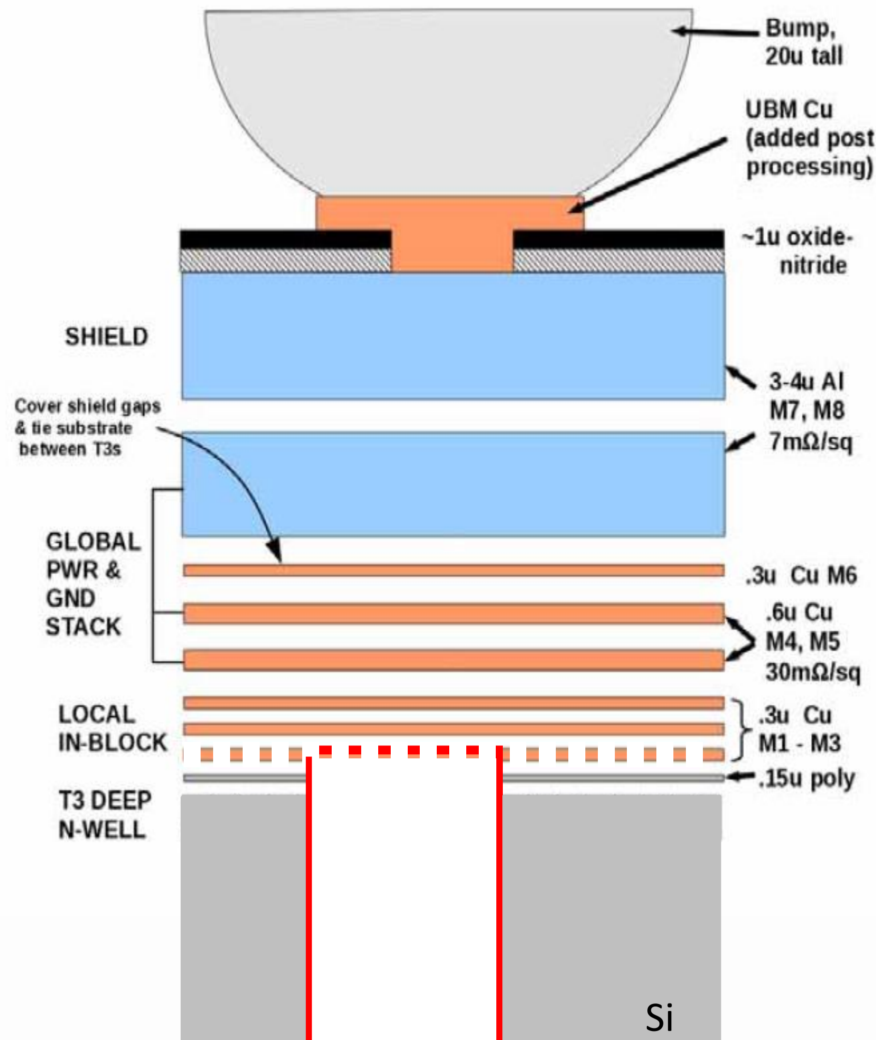
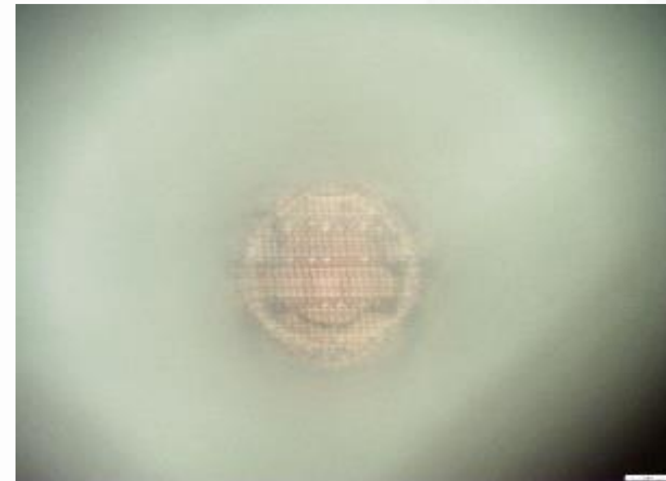
TSV and Oxide Etch Process



TSV from backside:

- Etch: Si / oxide / Poly-Si / oxide
- stop on M1 (cheesed M1)
- PECVD oxide deposition
- Oxide etch



TSV after silicon / Oxide etch (500x):
microscopic view into TSV AR2-3/ diam.60µm
→ cheesed/meshed M1
→ oxide opened?
→ harder decision for smaller diameter

TSV Via Backside – Via Last Process

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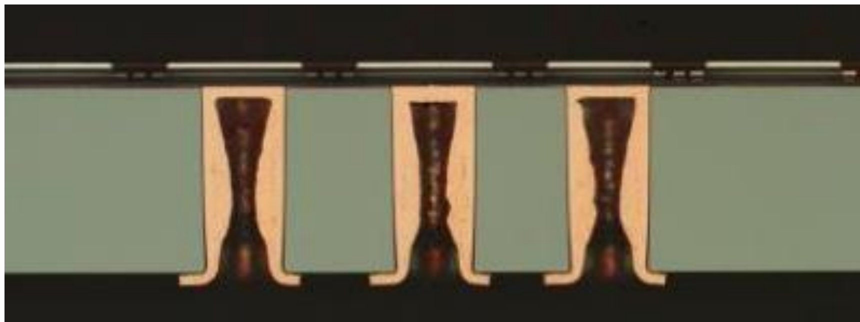
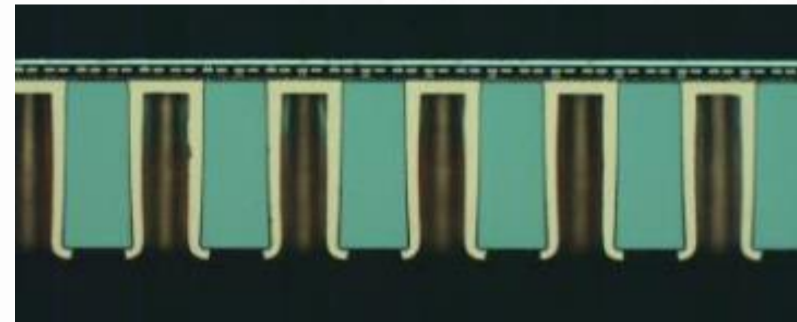
TSV Filling Process by Electroplating

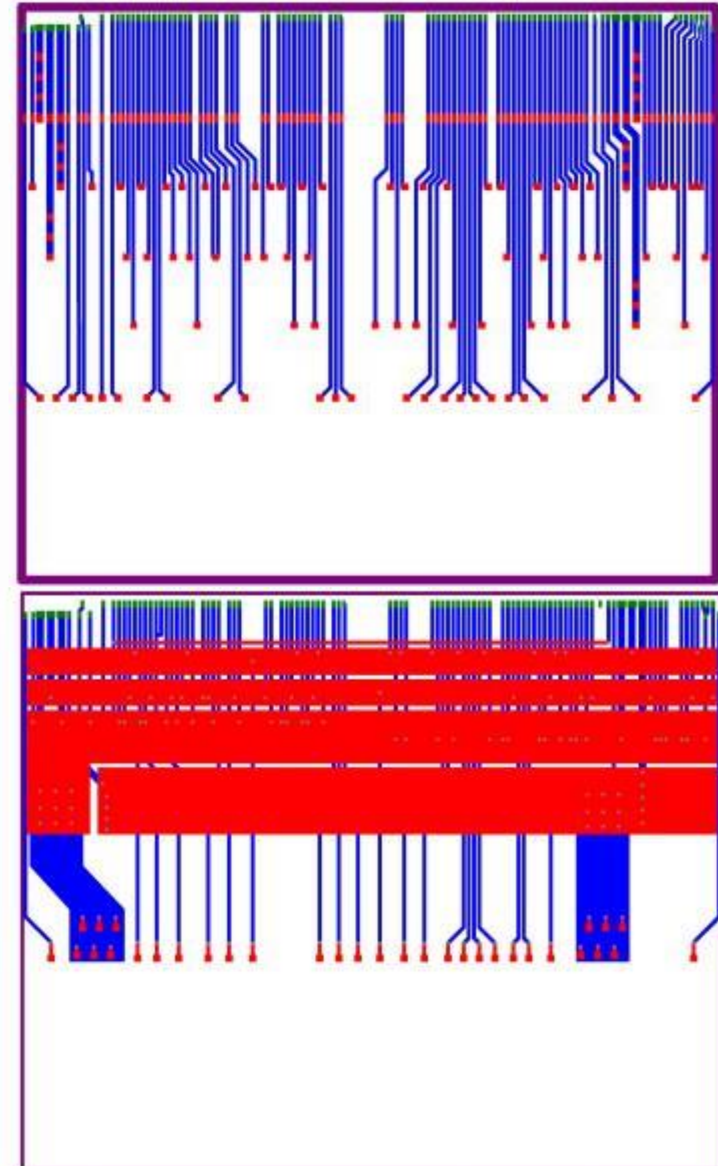
- IZM ATLAS FE-I4 TSV Phase 2:
  - First setup with not optimized via filling parameters
    → TSV filling tends to close the TSV at half of the TSV depth
  - Rework + second fill
  - Final cross section of TSVs after rework of the first via filling process step and 2nd filling
- MEDIPIX3 TSV Pilot Batch:
  - same IBM technology, same wafer size
  - Cross section of TSVs with optimized via filling process
  - TSV process already OK after first setup





RDL designs of the FE-I4 TSV chips

- Two different RDL designs are used for the FE-I4 chips with TSV:
  - simple design with one metal layer as for the Fe-I2/3 modules
  - a more complex RDL layout features 2 metal layers with an additional BCB passivation between the metal layers → takes over some of the functionality of the module flex (power distribution etc., only passive components are missing but can be added later)
  - both RDL designs are compatible with advanced laser soldering techniques



RDL structuring and visual inspection

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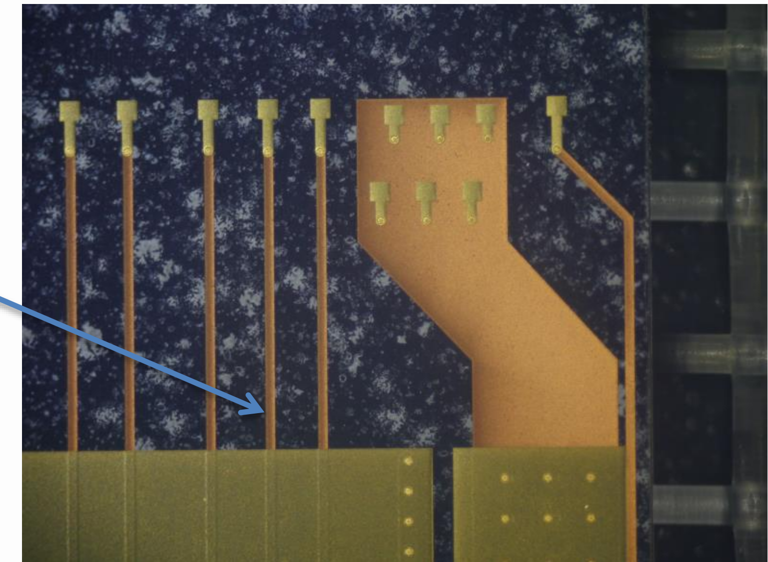
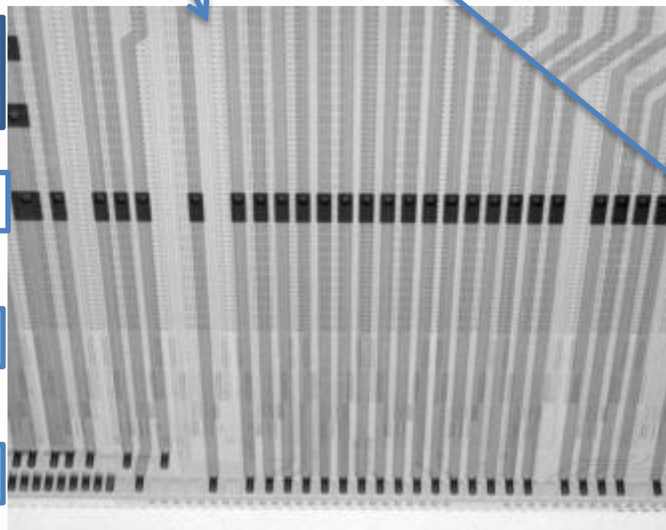
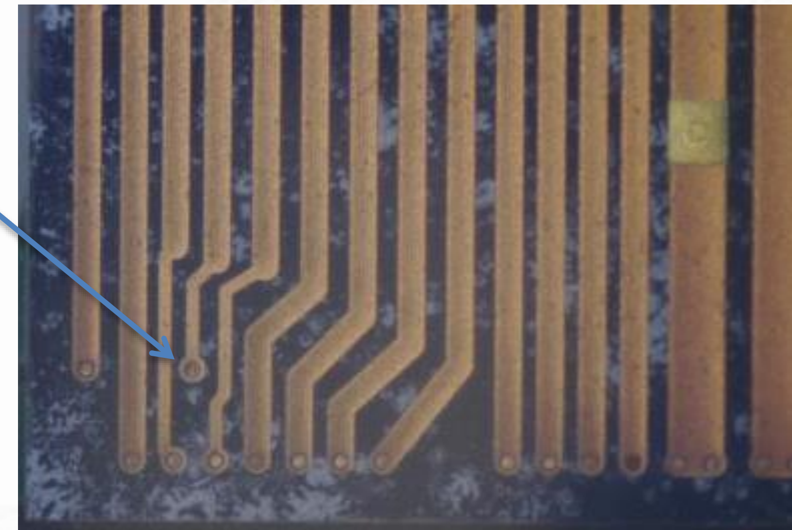
- Inspected chips chips showed good processing results regarding RDL processing:
  - good shape of the RDL layers (Cu and NiAu) and clear vias
  - X-ray image shows good metal coverage over full TSV depth



X-ray check of TSV filling and RDL-connection:





Backside discoloration pattern due to rework process

Kick-off Meeting of TSV project

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- Kick-off Meeting for the project in Bonn at 10/03/2017
- Project partner (U Bonn and IZM) agreed upon the implementation plan
- First actions about the next steps discussed:
  - Lessons learned from the previous experiences
  - TSV setup run process optimization
  - design of dedicated test structures for TSV setup run → special structures for measuring capacitance and inductance of TSV and RDL layers

Restricted · Europe/Zurich

AIDA 2020 PoC Kick-Off: Advanced Through Silicon Vias for Pixel Detectors

Friday 10 Mar 2017, 08:30 → 15:00 Europe/Zurich

Description Konferenzraum II PI

08:30 → 09:00 Überbick und Prozessierung von TSVs (30m)
Speakers: Kai Zoschke, Thomas Fritzsch (Fraunhofer IZM)
2017-03-10 Fraunh...

09:00 → 09:30 Zeitplan und Tests mit dem Ziel eines betriebsfähigen FE-I4 Moduls mit TSV Betrieb (30m)
Diskussion
Speakers: Fabian Huegging (University of Bonn (DE)), Thomas Fritzsch (Fraunhofer IZM)

09:30 → 10:00 ITk-Pixel Planungen (30m)
Speaker: Fabian Huegging (University of Bonn (DE))
Itk-pixel_overview_...

10:00 → 10:30 Ausblick und Details zu Bumping: Flip-Chip mit dem RD53A chip (30m)
Speakers: Fabian Huegging (University of Bonn (DE)), Hans Krueger (University of Bonn)
Itk-RD53A_bumpin...

10:30 → 11:00 CMOS Pixel Entwicklungen (30m)
Speaker: Tomasz Hemperek (University of Bonn (DE))
CMOS - IZM - 10Ma... CMOS - IZM - 10Ma...

11:00 → 11:30 Überblick über neuere Entwicklungen im Packaging (30m)

ATLAS FE-I4 TSV Work Planning

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WP1: TSV process step evaluation

March to May 2017

- Fabrication of process setup wafer with dedicated test structures
- Evaluation of individual process steps (wafer thinning, TSV etching, passivation and RDL layer deposition)
- Characterization of test structures

WP2: TSV wafer design and mask fabrication

June to July 2017

- Development of gds2 wafer layout mask set (TSV etch, passivation etch, RDL structuring, …)
- Fabrication of lithography glass masks

WP3: ATLAS FE-I4 batch TSV process

August to October 2017

- UBM deposition on the wafer front side,
- thinning of the wafer
- bonding of the thinned wafer onto carrier
- backside processing including TSV etch, deposition of passivation, plating base TSV filling and RDL multi-layer

WP4: Flip chip bonding process

November to December 2017

- Assembly of setup modules and optimization of bonding parameters
- Characterization of bonding interfaces and bonding yield
- Assembly of functional modules

WP5: Characterization of TSV chip sensor assemblies

January to May 2018

- Initial functional tests and tuning
- Full characterization of TSV pixel detector modules in lab and at test beams

ATLAS FE-I4 TSV Work Planning

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WP1 – Process Modifications:

- Reduced wafer thickness: 160µm → 120…90µm:

  + better visibility of via bottom after TSV etch / oxide etch
  + improvement of TSV filling behaviour
  - higher risk of wafer breakage

- Fabrication of TSV Daisy Chain Testwafer with dedicated M1 setup layer:

  +/- setup of TSV etch process but without poly-Si layer
  - additional wafer fabrication (process steps)

- Test of backside carrier wafer process:

  + higher stability up to dicing process
  + stabilisation of FE-I4 chip during flip chip process
  - carrier release after flip chip assembly
  - more cleaning steps necessary

Conclusions

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- U Bonn and IZM have long term relationship for bump bonding of hybrid pixel detectors including post processing of Readout IC wafers.
- Experience of usage of post process TSV for pixel detectors already for some years with quite some success.
- Goal is to generalize this approach not only for HEP pixel detectors but also for industrial similar detector projects like imager or compact CMOS cameras
- A versatile via last TSV process with straight side vias on IO pads and a multi-layer RDL is being developed for the ATLAS FE-I4 Pixel Detector as Proof-of-Concept
- Project started with a Kick-off Meeting on March 10, 2017 and currently a setup TSV run is prepared to find optimal processing parameters for the TSV process.