AIDA 2020

WP8/NA7 Large scale cryogenic liquid detectors

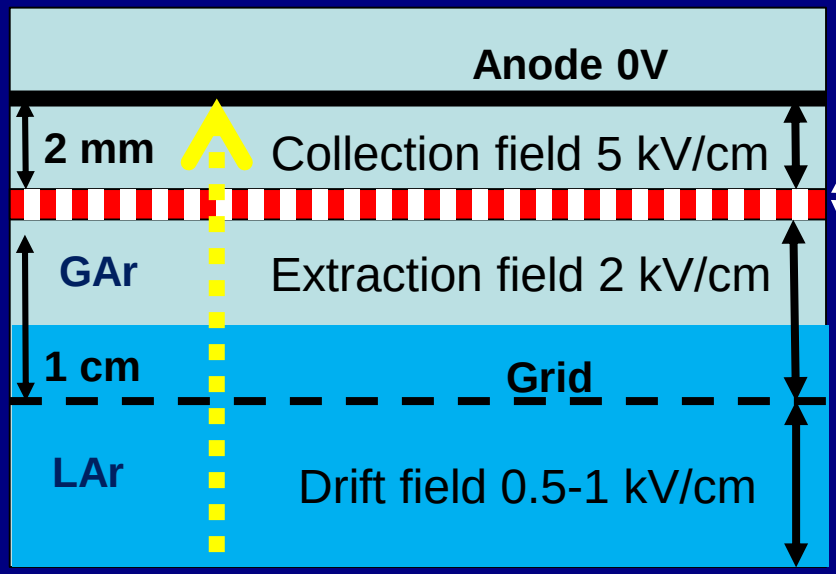
Charge readout and dual-phase

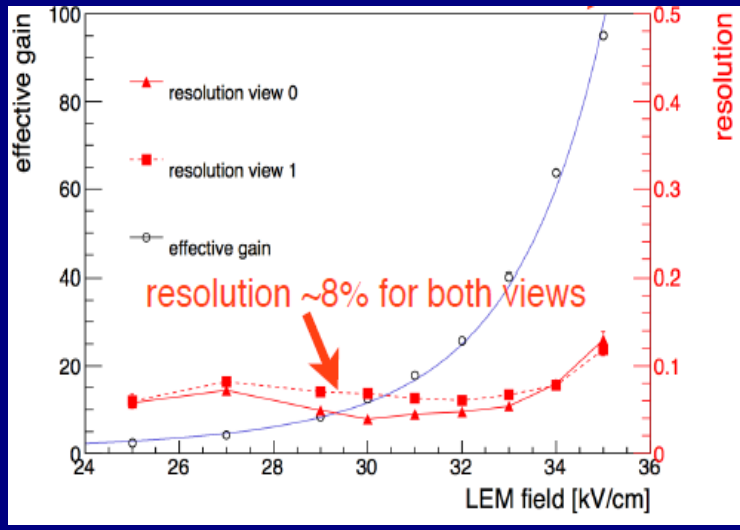
AIDA-2020 Annual meeting LPNHE
WP8 Report 5/4/2017

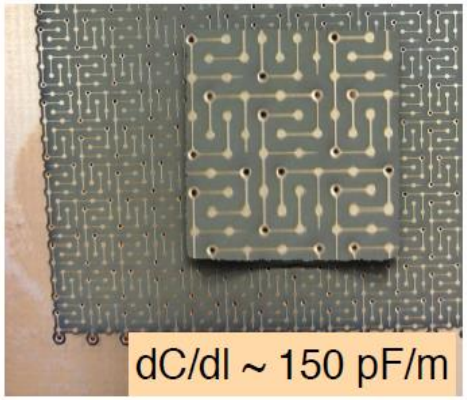
D.Autiero (IPNL Lyon)

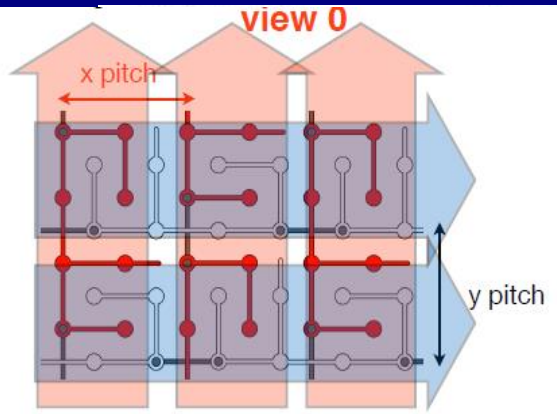
Dual-phase readout:

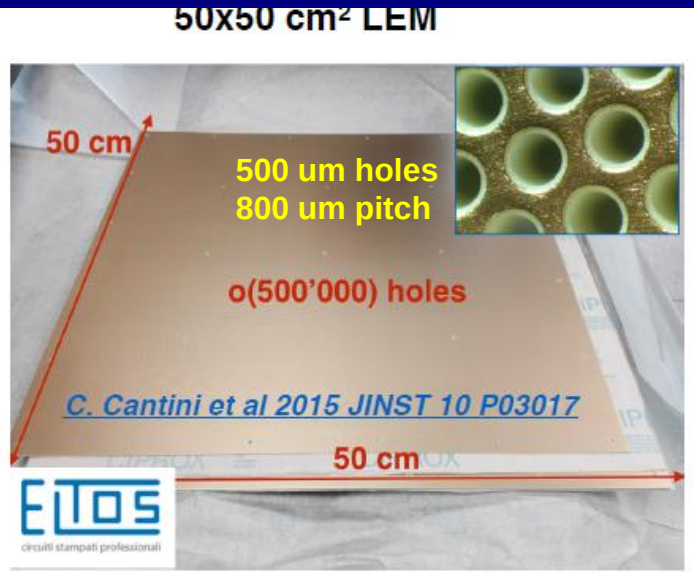
Long drift, high S/N: extraction of electrons from the liquid and multiplication with avalanches in pure argon with micro-pattern detectors like LEM (Large Electron Multipliers)
Tunable gain (~20 minimum), two symmetric collection views, coupling to cold electronics

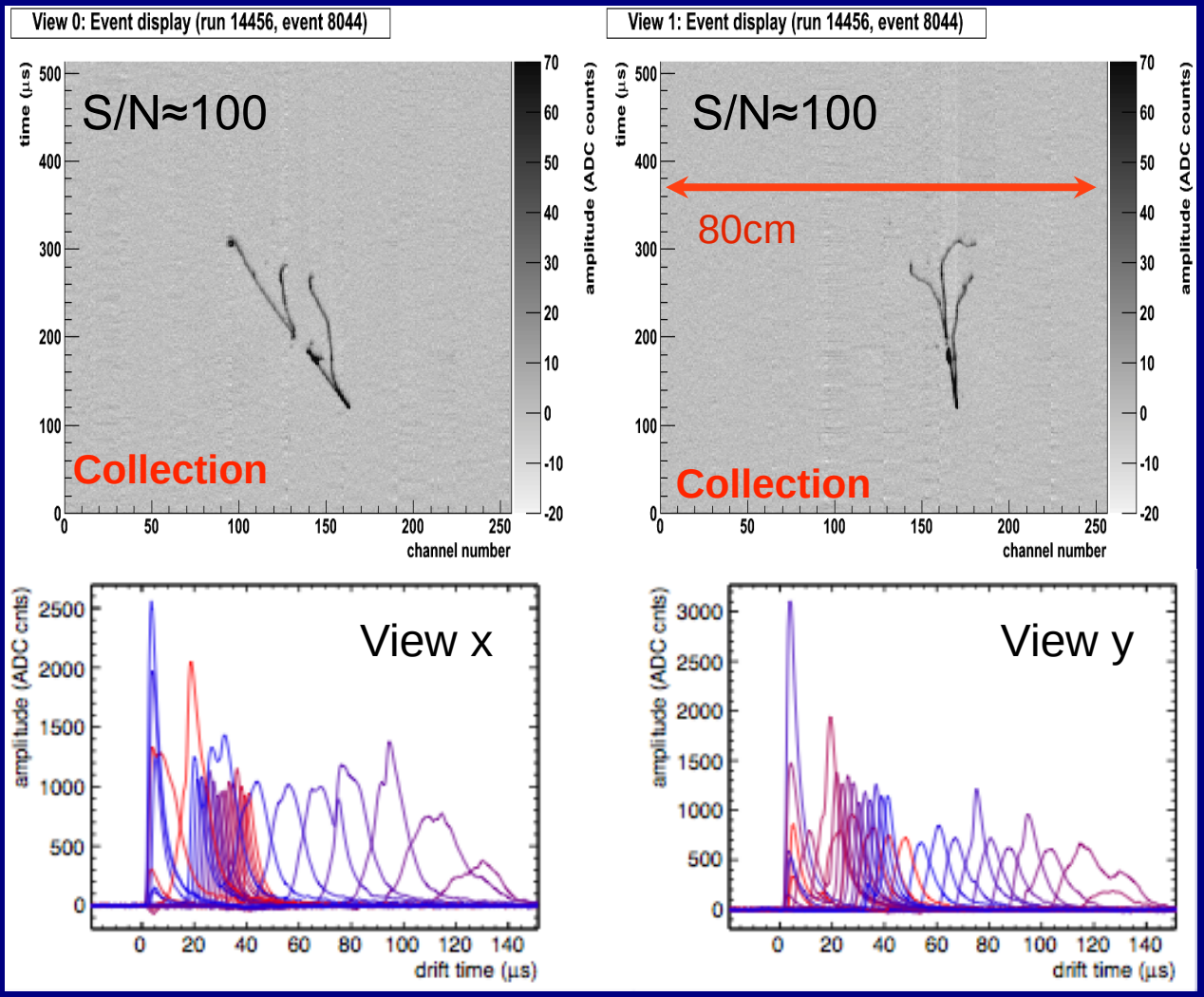








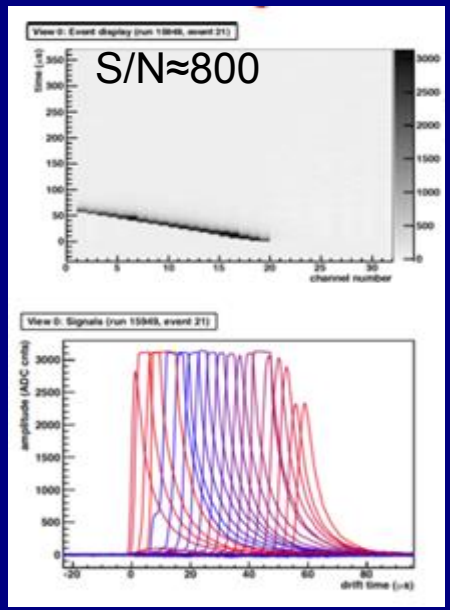




Dual-phase prototypes measuring real data events since 6 years with active volumes from 3 to 250 liters:

> 15 millions of cosmic events collected in stable conditions S/N~100 for m.i.p. achieved starting from gain ~15

- 3x1x1 m^3 setup and 6x6x6 m^3 DP ProtoDUNE at CERN



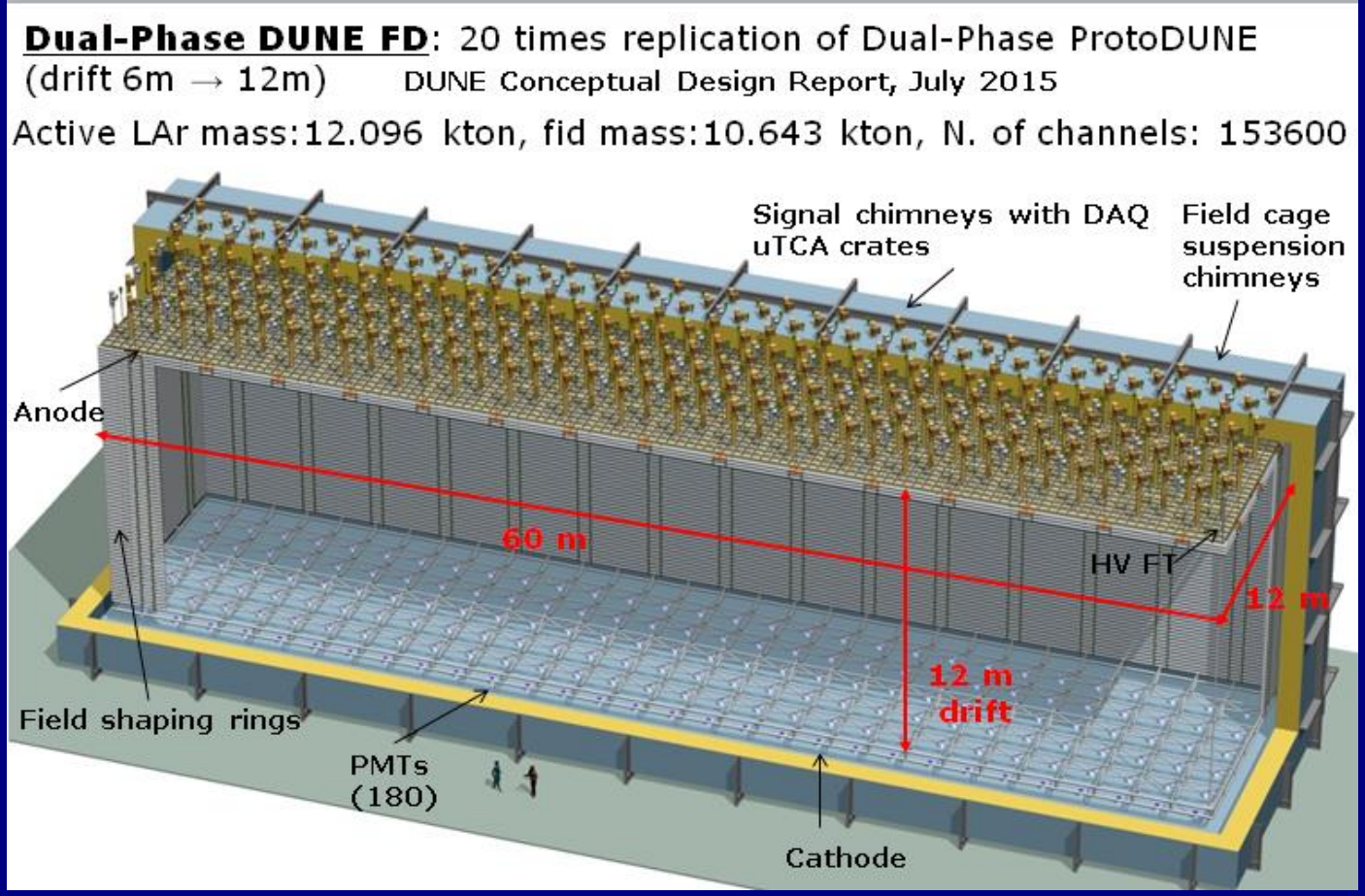
Max achieved gain ~200

Literature:

NIM A617 (2010) p188-192
NIM A641 (2011) p 48-57
JINST 7 (2012) P08026
JINST 8 (2013) P04012
JINST 9 (2014) P03017
JINST 10 (2015) P03017

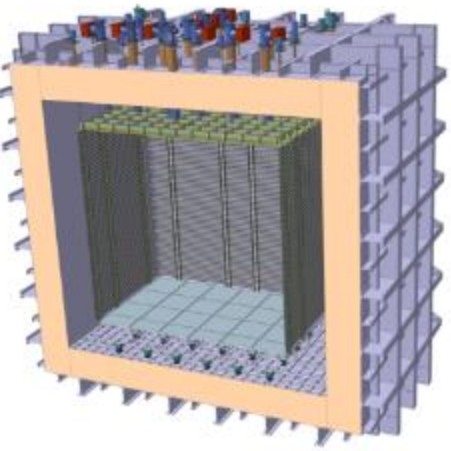
Dual-phase 10 kton FD module

- 80 CRP units
- 60 field shaping rings
- 240 signal FT chimneys
- 240 suspension chimneys
- 180 PMTs
- 153600 readout channels

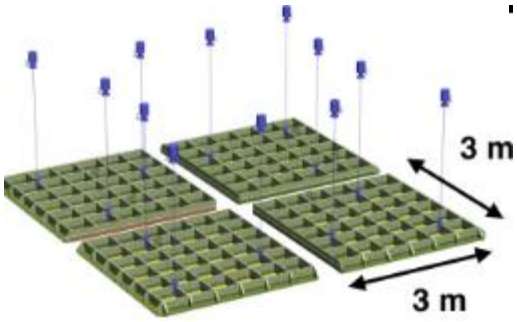


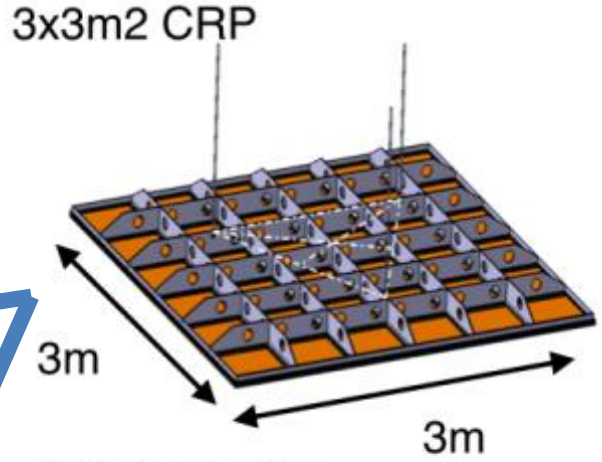
Advantages of double-phase design:

- Anode with 2 collection (X, Y) views (no induction views), no ambiguities
- Strips pitch 3.125 mm, 3 m length
- Tunable gain in gas phase (20-100), high S/N ratio for m.i.p. > 100, <100 KeV threshold, min. purity requirement 3ms → operative margins vs purity, noise
- Long drift projective geometry: reduced number of readout channels
- No materials in the active volume
- Accessible and replaceable cryogenic FE electronics, high bandwidth low cost external uTCA digital electronics



The Dual-Phase ProtoDUNE/WA105 6x6x6 m^3 detector is built out of the same **3x3m^2 Charge Readout Plane units (CRP)** foreseen for the 10 kton Dual-Phase DUNE Far Detector (same QA/QC and installation chains)

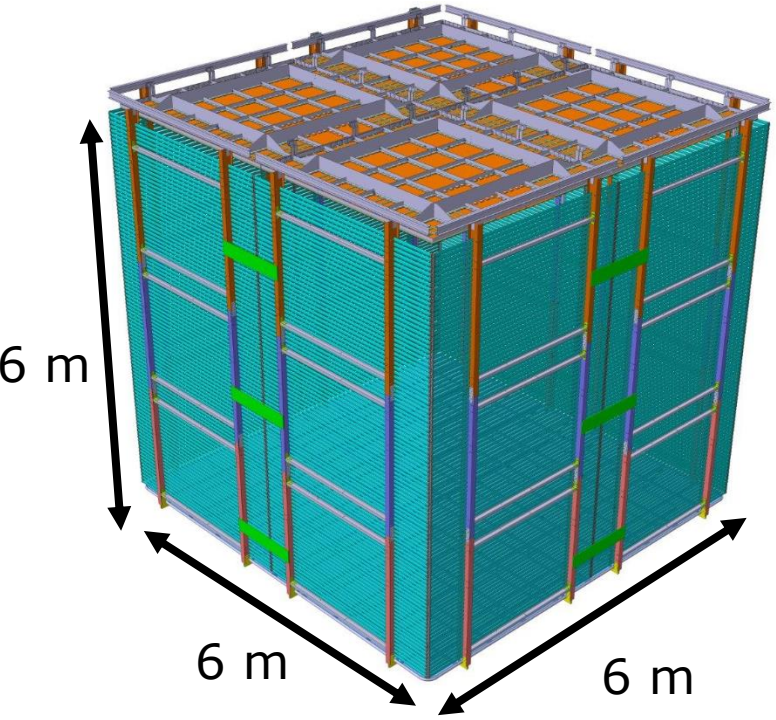


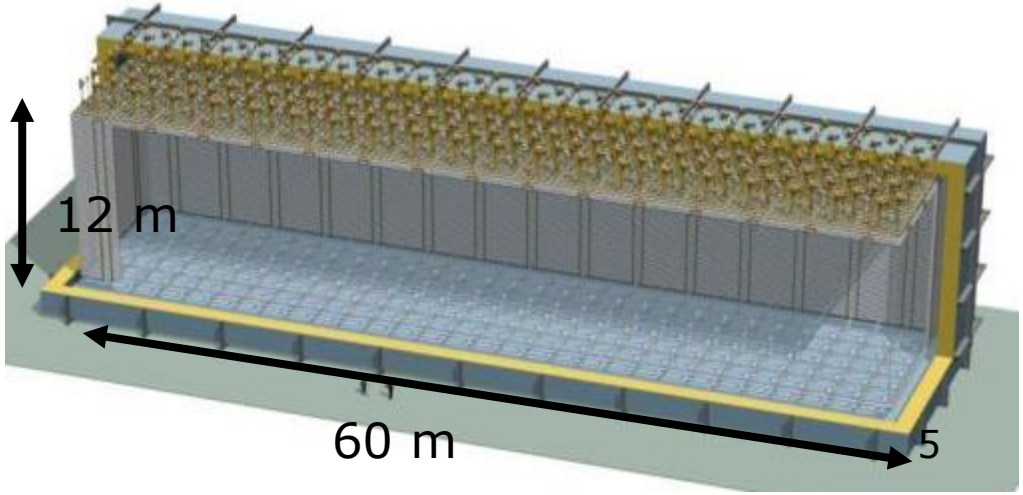


1920 channels/CRP
Accessible cold electronics in chimney

WA105: 4 CRP

10 kton: 80 CRP



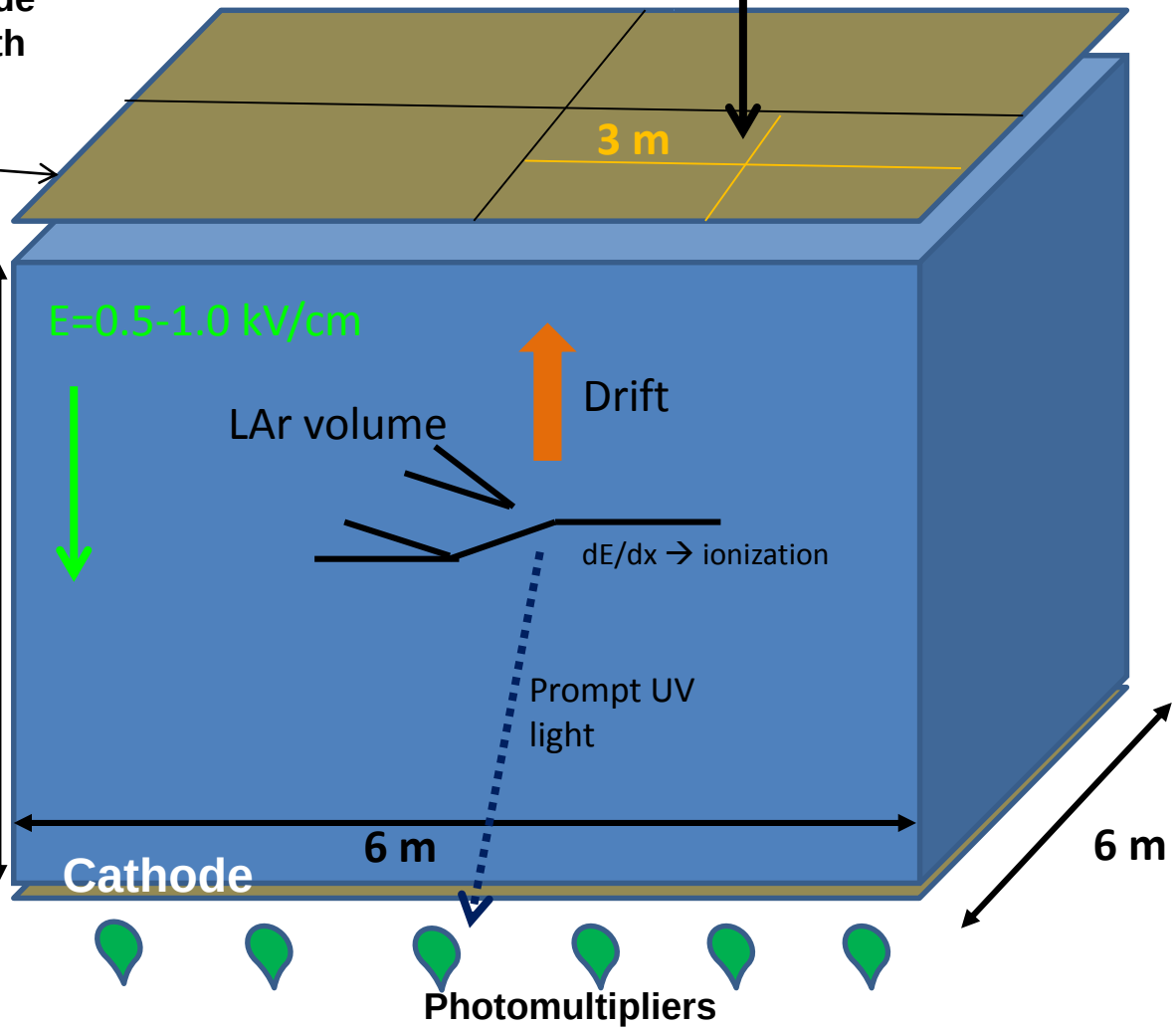


Dual phase liquid argon TPC
6x6x6 m^3 active volume

→ Event size: drift window of
7680 channels x 10000 samples ⇒ 146.8 MB

X and Y charge collection strips
3.125 mm pitch, 3 m long →7680 readout channels

Segmented anode in gas phase with dual phase amplification

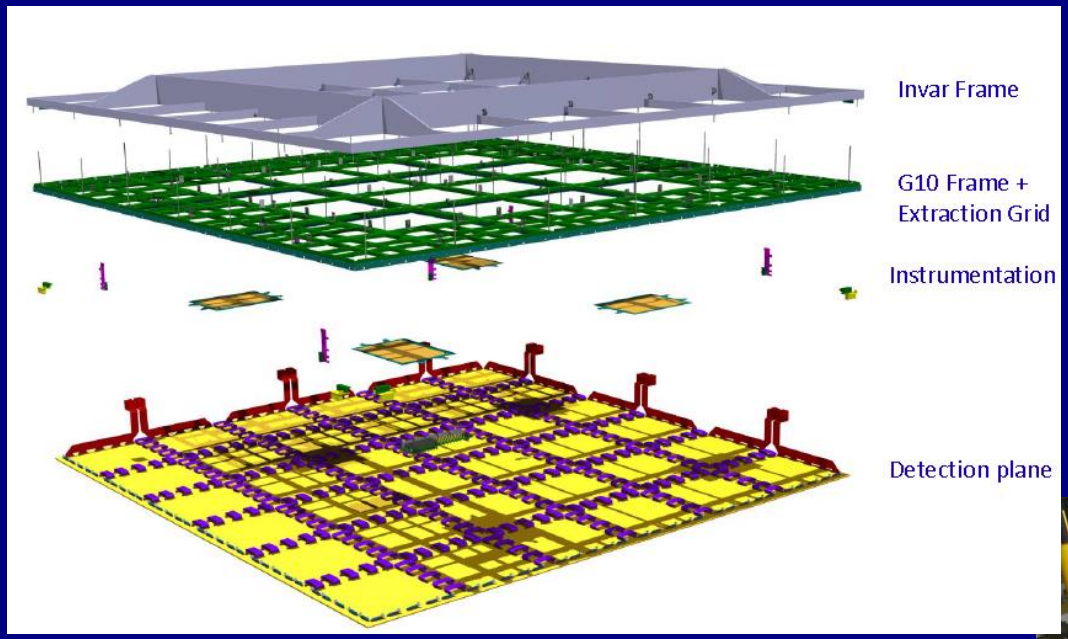


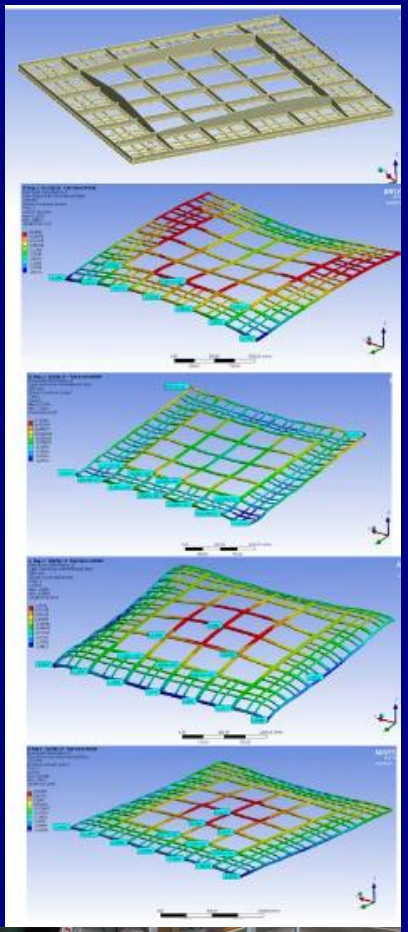
Drift coordinate
6 m = 4 ms
sampling 2.5 MHz
(400 ns), 12 bits

→ 10000 samples per drift window

3x3 m^2 CRPs integrating the LEM-anode sandwiches (50x50 cm^2) and their suspension feedthroughs

→ Invar frame + decoupling mechanisms in assembly in order to ensure planarity conditions +-0.5 mm (gravity, temperature gradient) over the 3x3 m^2 surface which incorporates composite materials and ensure minimal dead space in between CRPs

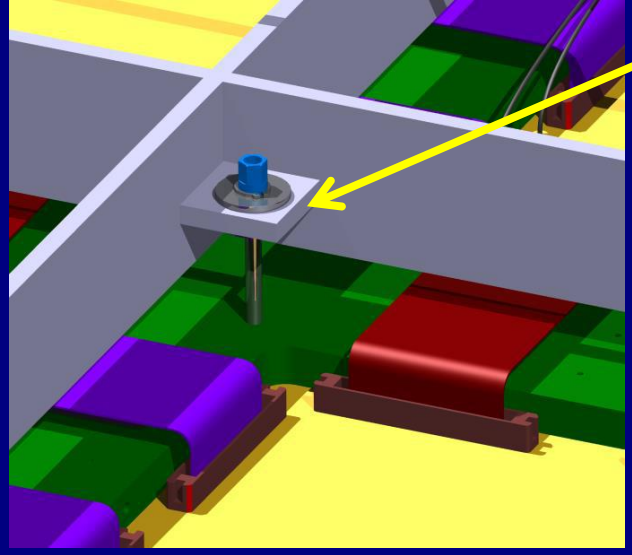




→See talks by B. Aimard (CRPs) and A. Delbart (LEM-anodes production) in DP parallel session

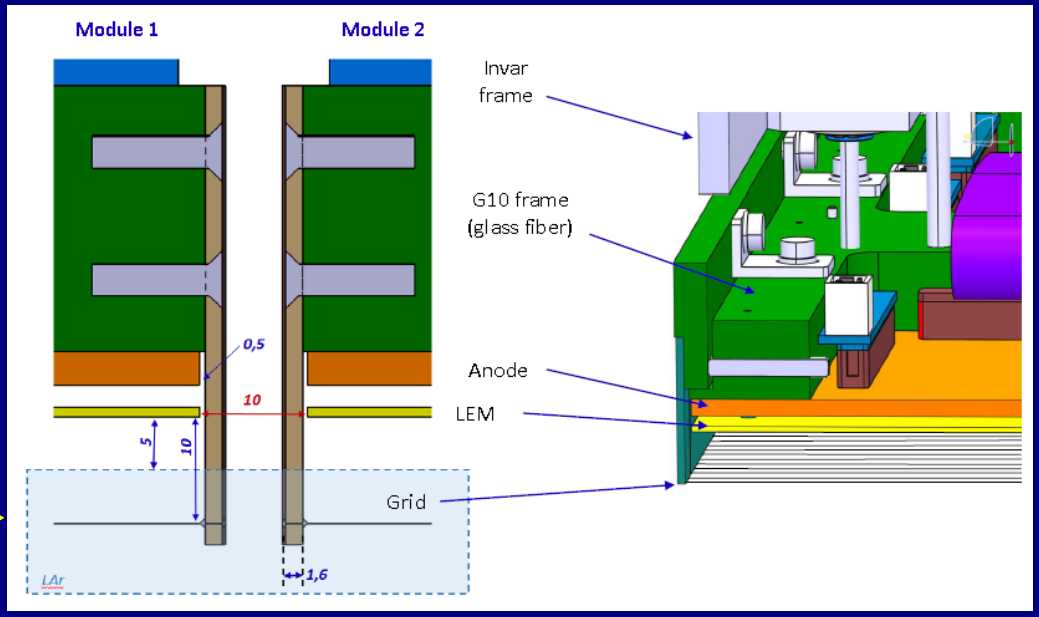
CRP mechanical structure design:

→ campaign of cold bath tests + photogrammetry on differential effects in thermal contraction, design of decoupling mechanism

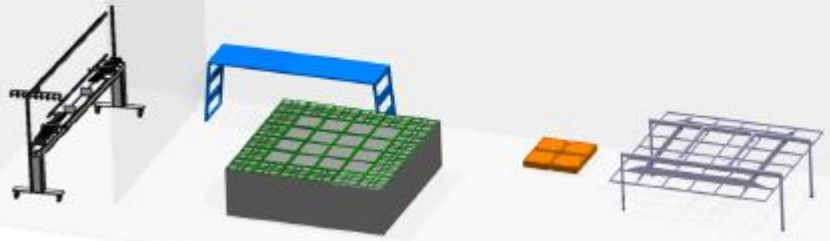


Thermal decoupling supports of G10 frame on invar frame

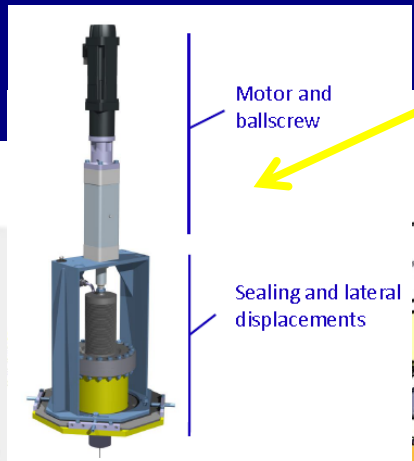
Integration of the grid of submerged extraction wires in the frame minimizing dead space in between CRPs. Tests for the wires system design

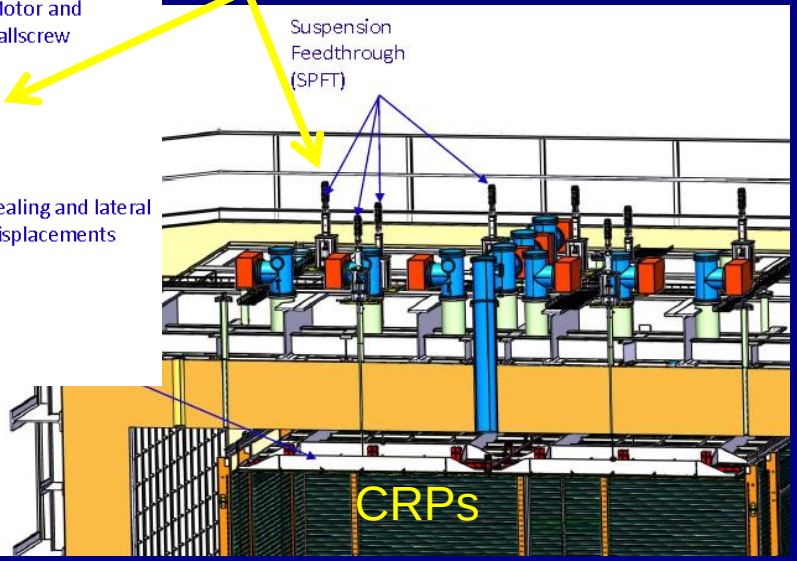


Tooling, assembly and installation procedures defined → getting ready for production



Suspension feedthroughs





WA105 Accessible cold front-end electronics and uTCA DAQ system 7680 ch

Full accessibility provided by the double-phase charge readout at the top of the detector

➢ **Digital electronics at warm on the tank deck:**

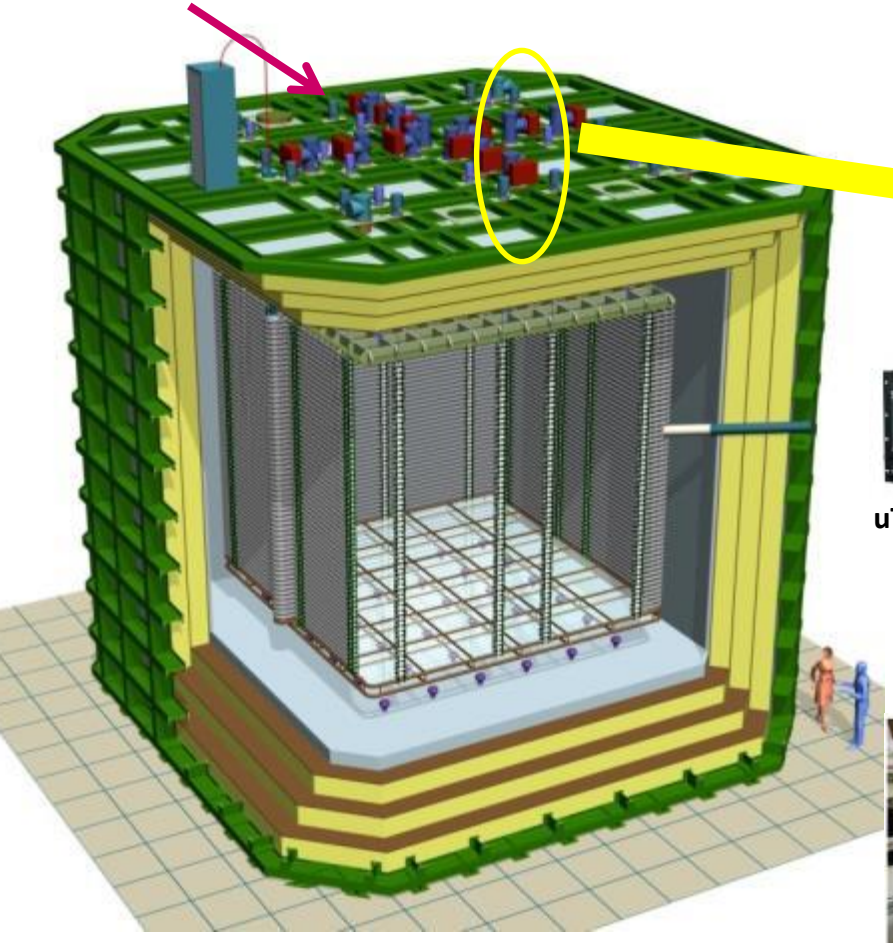
- Architecture based on uTCA standard
- 1 crate/signal chimney, 640 channels/crate

→ 12 uTCA crates, 10 AMC cards/crate, 64 ch/card

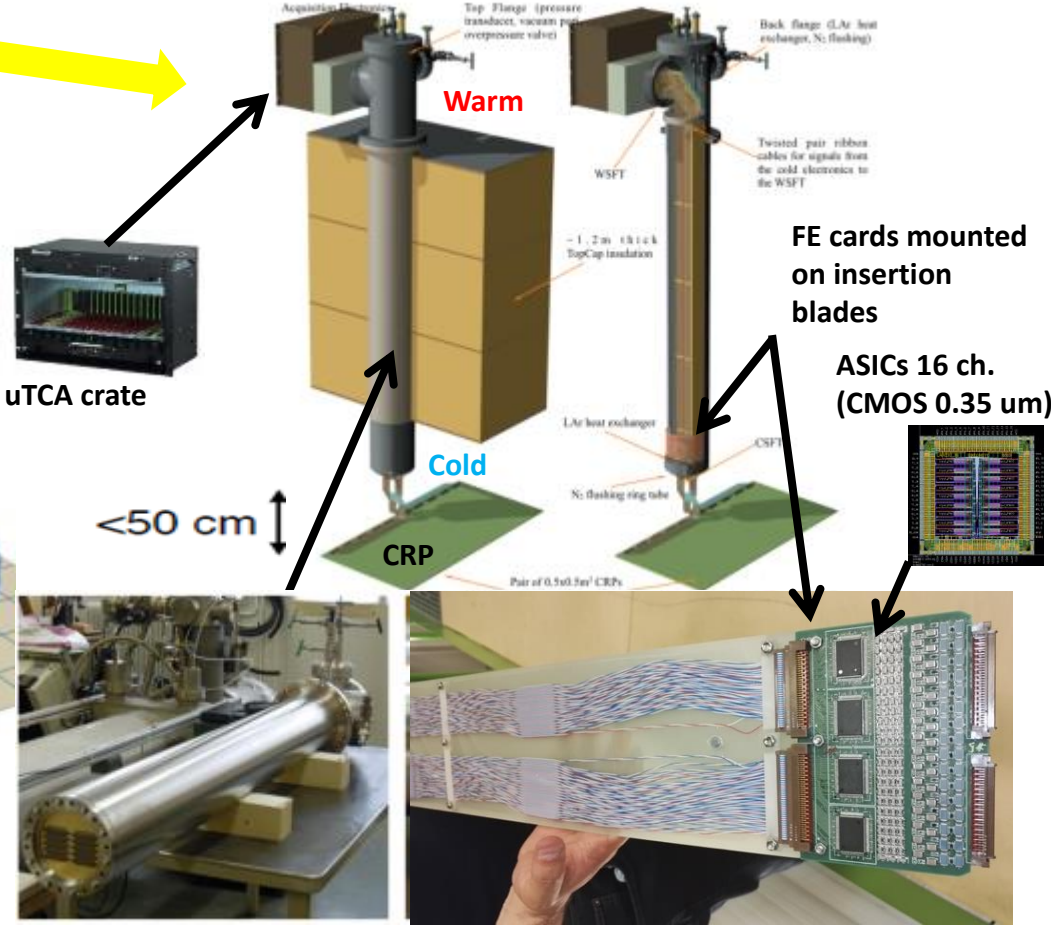
➢ **Cryogenic ASIC amplifiers (CMOS 0.35um) 16ch externally accessible:**

- Working at 110K at the bottom of the signal chimneys
- Cards fixed to a plug accessible from outside

→Short cables capacitance, low noise at low T



Signal chimney



Cost effective and fully accessible cold front-end electronics and DAQ

Ongoing R&D since 2006→ in production for 6x6x6 (7680 readout channels)

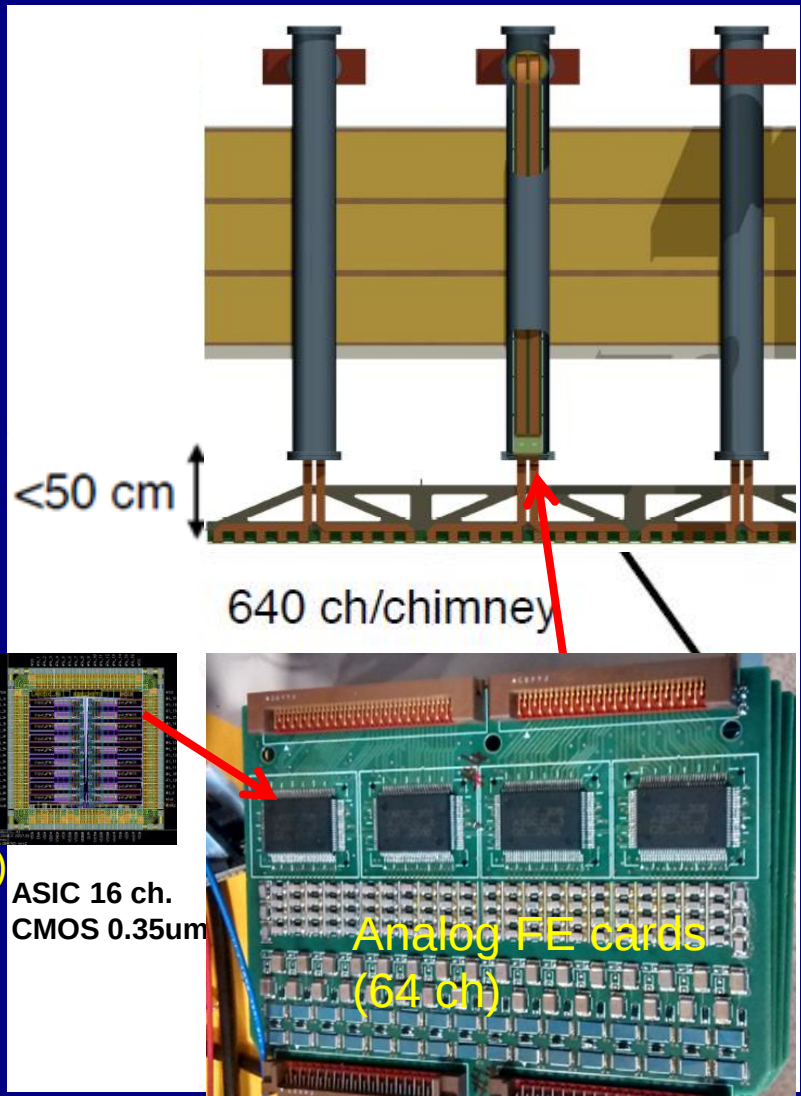
ASIC (CMOS 0.35 um) 16 ch. amplifiers working at ~110 K to profit from minimal noise conditions:

- FE electronics inside chimneys, cards fixed to a plug accessible from outside
- Distance cards-CRP<50 cm
- Dynamic range 40 mips, (1200 fC) (LEM gain =20)
- 1300 e- ENC @250 pF, <100 keV sensitivity
- Single and double-slope versions
- Power consumption <18 mW/ch
- **Produced at the end of 2015 in 700 units (entire 6x6x6)**
- **1280 channels installed on 3x1x1**

DAQ in warm zone on the tank deck:

- Architecture based on uTCA standard
- Local processors replaced by virtual processors emulated in low cost FPGAs (NIOS)
- Integration of the time distribution chain (improved PTP)
- Bittware S5-PCIe-HQ 10 Gbe backend with OPENCL and high computing power in FPGAs
- **Production of uTCA cards started at the end of 2015, pre-batch already deployed on 3x1x1**

→ Large scalability (150k channels for 10kton) at low costs

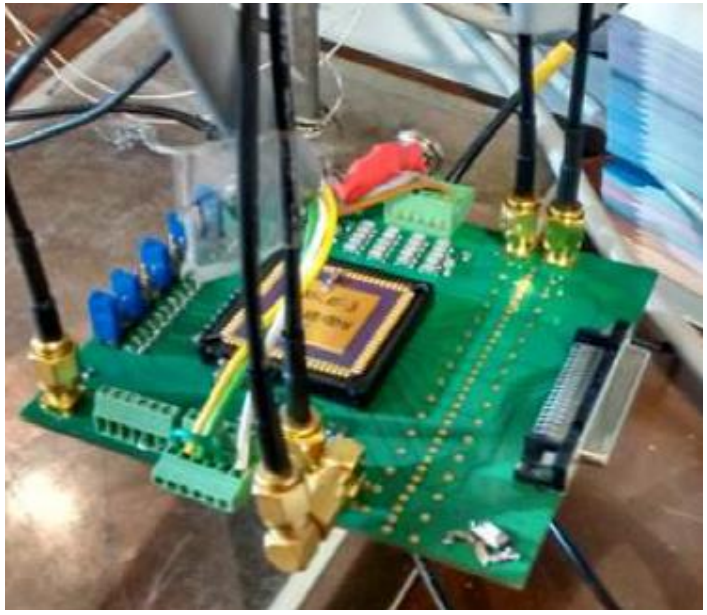


Cryogenic FE electronics :

Dual-slope ASICs final version

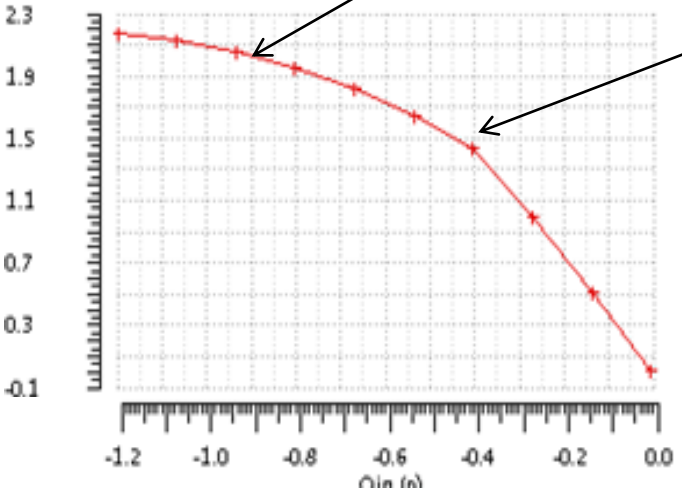
- 16 channels
- Double slope gain with “kink” at 400 fC
- 1200 fC dynamic range

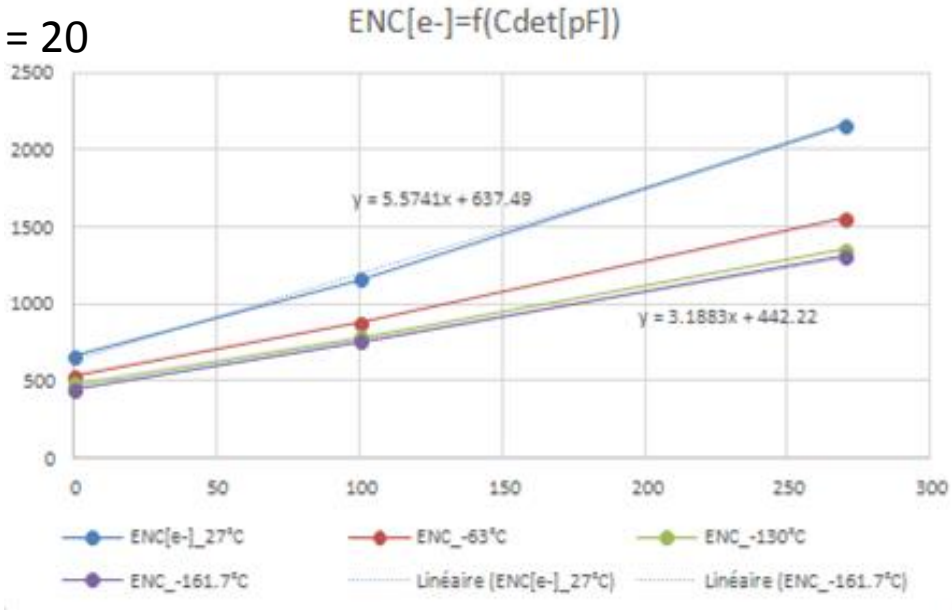
(batch of 25 circuits) tested in January 2016, fully satisfactory. Full production for 6x6x6 produced and purchased (700 chips).



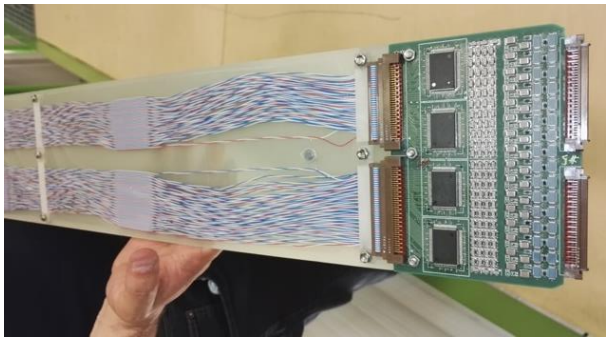
~log regime up to 1200 fC

Kink at 400 fC
~13 mip with
LEM gain = 20



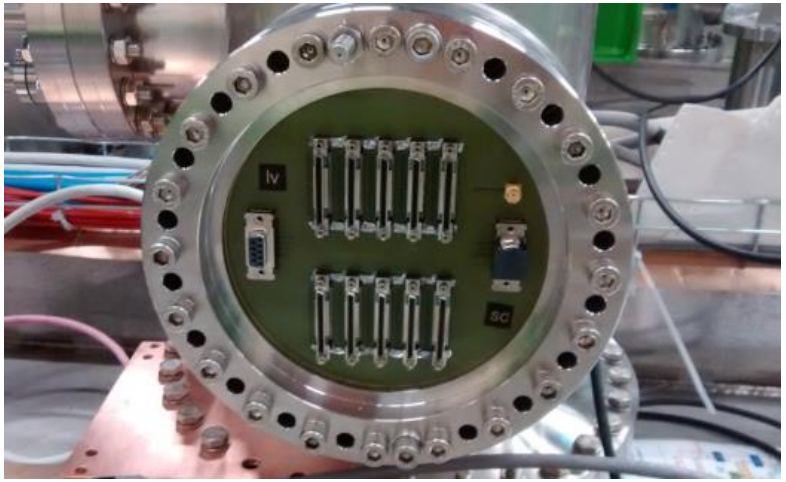


FE-cards designed in 2016 together with chimneys warm flanges PCBs

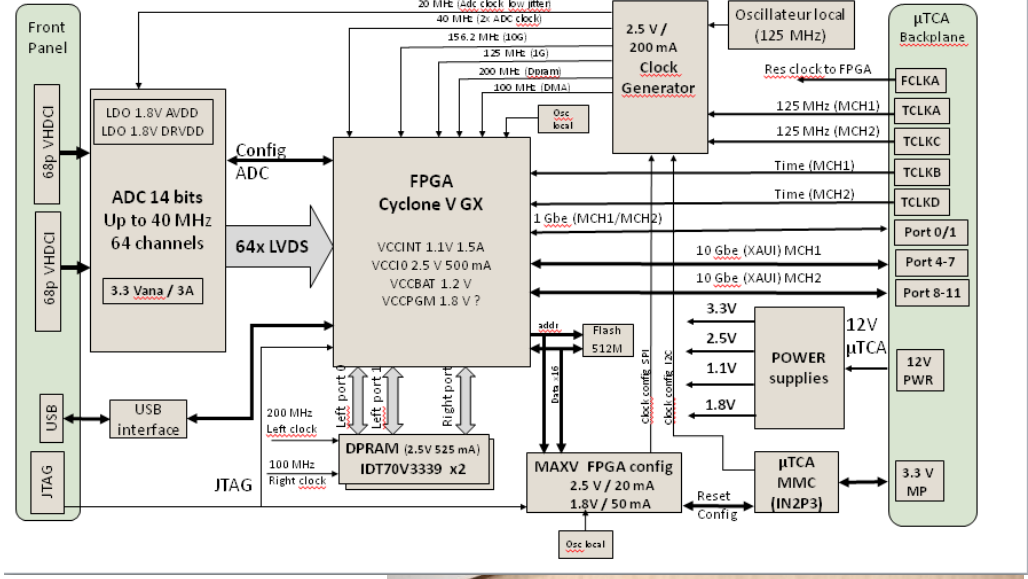


20 FE cards (1280 channels) produced and installed on 3x1x1 pilot detector at CERN

Warm flange PCB with VHDCI connections to uTCA crate for digitization



uTCA DAQ system:



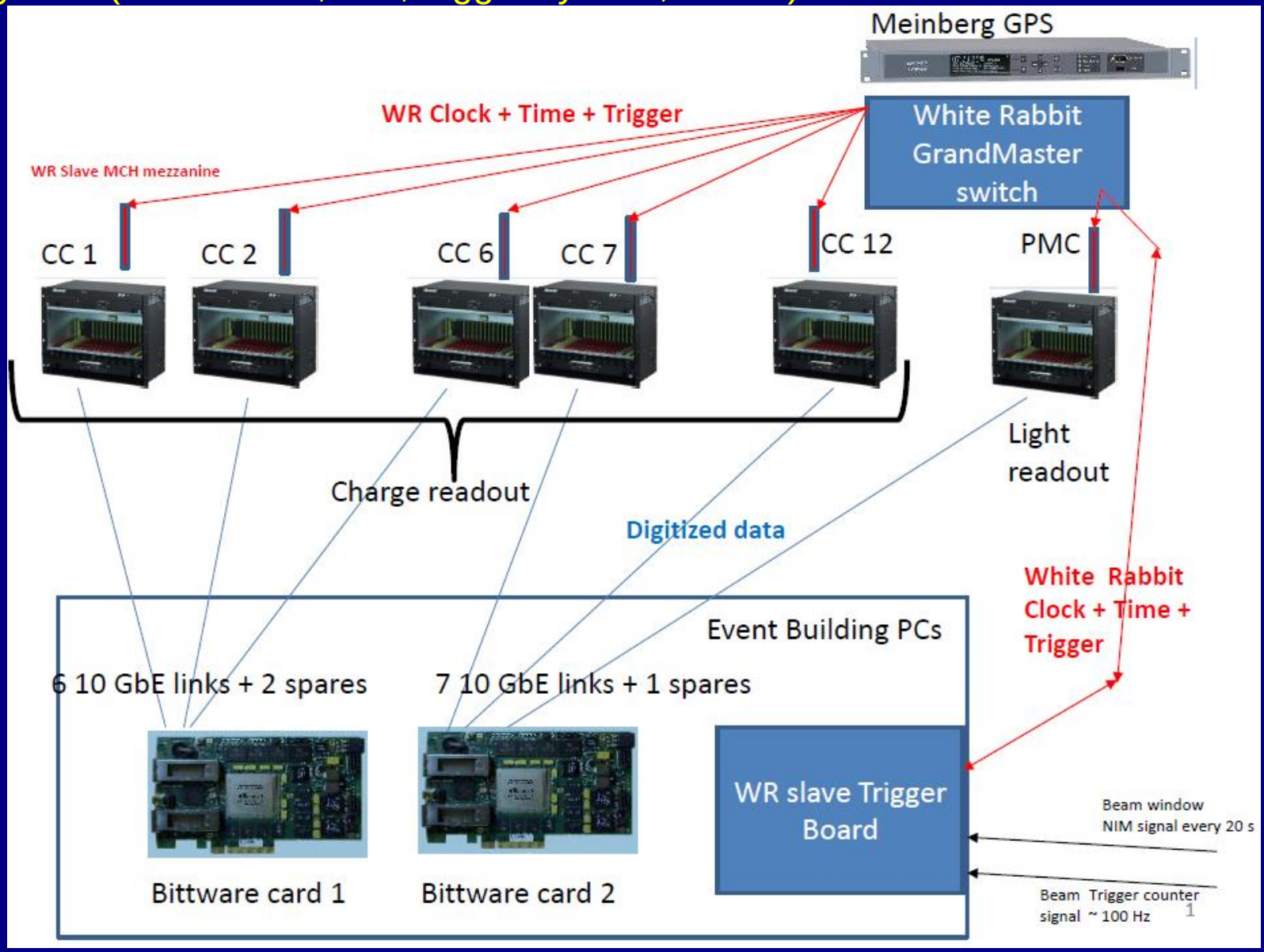
64 channels AMC digitization cards (2.5-25 MHz, 12 bits output, 10 GbE connectivity

- Demonstrator card with 64 ADC channels built and tested in 2015 for the definition of the final card
- Purchase of main components (ADCs, FPGAs, IDT memories) of the final cards by end of 2015 to equip the entire 6x6x6
  - Final design of digitization PCBs May 2016
  - First assembled cards received in August 2016.

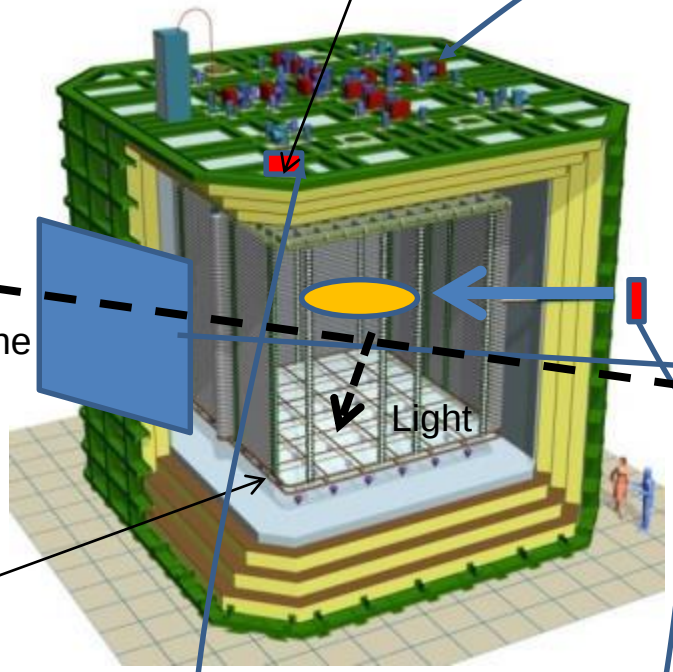
- 20 cards produced by September 2016 to equip the 3x1x1
- Cards production going to be completed with the 2017 budget of remaining 100 FE and uTCA cards for 6x6x6 (main components available)
- The warm flange PCB design is based on an extension of the ones of the 3x1x1

Global uTCA DAQ architecture

integrated with « White Rabbit » (WR) Time and Trigger distribution network
+ White Rabbit slaves nodes in uTCA crates +
WR system (time source, GM, trigger system, slaves)



DAQ timing-trigger integration



uTCA crate of LRO

x12 Charge readout WR links

Trigger counter

Cosmic muon

Start of spill signal (cable)

External trigger plane for cosmics

Light

Crate with NIM logic

PMTs for light readout

Light readout WR link

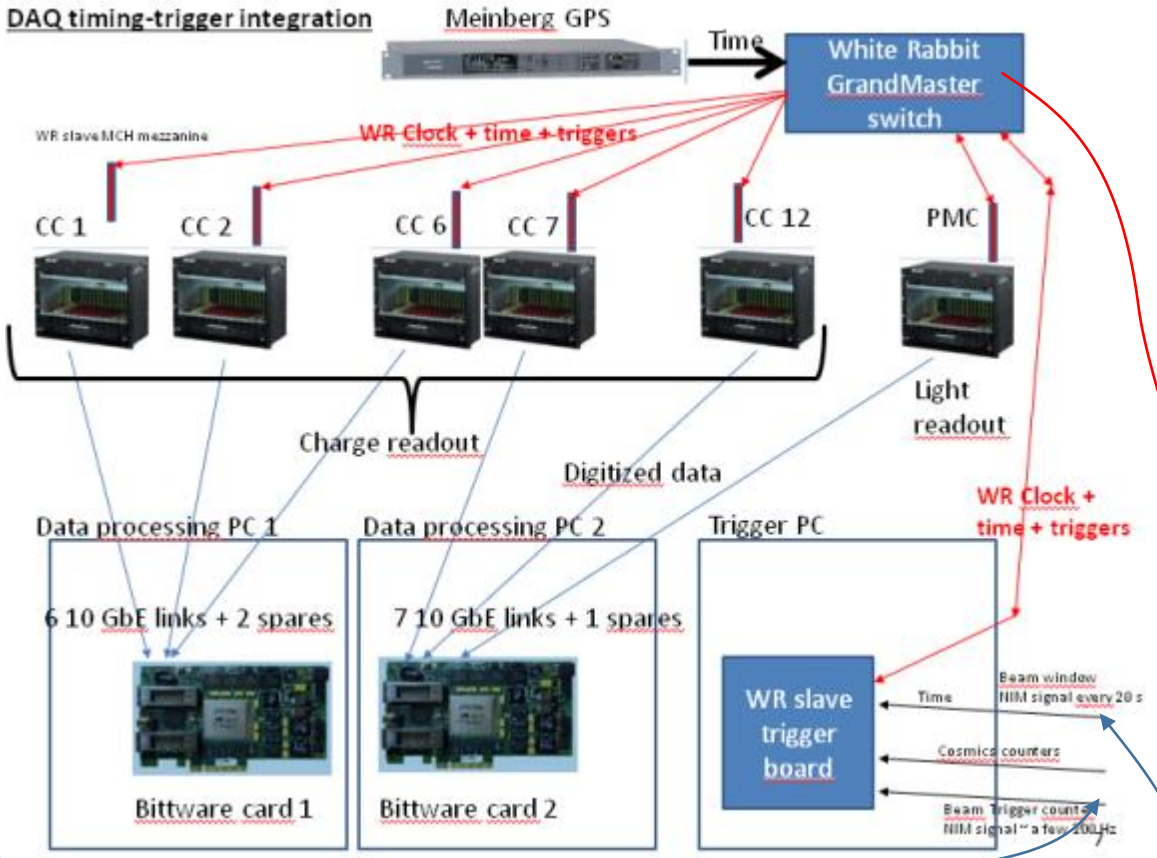
PC with WR time stamping card

Time stamps:

- **Beam trigger**
- **Start of spill**
- **External cosmic trigger**
- **Calibration pulses**

WR switch (optical links 1 Gbps)

Beam triggers from SPS
Tertiary beam line ~100Hz



Beam instrumentation detectors

electrical signals

NIM crate for trigger logic

Beam trigger logic signals

VME crate for beam DAQ

WR card

SPS start of spill

WR network

Beam data output

Beam instrumentation DB

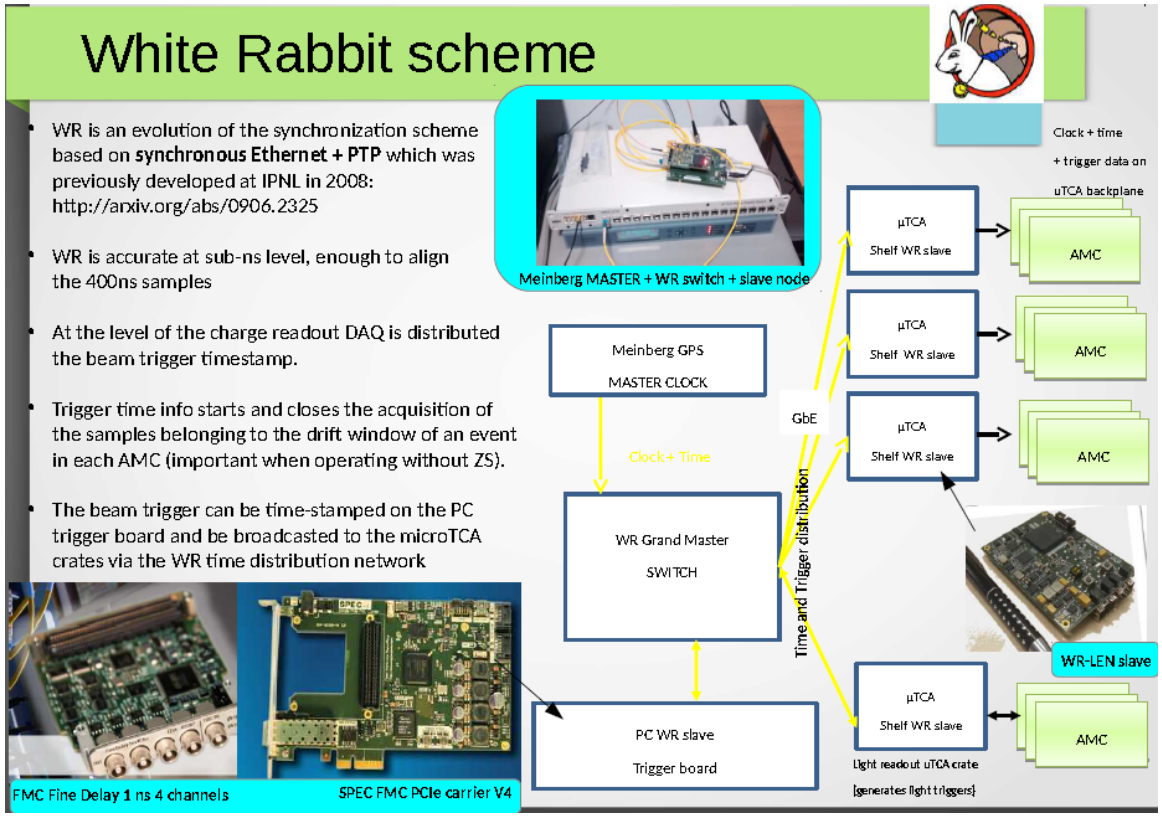
queries

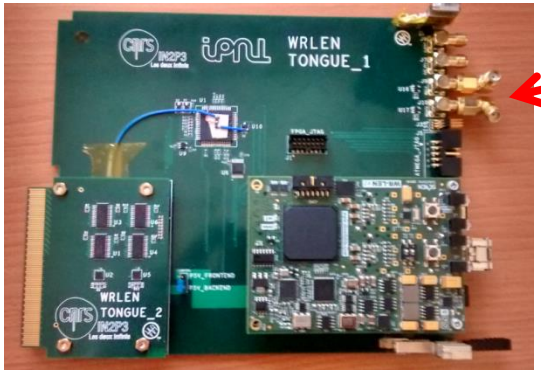
Protune-DP offline or online processing

White Rabbit trigger time-stamping PC (SPEC + FMC-DIO)

White Rabbit Grand-Master

GPS unit



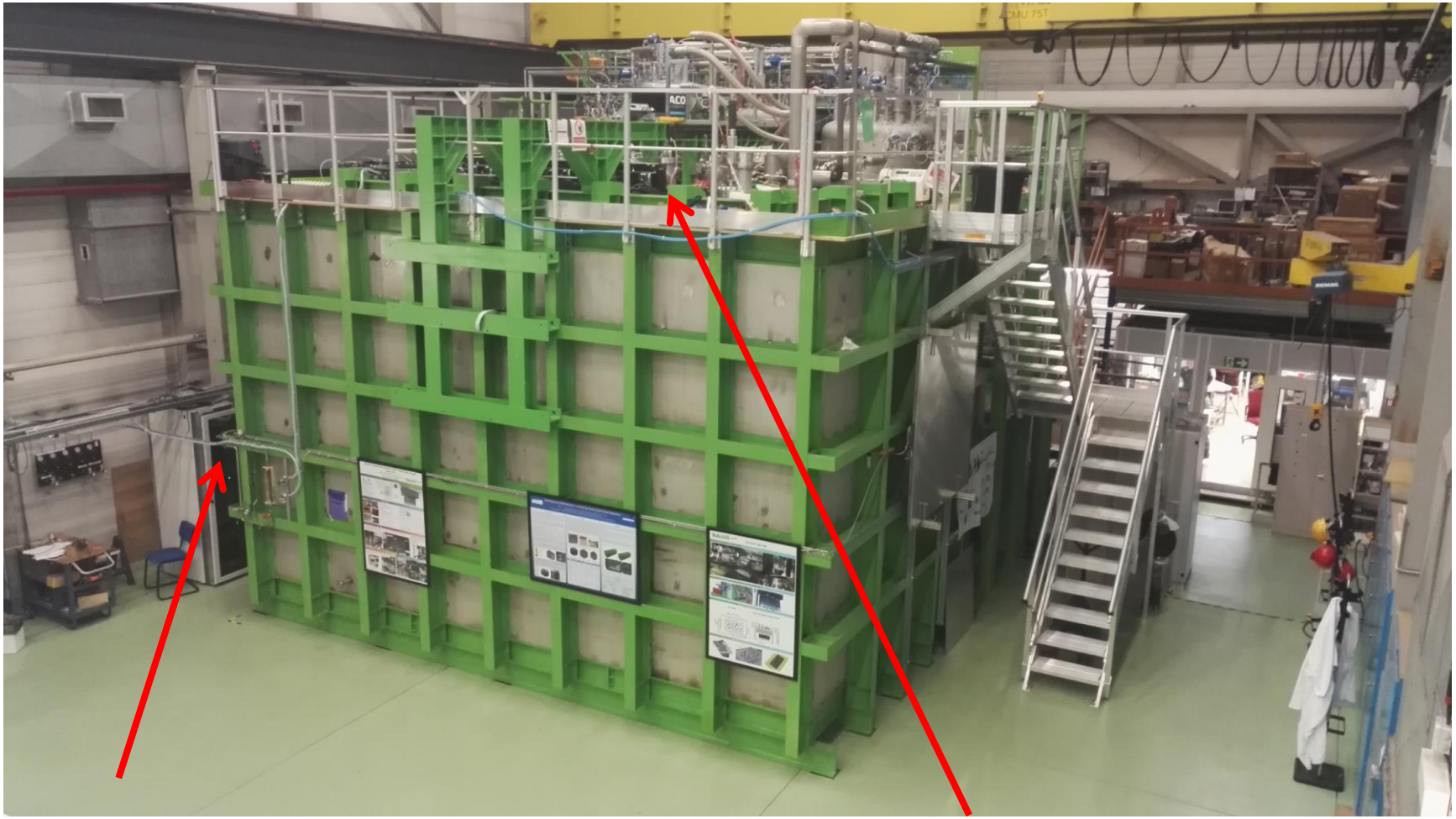


White Rabbit uTCA slave node based on WRLEN developed and produced for entire 6x6x6

Other components of the chain (GPS receiver, WR grandmaster, SPEC+ FMC-DIO + 13 WRLEN) available commercially

6x6x6: 12 uTCA crates (120 AMCs, 7680 readout channels)

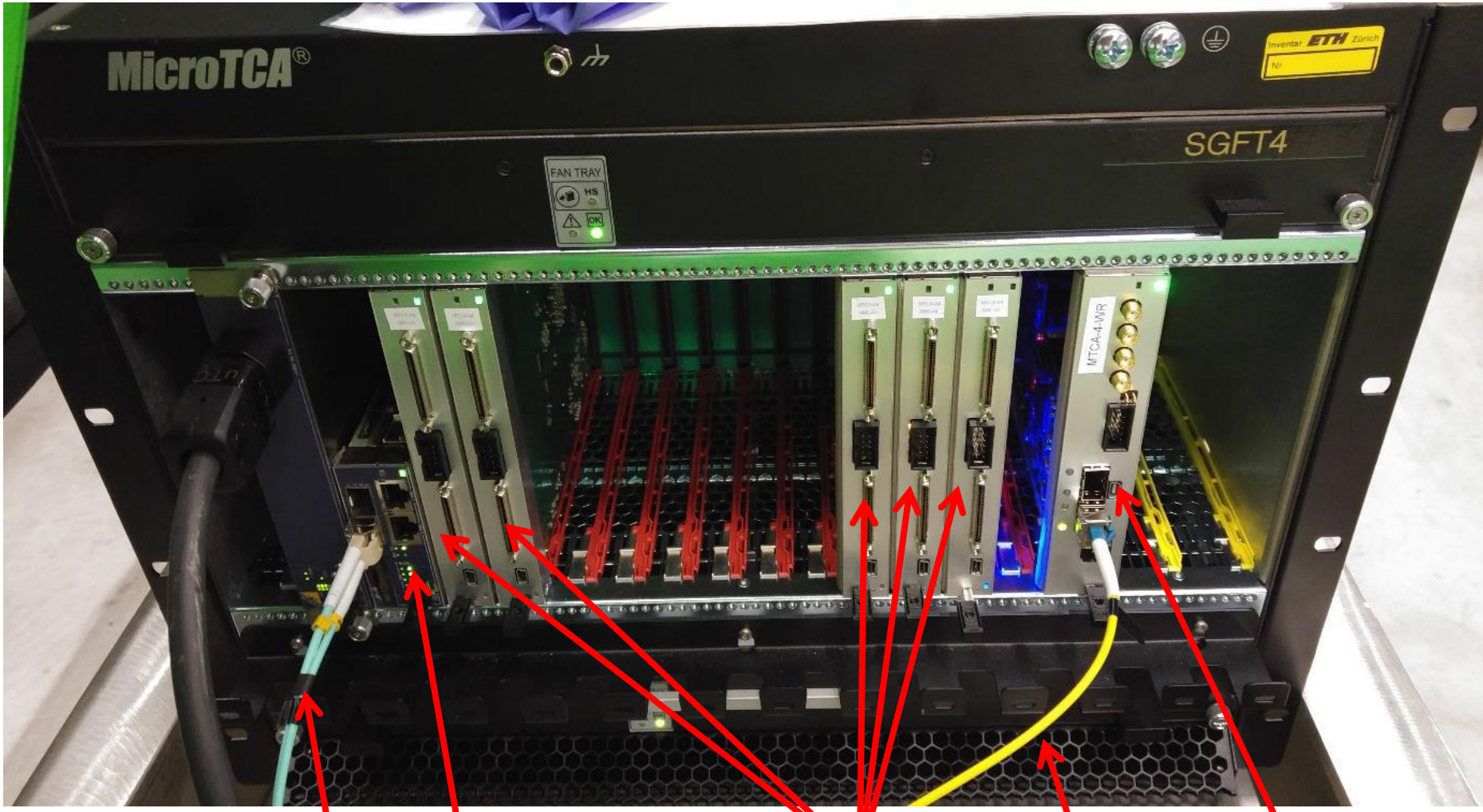
→ 3x1x1: 4 uTCA crates (20 AMCs, 1280 readout channels)



Event builder, network, GPS/White Rabbit GM, WR Trigger PC

Signal Chimneys and uTCA crates

How a crates was looking like before VHDCI signals cabling to the warm flange



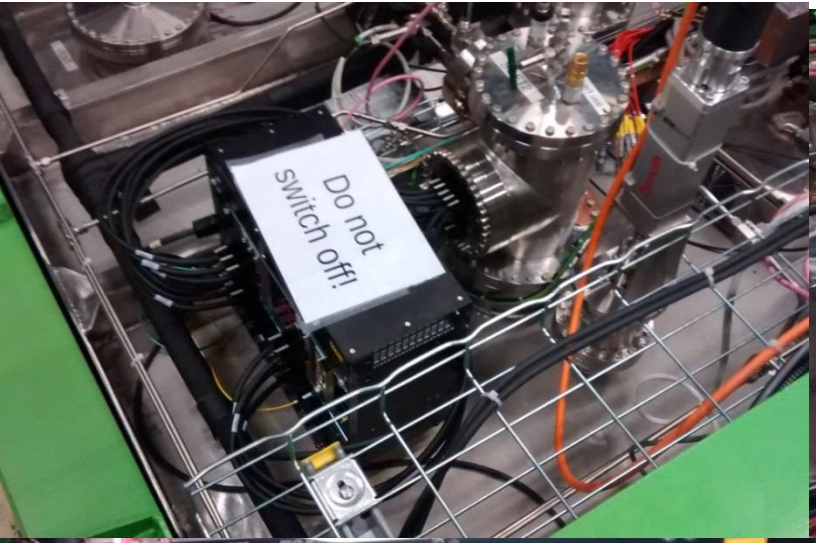
MCH

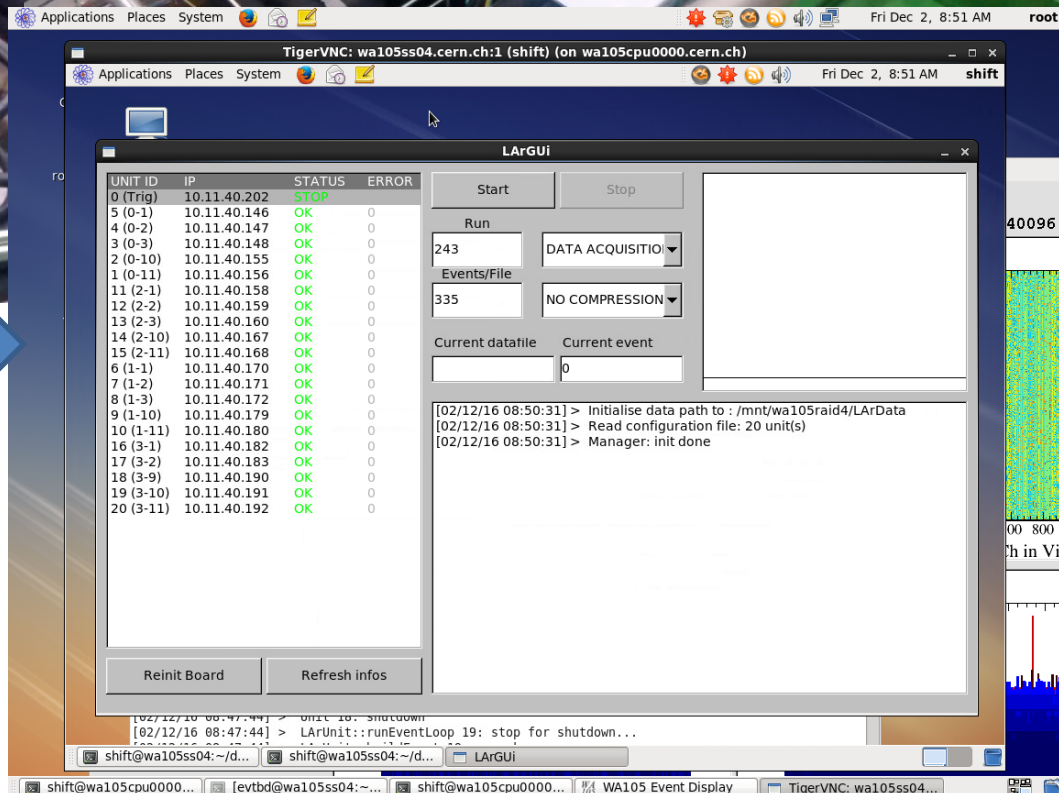
AMC 64 channels digitization cards

WR uTCA slave card node with WRLEN mezzanine

10 Gbit/s data link

White Rabbit optical link



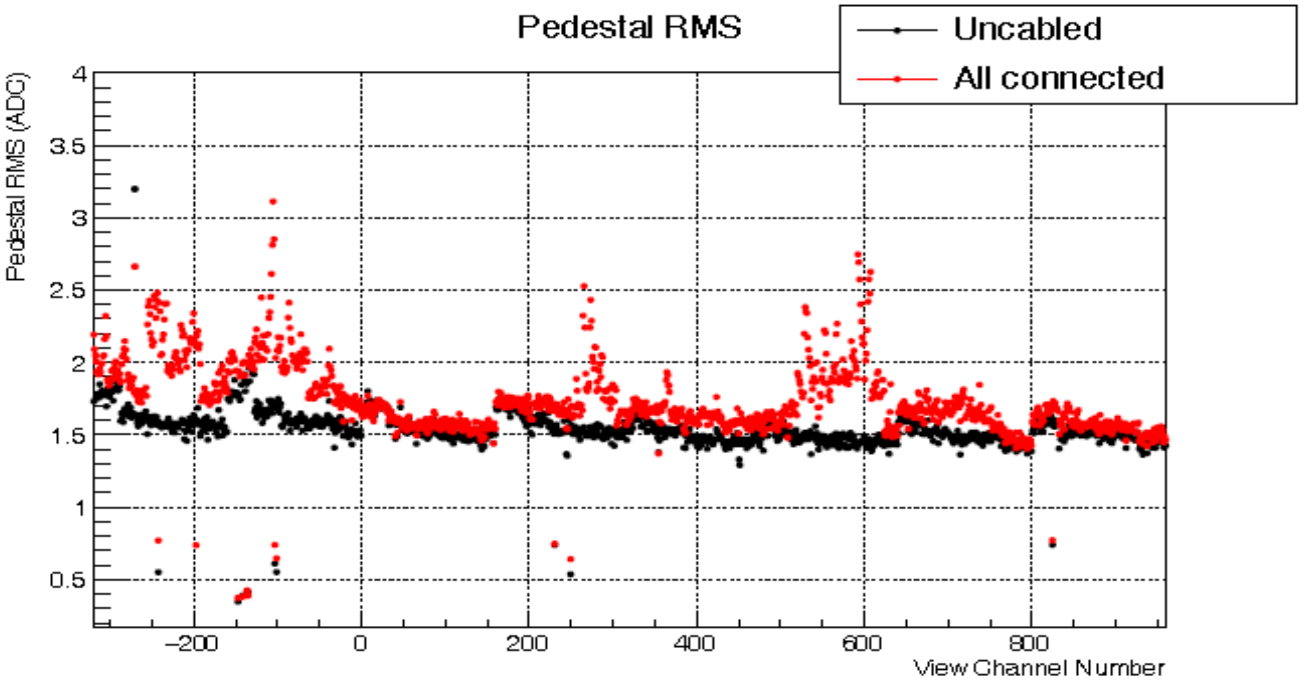


Run control with 20 AMCs

Automatic data processing on online storage/processing farm for purity and gain analysis + data transfer on EOS

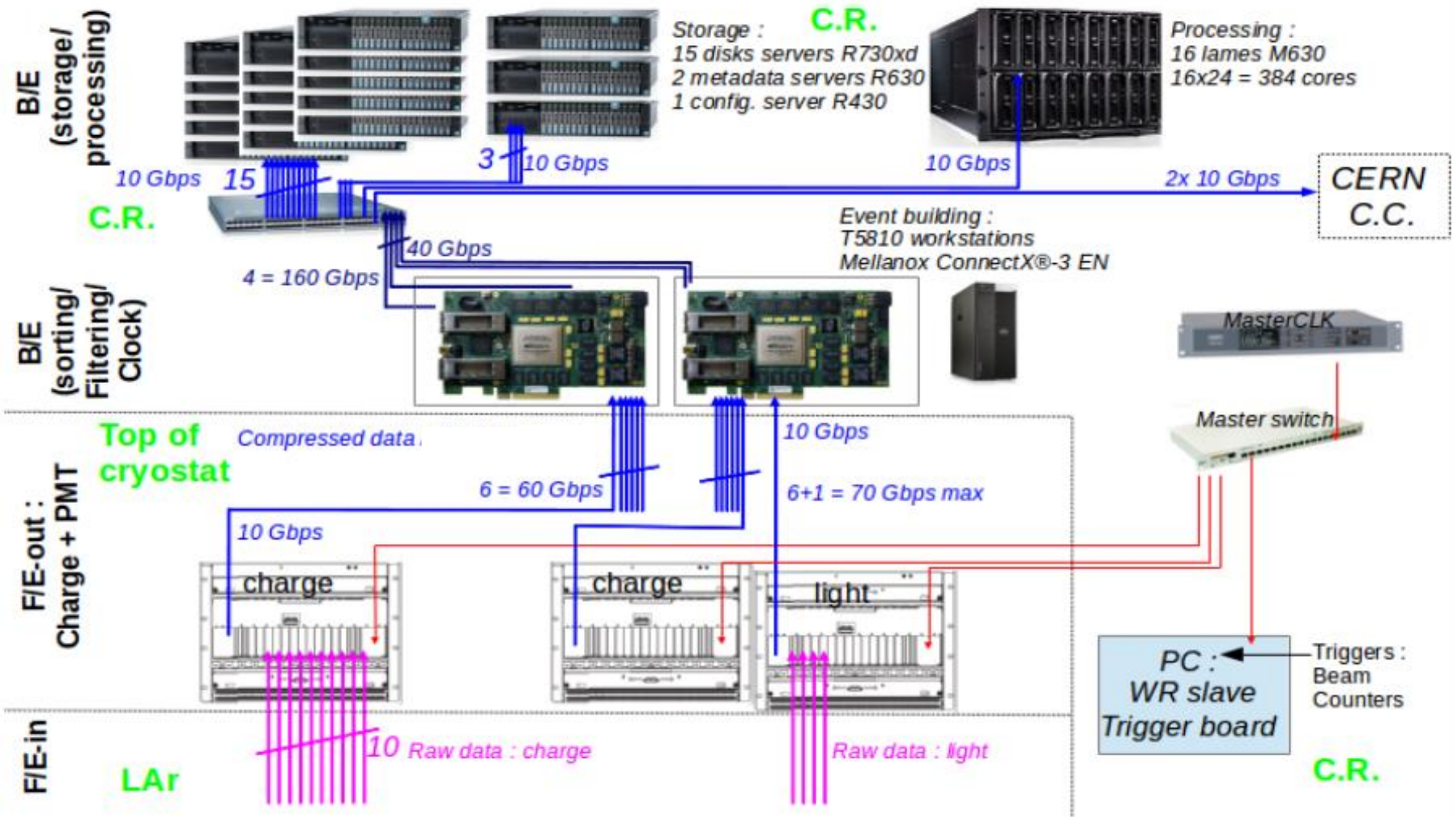
Stable system, noise conditions at warm 1.5-1.7 ADC counts RMS

Several campaigns of checking of the grounding conditions/noise measurements since June 2016.
Good noise conditions with some residual small issues related to slow-control/HV grounding and cabling
→ Average RMS noise 1.7 ADC counts (0.82 mV) at warm with all systems active and cabled 1.5 ADC counts with slow control/HV cables disconnected from flanges



The grounding scheme for the 6x6x6 is more sophisticated with the cryostat, FE electronics and slow control completely insulated from external environment and only referred to cryostat ground.

Online processing and storage facility: internal bandwidth 20 GB/s, 1 PB storage, 384 cores: key element for online analysis (removal of cosmics, purity, gain, events filtering)



C.R. stands for Counting Room

- First design of online storage/processing DAQ back-end farm performed in 2016 (1PB, 300 cores, 20Gb/s data flow),

DELL-based solution : configuration

storage servers :
* 15 R730XD (storage servers) including :
* 16 disks 6To
* 32Go RAM
* 2 disks system RAID 1, 300 Go 10k
* 1 network card Intel X540 double port 10 GB
* 4 years extended guarantee (D+1 intervention)
* 2 processors Intel Xeon E5-2609 v3
* raid H730P
* Rails with management arm
* double power supply

configuration server :
* 1 R430 (configuration server)
* 1 processor E5-2603 v3
* RAID H730
* 2 hard disks 500 Go Nearline SAS 6 Gbps 7,2k
* 16 Go DDR4
* Rails with management arm
* double power supply

Offline computing farm: 16*24 = 384 cores
* 1 blade center PowerEdge M1000e with 16 lames M630, each including :
* 128Go DDR4
* 2 processors Intel Xeon E5-2670 v3
* 4 years extended guarantee (D+1 intervention)
* 2 hard disks 500 Go SATA 7200 Tpm
* netwok Intel X540 10 Gb

metadata servers (MDS) :
* 2 R630 (metadata servers), including :
* 2 disks 200 Go SSD SAS Mix Use MLC 12Gb/s
* 2 processors Intel Xeon E5-2630 v3
* 32Go DDR4
* RAID H730p
* network : Intel X540 2 ports 10 Gb
* 4 years extended guarantee (D+1 intervention)
* Rails with management arm
* double power supply

Switch Force10, S4820T (see next slide) :
* 48 x 10GbaseT ports
* 4 x 40G QSFP+ ports
* 1 x AC PSU
* 2 fans

- Smaller test scale system already installed and operative for 3x1x1

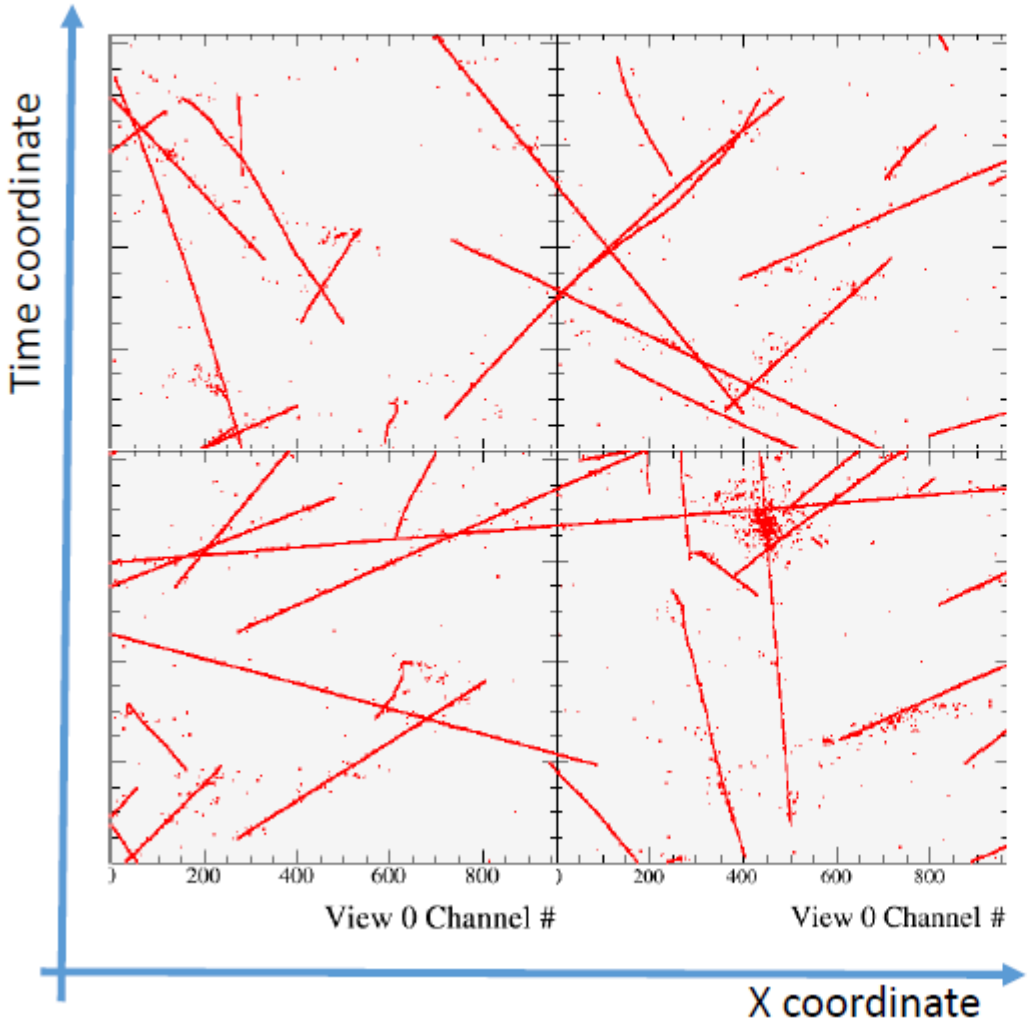
- Tests to finalise the architecture of final online storage/processing facility.

- Thanks to CERN/IT support

Typical event signature for ground surface Liquid Ar TPC operation

For each beam trigger we can have on average 70 cosmics overlapped on the drift window after the trigger (these cosmics may have interacted with the detector in the 4 ms before the trigger and in the 4 ms after the trigger → chopped tracks, “belt conveyor” effect

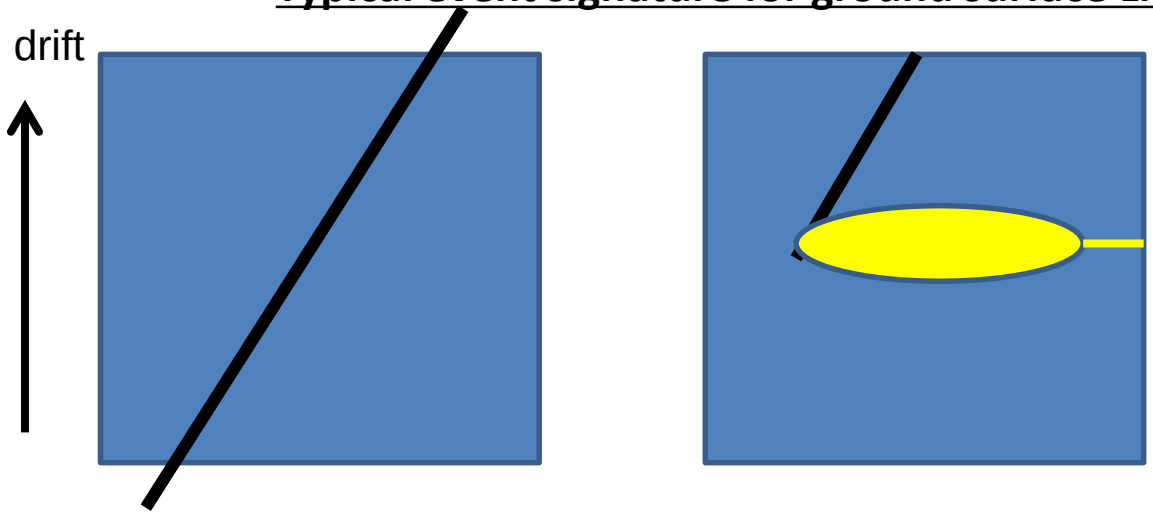
In-spill cosmics in charge data



Example of cosmics only event (in one of the views)

- Red points are reconstructed hits
- TPC is readout in 4 3x3m^2 modules
- After track reconstruction:
  - Attempt to correlate found tracks with light data
  - Remove CR background from beam event
  - Select a subsample of long tracks for calibration purposes

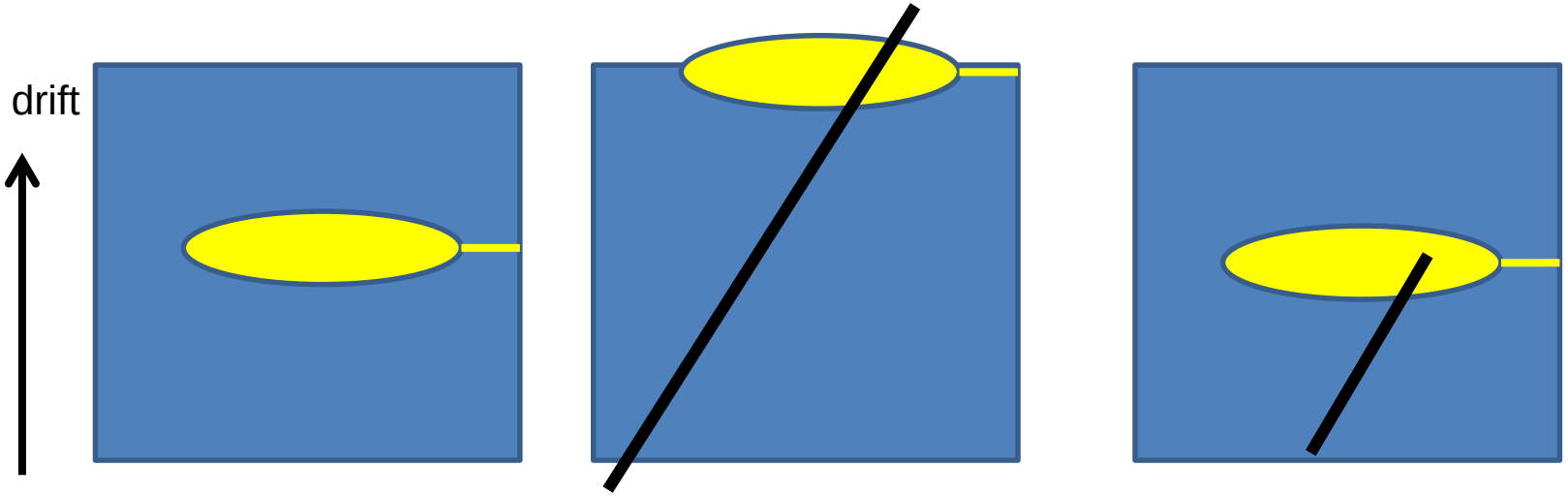
Typical event signature for ground surface Liquid Ar TPC operation



t=beam trigger - 2 ms

t=beam trigger → reconstructed event

The « belt conveyor » effect +- 4 ms around the beam trigger time



t=beam trigger

t=beam trigger + 2 ms

reconstructed event

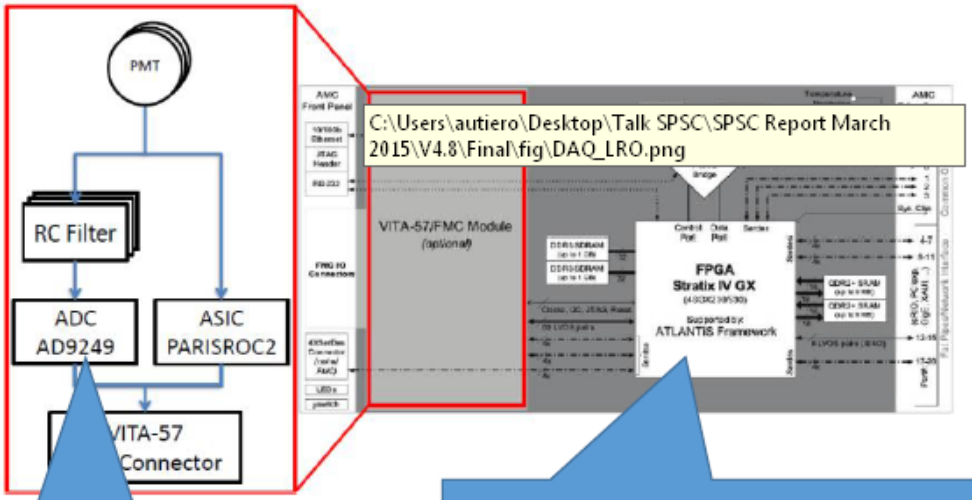
→ During spills it is needed a continuous digitization of the light in the +-4 ms around the trigger time (the light signal is instantaneous and keeps memory of the real arrival time of the cosmics)

→ Sampling can be coarse up to 400 ns just to correlate to charge readout

Light readout electronics

Two modes of acquisition:

- External beam trigger to acquire ±4ms around the spill
- Internal trigger from PARISROC2 ASIC to acquire short time segments



Digitizer: nominally runs at 40 MHz, 14 bits

Digitizer data is buffered in 1G memory buffer connected to FPGA Averaged for a multiple of 40MHz (to reduce the data volume)

→ Sum 16 samples at 40MHz to get an effective 2.5 MHz sampling like for the charge readout

The LRO card has to know spill/out of spill
Out of spill it can define self-triggering light triggers when “n” PMTs are over a certain threshold and transmit its time-stamp over the WR

Conclusions:

- Intensive developments on charge readout and dual-phase during the last years
- Large scale charge readout system already implemented on the 3x1x1 prototype
- Looking forward to the final demonstration with the 6x6x6 protoDUNE-DP at CERN