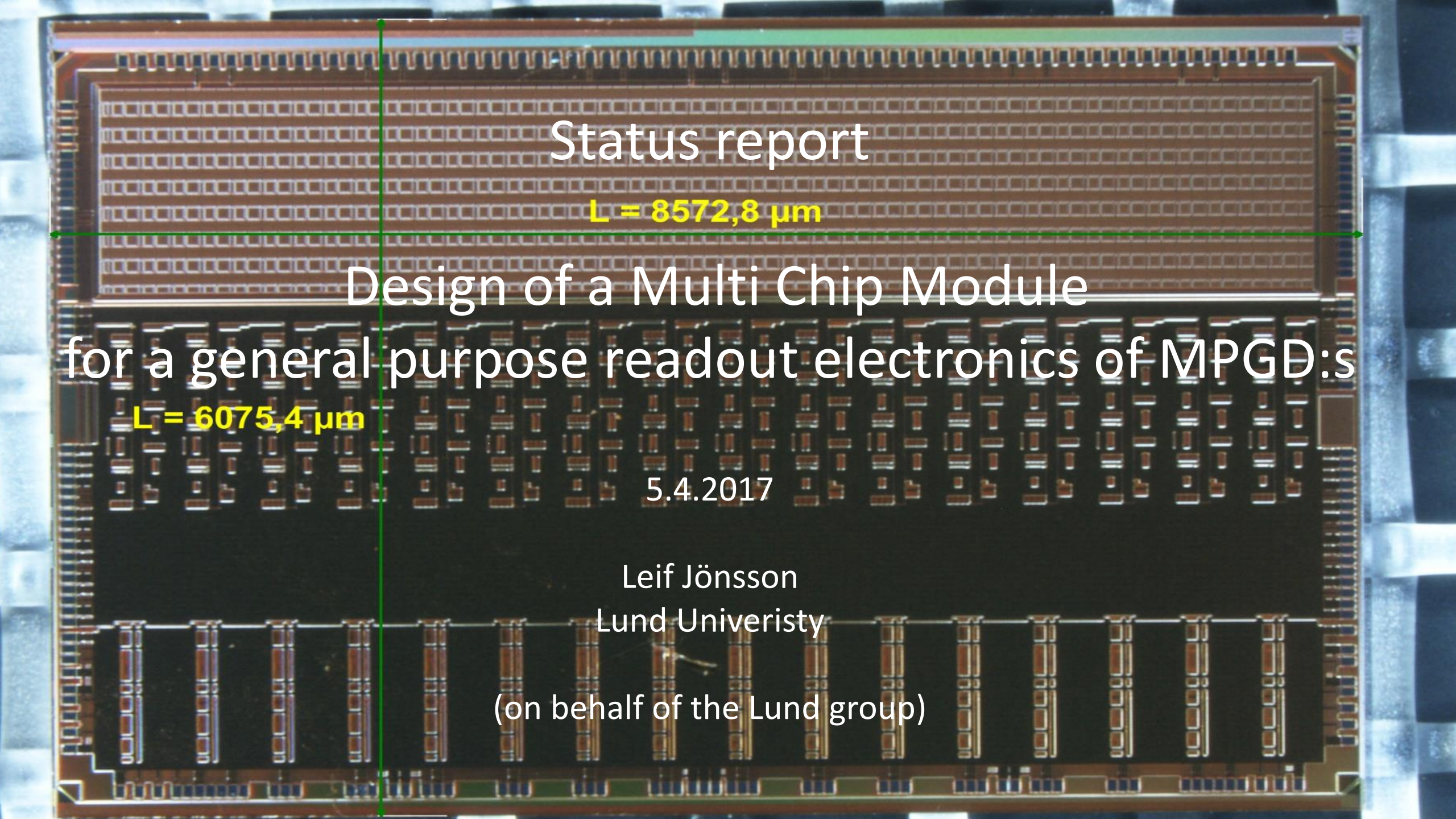

Status report

Design of a Multi Chip Module for a general purpose readout electronics of MPGD:s

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Leif Jönsson
Lund Univeristy

(on behalf of the Lund group)

The goal of the full project: Construct a TPC with excellent position resolution and two-track separation.
This requires: Small readout pads (<= 1x6 mm2).
The channel density of the readout electronics has to match the small pad size.

- The 'proof-of-princple' has been demonstrated and the project is now in the 'feasibilty phase', the aim of which is to produce front-end electronics comparable in size to the readout pads.
- This readout electronics can be used in smaller MPGD-detectors for applications in various other fields like medical diagnostics , material science at XFEL, and for investigations at ESS.

- The readout electronics is based on the SALTRO16 ASIC, which integrates the analogue and digital processing in the same chip.
- The size of the die itself is 8.7x6.2 mm^2, which corresponds to a channel occupancy of 3.37 mm^2/channel.

- As this project was started it was not possible to find a company which could package the SALTRO ASIC in a small enough capsule to satisfy our requirement.

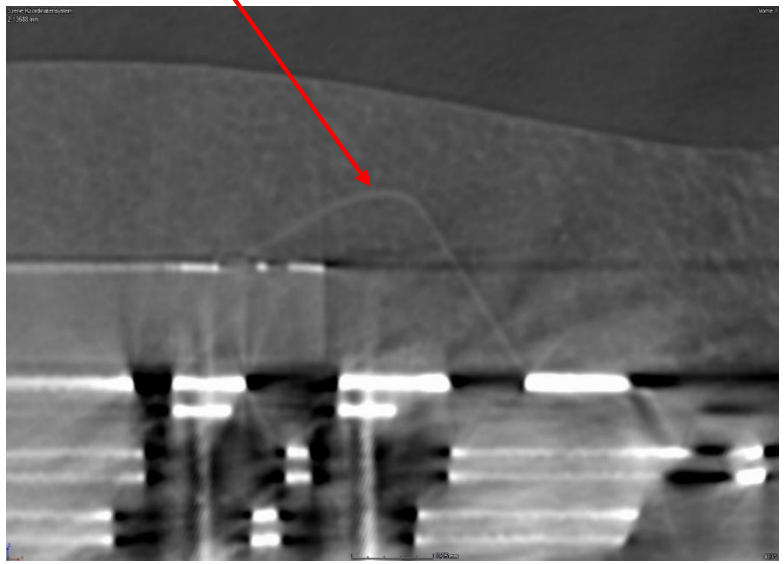
$\Rightarrow$ We decided to go for a 'chip-on-board' solution.

$\Rightarrow$ We developed a carrier board onto which the SALTRO ASIC was bonded and covered with an epoxy glob to protect the ASIC and the bonding wires. The size of the carrier board is 12x8.9 mm^2. Eight of these carrier boards should be mounted on a Multi-Chip-Module (MCM) board, which also contained a CPLD, connectors and passive components. This increases the channel occupancy to 6.4 mm^2/channel

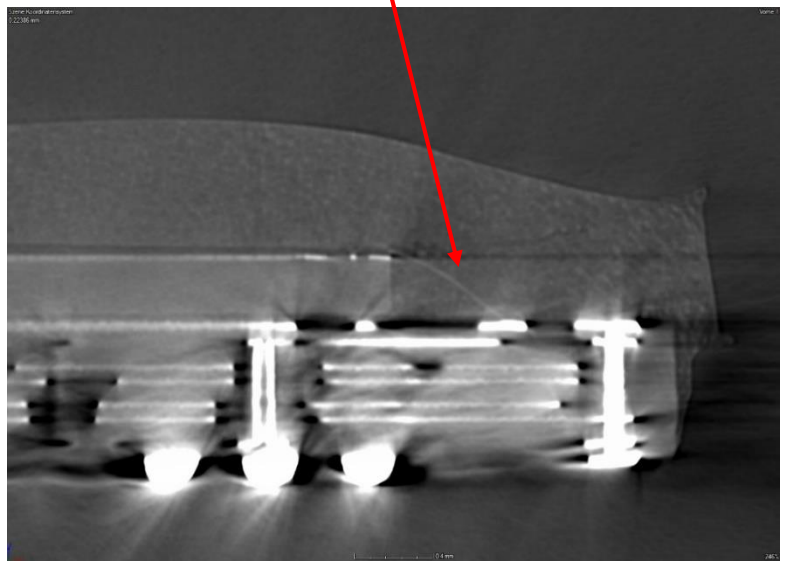
Outcome: After some initial problems had been sorted out, the Swedish company managed to bond one ASIC on a Carrier board, where all connections were verified, also after application of the epoxy glob and the soldering balls.

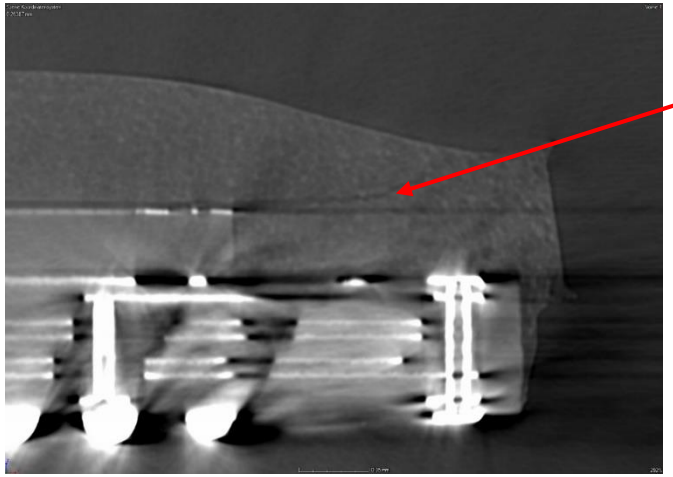
However, as the carrier board had been soldered onto an adaptor board for characterization, some areas had lost connection.
X-ray investigations showed the following:

Normal bonding loop

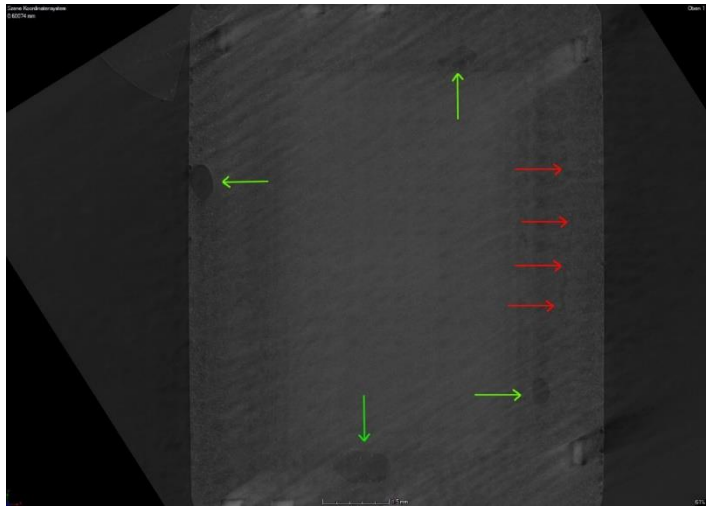


Bond wire without a significant loop





Cracks in the epoxy (red arrows in the right hand side picture) and air bubbles (green arrows in the right hand side picture).



Conclusion:

- There is nothing indicating an error in the design of the carrier board.
- The lost connections are due to the different expansions of the PCB and the epoxy material in the soldering process, which causes breaks in those wires where the wire loop is not sufficiently high.
- Another disadvantage of this method is that the surface of the epoxy layer is not flat enough to provide efficient cooling.

- Through contacts with CERN we were directed to three companies , which are able to offer packaging in small enough capsules. After intense communication with these companies and careful evaluation we at the end signed a contract with NovaPack in Grenoble for a pre-serie of 25-30 chips. This happened on the 16th of February 2017.

- The chips from the pre-serie will be used for characterization before the production order. The total sample is about 840 SALTRO ASIC:s.

- NovaPack has started the substrate design and this is expected to be completed by the end of week 15 (April 10-14).

- After that they will submit the CAD file for review by us.

- As we have approved the design the lead time will be about 6-7 weeks to get the substrates plus bout 2 weeks to deliver the initial packages.

⇒ In the middle of June we can expect the first parts.

⇒ Characterization of the chips can start

- In the mean time we have started to prepare the test set-up.

- The MCM-board is a very dense board and not ideal for characterization of the chips.

- We have therefore produced a Development Board, in a size suitable for lab work.

- It is a stand alone board, containing only one SALTRO-chip in TQFP package and a CPLD for control of the data handling but also the necessary voltage regulators.

- Several test points and connectors allow for connection to a logic analyzer.

- Data will be read out by serial readout over a 40 MHz DTC link connecting the MCM board (alternatively the Development Board) and an SRU (Scalable Readout Unit). Data will be processed by a PC

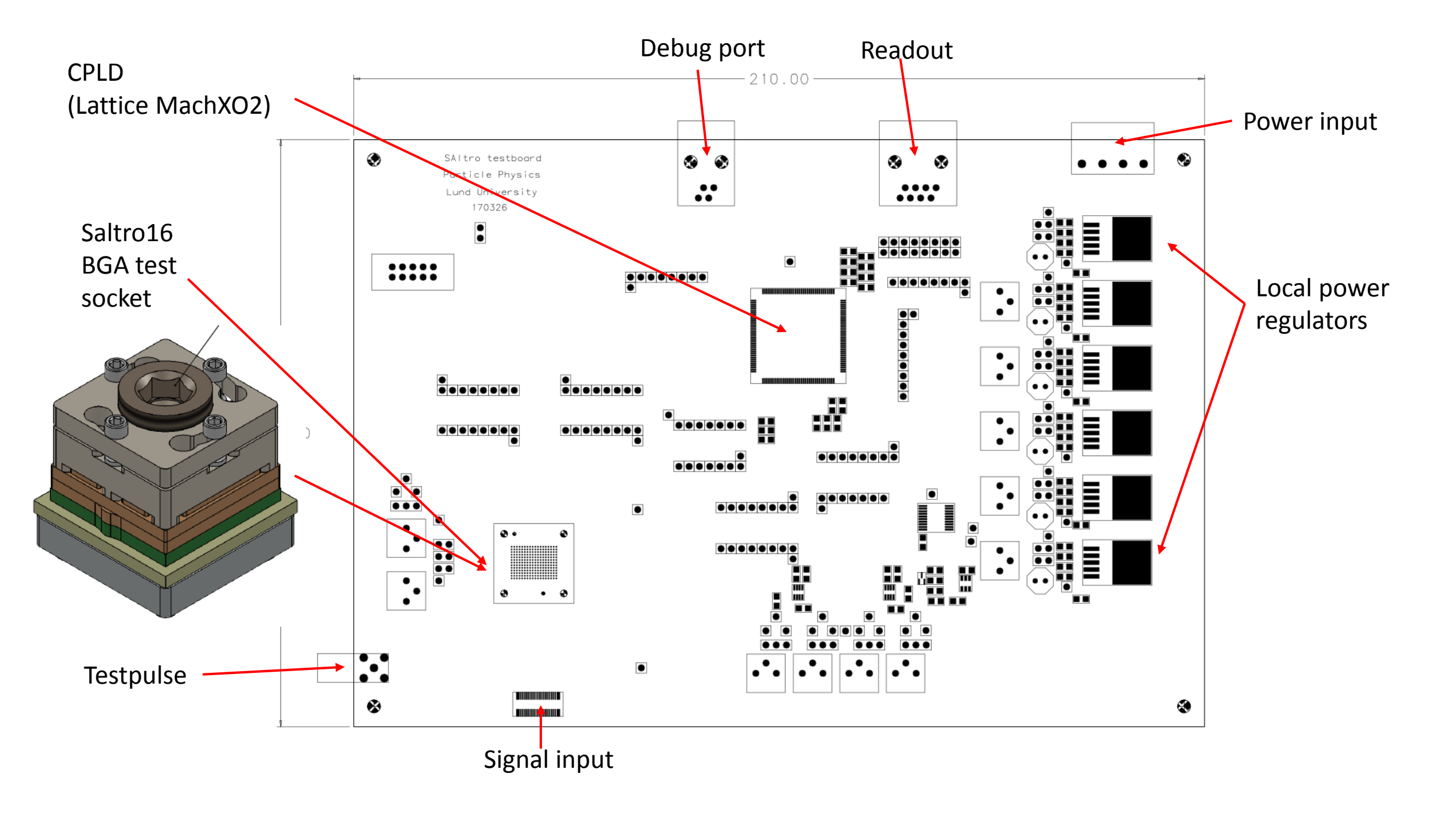
- The Development Board has been used to test the FPGA firmware and to establish the communication between the SALTRO16-chip in the TQFP package and the SRU.

- The firmware of the CPLD (on the Development Board) is taken from the ALICE experiment and the firmware for the SRU is using the ALICE and TOTEM systems.
A master student is working on the modification and further development to meet our requirements.

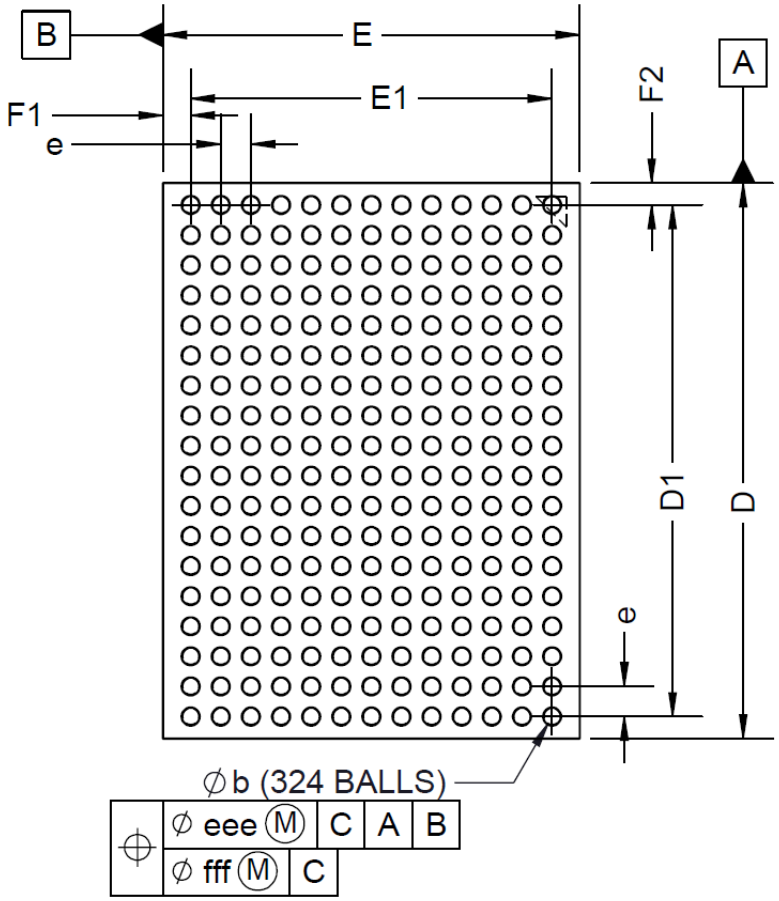
- The PC DAQ is based on the EUDET TPC ALTRO DAQ, modified to handle Ethernet/UDP.

The Development Board now has to be modified to enable test of the ASIC:s packaged in capsules of size 12x9 mm^2 and to adapt to the substrate design.

- Single Saltro16 readout in a BGA ZIF (zero insertion force) test-socket
- Same CPLD & connections as in final circuit
- Same power distribution
- Test-points on all signals
- 8-layer board 210x145mm
- No impedance control, no signal timing/length matching
- HDI design because of BGA footprint (buried 0.1mm vias)
- 3 signal layers, 5 power layers


CPLD
(Lattice MachXO2)
Debug port
Readout
Power input
Saltro16
BGA test
socket
Local power
regulators
Testpulse
Signal input
210.00
SAltro testboard
Particle Physics
Lund University
170326

BGA package



	MIN	NOM	MAX
A			1.70
A1	0.18		
A2		1.08	
A3		0.28	
b	0.30	0.35	0.40
D	11.85	12.00	12.15
D1		11.05	
e		0.65	
E	8.85	9.00	9.15
E1		7.80	
F1		0.60	
F2		0.475	
ddd			0.10
eee			0.15
fff			0.08

Saltro16 ballpad connections

	1	2	3	4	5	6	7	8	9	10	11	12	13	
A	PasaTestP	Shutdown	PasaTestN	AdcTestP	RefN	Vcm	CmOut	chipadd [1]	chipadd [3]	adc_add0	l2yb	ack_en	tstout	A
B	TestMode	PreampMode	BiasDecay	AdcTestN	VddAdcA	RefP	BiasGate	chipadd [0]	chipadd [2]	adc_add1	trgb	ackb	bd [00]	B
C	InCDM15	VddPasaA	VddPasaA	VddAdcA	VddAdcA	GndAdcDig	VddAdcDig	VDD	VDD	tsm	bd [01]	bd [02]	bd [03]	C
D	InCDM14	VddPasaA	VddPasaA	VddAdcA	GndAdcA	GndAdcDig	VddAdcDig	VDD	GND	DVDD	bd [04]	bd [05]	bd [06]	D
E	InCDM13	VddPasaA	GndPasaA	VddAdcA	GndAdcA	GndAdcDig	VddAdcDig	GND	DVSS	DVDD	bd [07]	bd [08]	bd [09]	E
F	InCDM12	VddPasaA	GndPasaA	VddAdcA	GndAdcA	GndAdcDig	VddAdcDig	GND	DVSS	DVDD	bd [10]	bd [11]	bd [12]	F
G	InCDM11	VddPasaA	GndPasaA	GndPasaA	GndAdcA	GndAdcDig	VddAdcDig	DVSS	DVSS	DVDD	scan ena	bd [13]	bd [14]	G
H	InCDM10	VddPasaA	GndPasaA	GndPasaA	GndAdcA	GndAdcDig	VddAdcDig	DVSS	DVSS	DVDD	bd [15]	bd [16]	bd [17]	H
J	InCDM9	VddPasaA	GndPasaA	GndPasaA	GndChipGuard Ring	GndAdcDig	VddAdcDig	DVSS	DVSS	DVDD	bd [18]	bd [19]	rdoclk	J
K	InCDM8	VddPasaA	GndPasaA	GndPasaA	GndChipGuard Ring	GndAdcDig	VddAdcDig	DVSS	DVSS	DVDD	bd [20]	bd [21]	bd [22]	K
L	InCDM7	VddPasaA	GndPasaA	GndPasaA	GndAdcA	GndAdcDig	VddAdcDig	DVSS	DVSS	DVDD	bd [23]	bd [24]	bd [25]	L
M	InCDM6	VddPasaA	GndPasaA	GndPasaA	GndAdcA	GndAdcDig	VddAdcDig	DVSS	DVSS	DVDD	ScanMode	bd [26]	bd [27]	M
N	InCDM5	VddPasaA	GndPasaA	GndPasaA	GndAdcA	GndAdcDig	VddAdcDig	GND	DVSS	DVDD	bd [28]	bd [29]	bd [30]	N
P	InCDM4	VddPasaA	GndPasaA	VddAdcA	GndAdcA	GndAdcDig	VddAdcDig	GND	DVSS	DVDD	bd [31]	bd [32]	bd [33]	P
R	InCDM3	VddPasaA	VddPasaA	VddAdcA	GndAdcA	GndAdcDig	VddAdcDig	VDD	GND	DVDD	bd [34]	bd [35]	bd [36]	R
T	InCDM2	VddPasaA	VddPasaA	VddAdcA	VddAdcA	GndAdcDig	ClkSelect	VDD	VDD	SoftRst	bd [37]	bd [38]	bd [39]	T
U	InCDM1	Gain1	ShapingTime1	ShapingTime3	Vcm	CmOut	ClkAux	chipadd [4]	chipadd [5]	cstbb	grstb	writeb	dolo_en	U
V	InCDM0	Gain2	ShapingTime2	Polarity	RefN	RefP	sclk	chipadd [6]	chipadd [7]	trsf_en	trsfb	errorb	dstb	V
	1	2	3	4	5	6	7	8	9	10	11	12	13	

Status of the DAQ system:

The CPLD: The firmware is written and has been tested.

The SRU: For the firmware a lot is already done.
⇒ we can read/write SALTRO and CPLD registers.
⇒ we can send software tiggers to the SALTRO.
⇒ we can read partial event data.

Still to do: The memory management on the SRU to read full events still has to be optimized.
A hardware trigger to the SRU:s has to be implemented.

The detector control between the MCM and SRU is ready and has been tested.
The readout to the PC is partly implemented.

Still to do is: ⇒ define data format
⇒ test the full readout of the Development Board, the max data rate and the trigger rate

The PC DAQ: The modification of the ALTRO DAQ is in progress.
The detector control between the SRU and PC is mostly done and partly tested.

Still to do: ⇒ Some intermittent problems on the SRU still have to be solved
⇒ Everything has to be tested

Readout of the Development Board:

⇒ The simple stand alone data reciever is ready.
⇒ The implementation into the DAQ system has to be done.

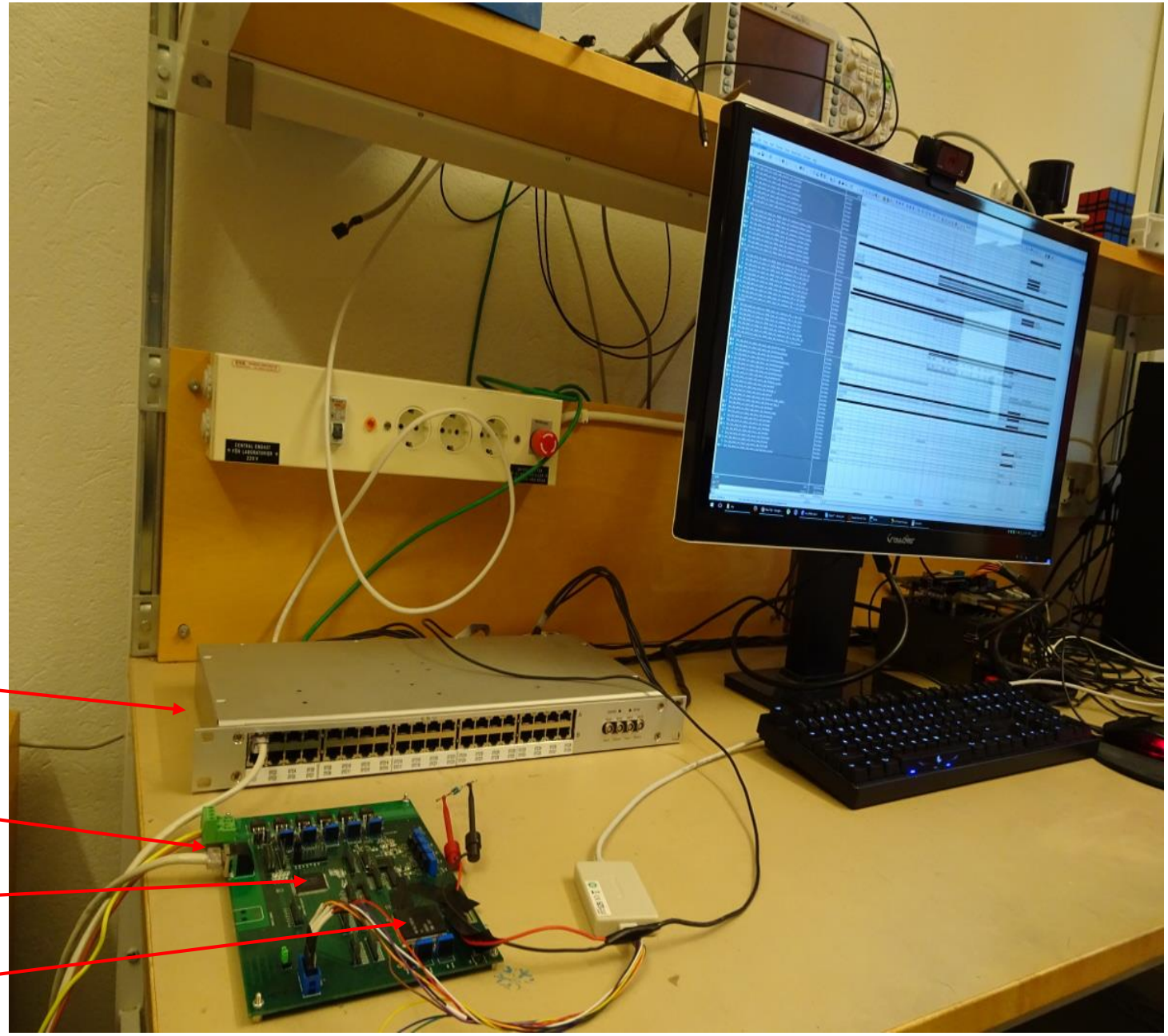
Trigger handling:

⇒ The trigger handling has to be implemented.

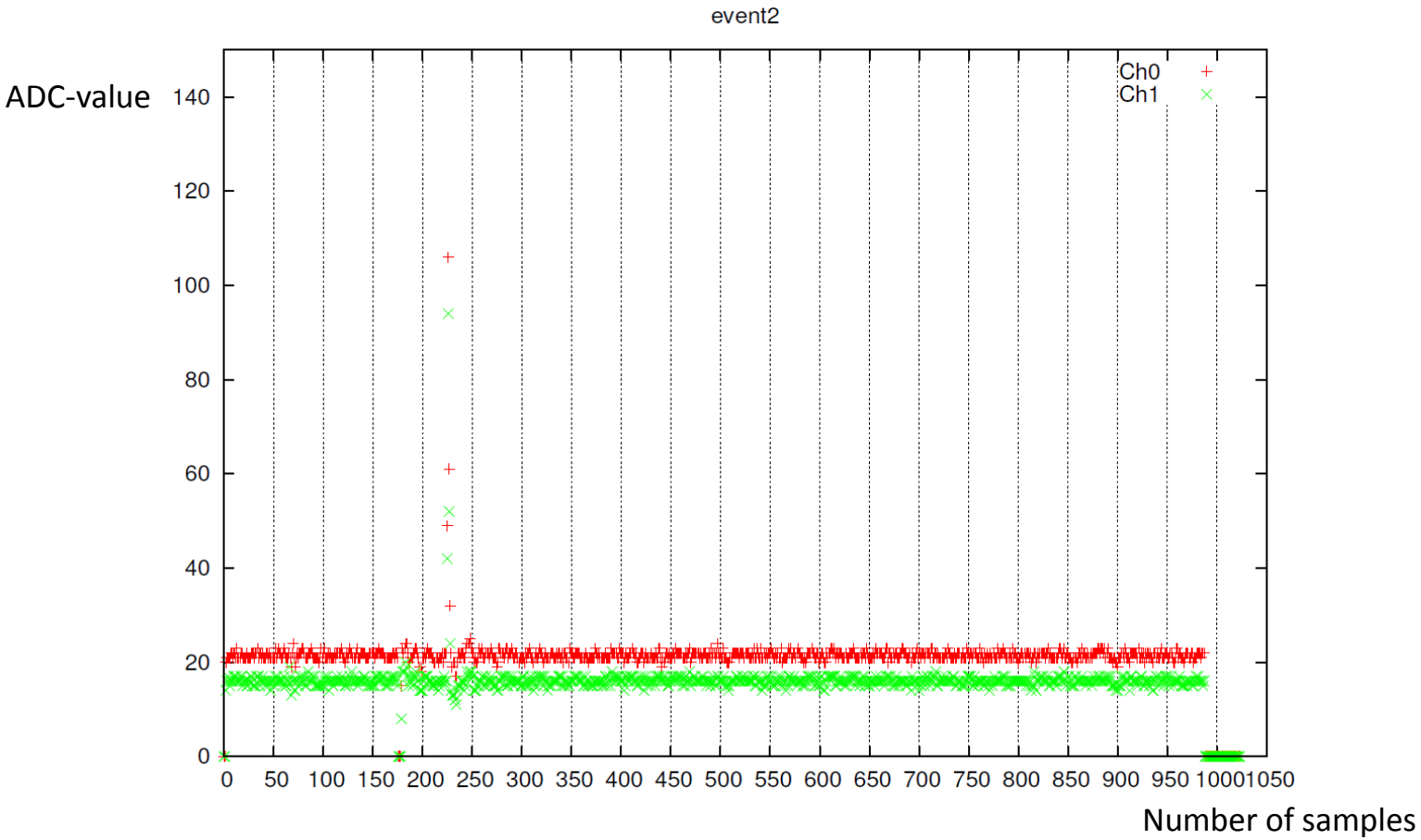
Monitor and run control:

⇒ This is the same as in the ALTRO DAQ.
⇒ The slightly different data format has to be implemented.

The development set-up



Event with two channels fully read (0 and 1) from the Development Board, the peak is induced by a generated pulse from the SRU.
If reading all channels only 180 samples can currently be read, one must rearrange the memory management on the SRU for full readout (to be done).
The standalone data receiver was used (to be implemented in PC DAQ).



Towards the final system

The CPLD has to be tested with 8 chips on the MCM board.

For the SRU the following things have to be done:

- ⇒ Implement handling of up to 40 MCM boards.
- ⇒ Implement a memory manager for reading full events with up to 1000 samples.
- ⇒ Implement resending of lost Ethernet/UDP data packets.
- ⇒ Implement power pulsing.
- ⇒ Implement clock synchronization between multiple SRU:s.
- ⇒ Implement the trigger system.

For the PC DAQ the following things have to be done:

- ⇒ Implement handling of multiple SRU:s.
- ⇒ Implement handling of 40 MCM boards per SRU.
- ⇒ Implement an interface to a common DAQ.
- ⇒ Implement the trigger handling.

Summary

- The packaging of the SALTRO16 ASIC:s is underway. Delivery of the preseries is expected mid June.
- The design of the MCM Development Board is ready and will be scrutinized before the PCB is ordered.
- The Test Socket is ordered and delivery is expected on April 25.
- A first version of the DAQ system enables readout of data but further development will be done to improve it