Design and submission of the RD53A chip

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AIDA-2020 2nd Annual Meeting

4-7 April 2017 – LPNHE, Paris

Outline

- RD53 – Challenges & Goals
- The RD53A demonstrator: overview and floorplan
- Analog front-end design
- Status and Conclusions

RD53 – An overview

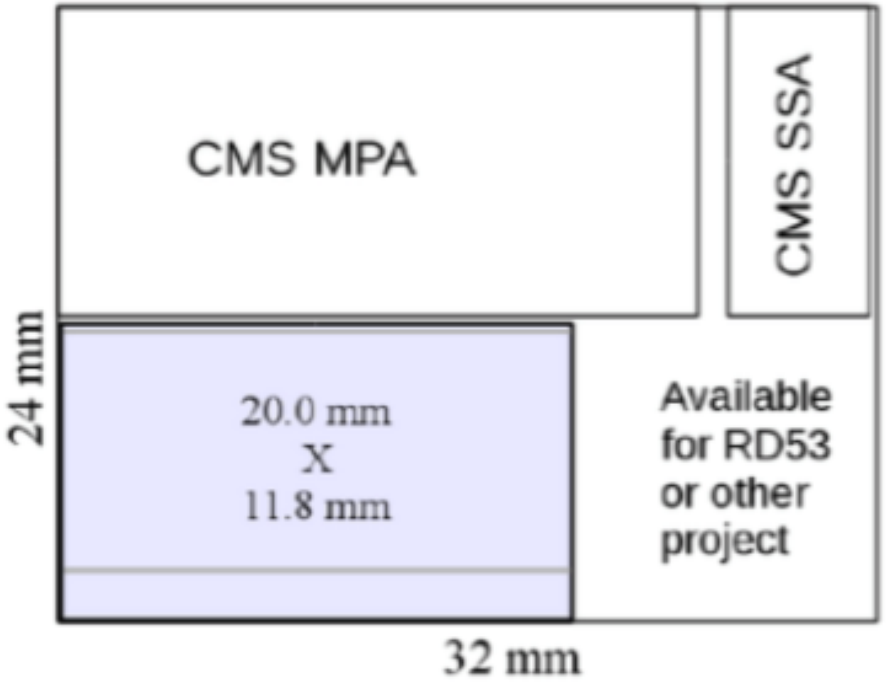
- Focused R&D program aiming at the **development of pixel chips** for ATLAS/CMS **phase 2 upgrades**
- 19 institutions from Europe and US
  - Bari, Bergamo-Pavia, Bonn, CERN, CPPM, Fermilab, LBNL, LPNHE Paris, Milano, NIKHEF, New Mexico, Padova, Perugia, Pisa, Prague IP/FNSPE-CTU, RAL, Seville, Torino, UC Santa Cruz.

- **65 nm CMOS** is the common technology platform
- RD53 Goals:
  - Detailed understanding of **radiation effects** in 65nm → guidelines for radiation hardness
  - Development of **tools and methodology** to efficiently design large complex mixed signal chips
  - Design of a **shared rad-hard IPs library**
  - Design and characterization of common engineering run with **full sized pixel array chip**

RD53A - Large Scale prototype

- The efforts of the RD53 collaboration are leading to the submission of the RD53A chip
- 400 x 192 pixel, 50um x 50um pixel, 20mm x11.8mm chip
- Goal: demonstrate in a large format IC
  - suitability of **65nm technology** (including radiation tolerance)
  - **high hit rate**: 3 GHz/cm^2
  - **trigger rate**: 1 MHz
  - **Low threshold operation** with chosen **isolation** strategy and **power distribution**

- Not intended to be a production chip
  - will contain design variations for testing purposes (with **3 different versions of the analog very front-end)**
  - wafer scale production will enable prototyping of bump bonding assembly with realistic sensors in new technology



- **Final design almost ready**
- **Submission: May 31, 2017**

RD53A main specifications

From the Spec. document **http://cds.cern.ch/record/2113263**

- **Hit rate:** up to 3 GHz/cm^2 (75 kHz pixel hit rate)
- **Detector capacitance**: < 100 fF (200 fF for the edge pixels)
- **Detector leakage**: 10 nA (20 nA for the edge pixels)
- **Trigger rate**: max 1 MHz
- **Trigger latency**: 12.5 us
- **Low threshold**: 600 e- → severe requirements on noise and dispersion
- **Min. in-time overdrive**: < 600e-
- **Noise occupancy**: < 10^{-6} (in a 25ns interval)
- **Hit loss @ max hit rate**: 1%
- **Radiation tolerance**: 500 Mrad @ -15° C

Radiation tolerance

- RD53A should be able to withstand with radiation dose levels at least **up to 500 Mrad**
- Extensive irradiation campaign in past 3 years to qualify the technology
- Significant radiation damage above 100 Mrad:
  - Analog: transconductance, Vt shift
  - Digital: speed degradation

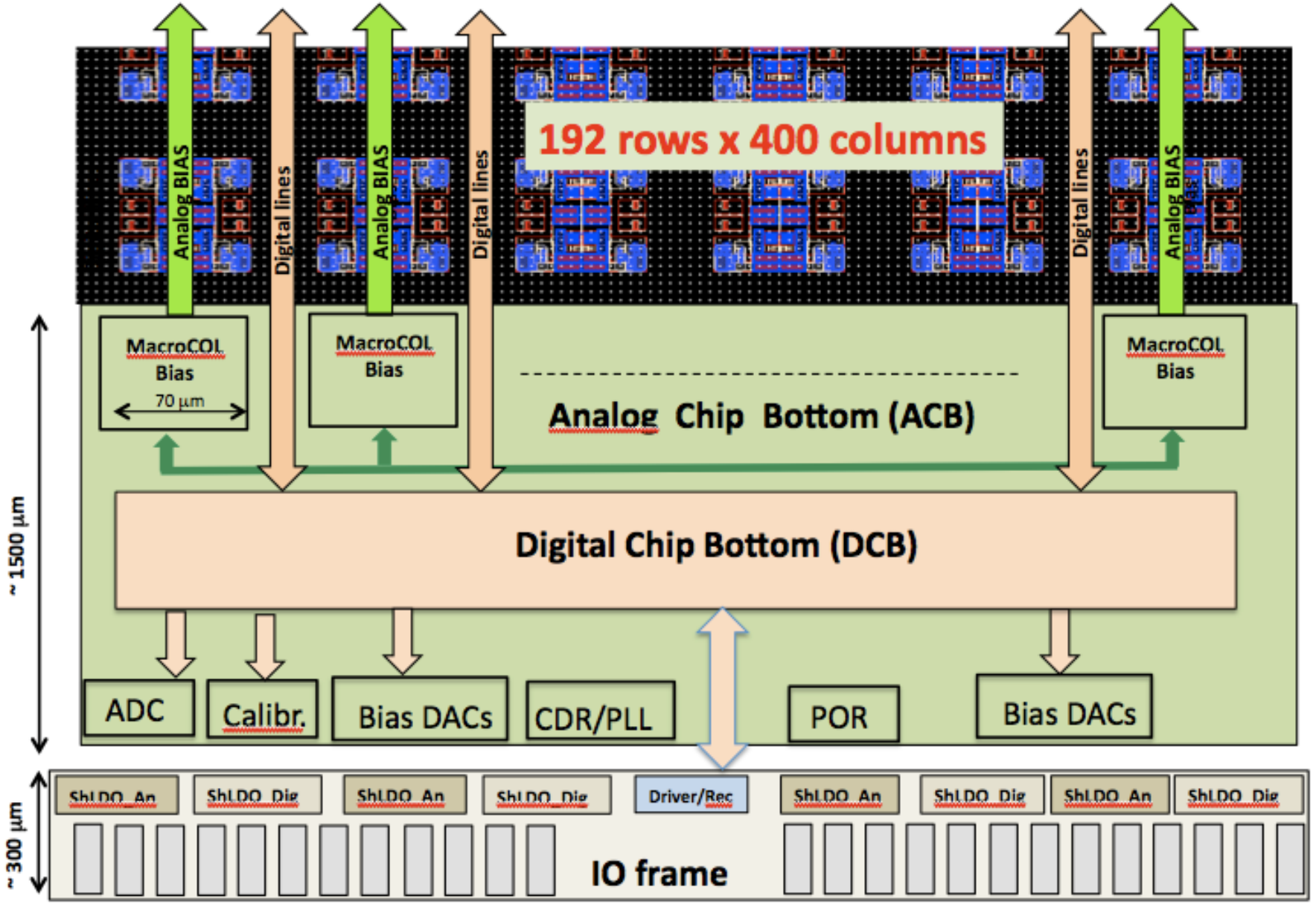
See M. Menouni talk

- **CHIPIX65** and **FE65-P2** demonstrator being characterized after irradiation

See N. Demaria talk for the CHIPIX demonstrator

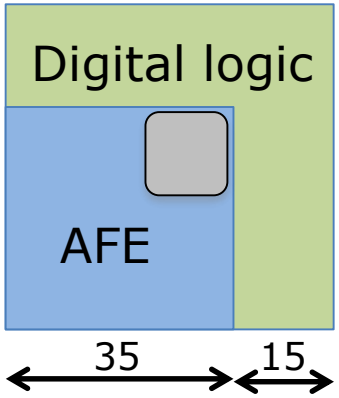
- 200 Mrad and 500 Mrad **simulation models** were developed to "predict" the circuit behavior and have been extensively exploited during design phase

RD53A floorplan



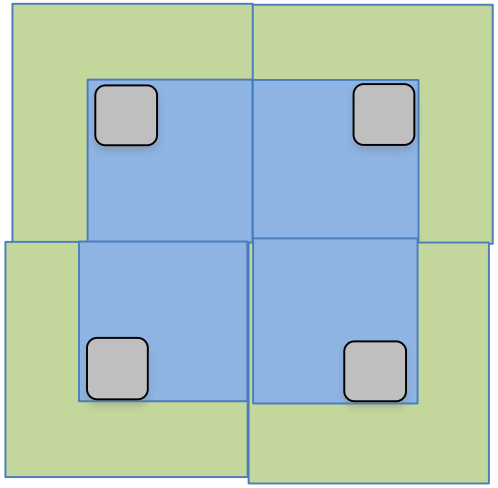
RD53A Pixel floorplan

- 50% Analog Front End (AFE) - 50% Digital cells



The "analog island" concept

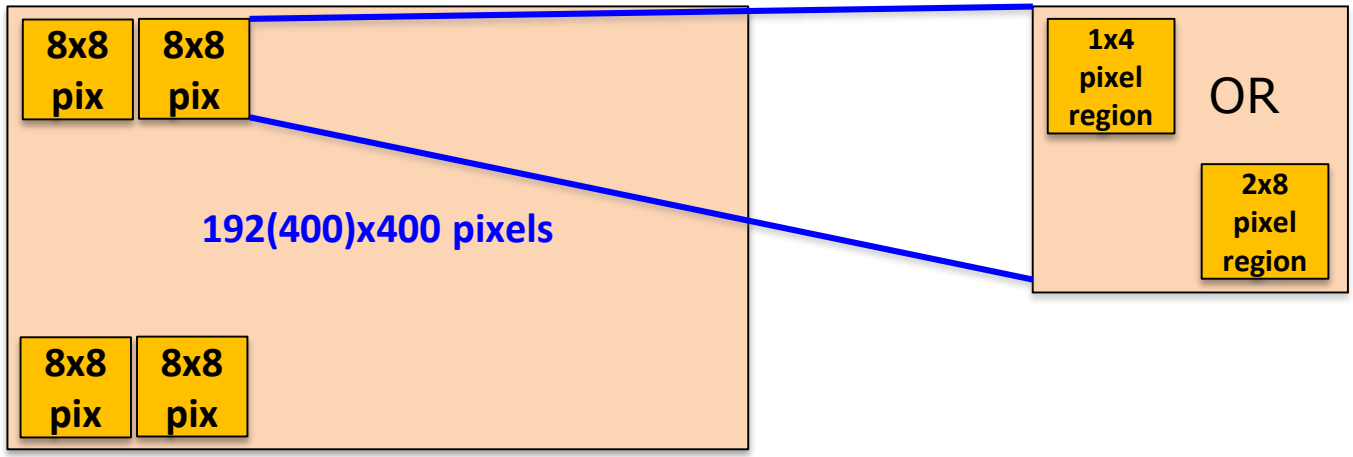
A "quad"



- The pixel matrix is built up of **8x8 pixel cores** → 16 analog islands (quads) embedded in a flat digital synthesized sea
- A pixel core can be simulated at transistor level with analog simulator
- All cores (for each FE flavour) are identical → Hierarchical verifications

Pixel array logic organization

- **Basic layout unit**: 8x8 digital Pixel Core → synthesized as one digital circuit



- One Pixel Core contains multiple Pixel Regions and some additional arbitration and clock logic
- Pixel Regions share most of logic and trigger latency buffering

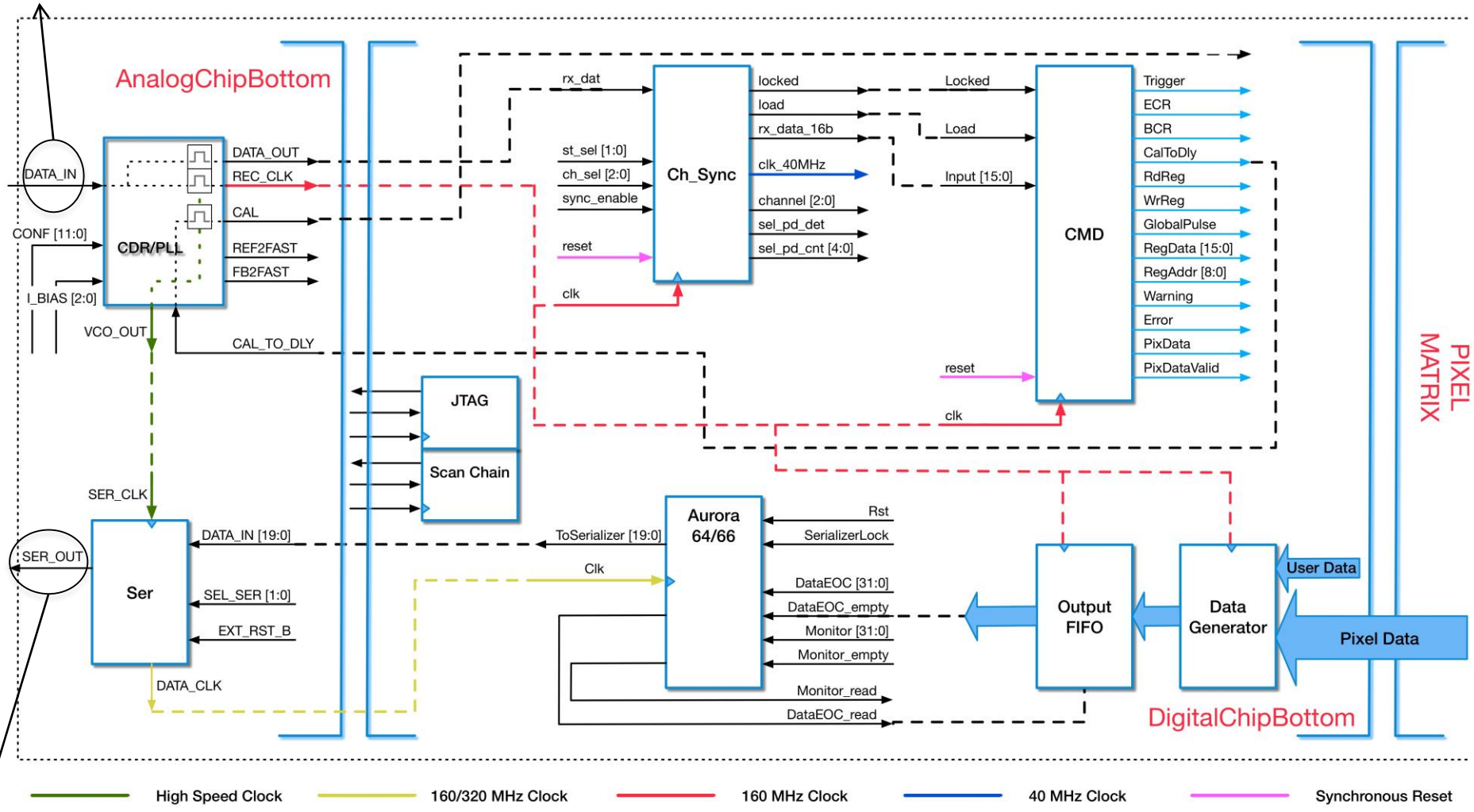
Distributed Buffering Architecture (FE65_P2 based):
- distributed TOT storage

Centralized Buffering Architecture (CHIPIX65 based (4x4)):
- centralized TOT storage
- Integrated with Synch FE

See S. Marconi talk

Digital Chip Bottom (DCB)

Single serial input stream



Port A: 1-2-4 CML outputs @ 1.28 Gbps

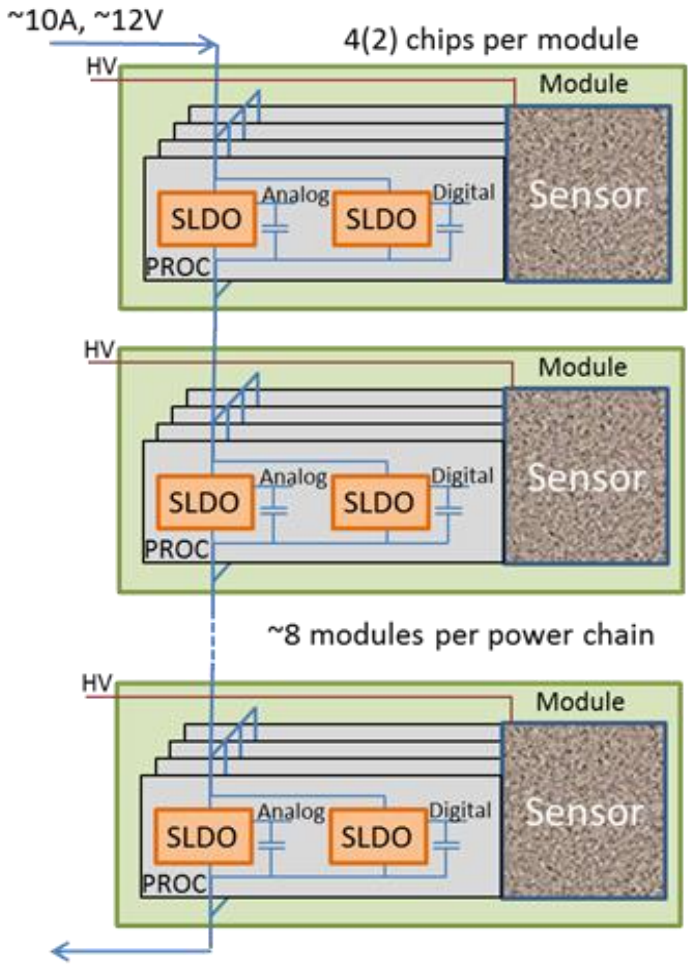
OR

Port B: 1 output @ 5.12 Gbps

Serial Powering

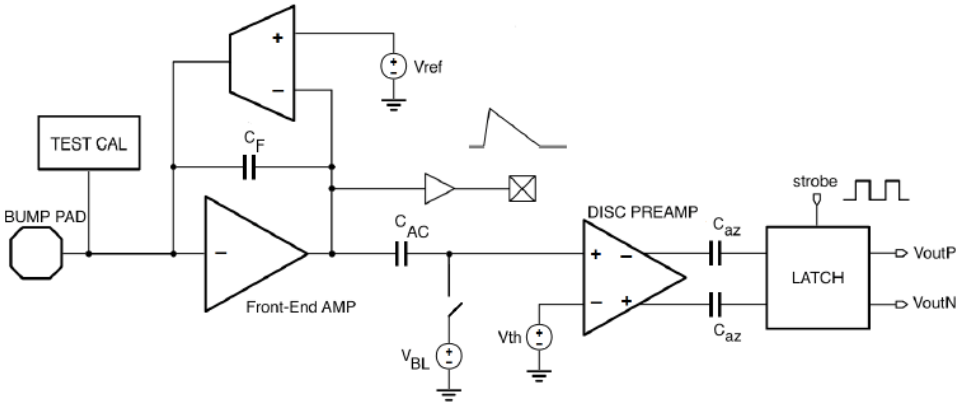
- RD53A is designed to operate with **Serial Powering** → constant current to power chips/modules in series
- Based on ShuntLDO
- Dimensioned for production chip

- **Three operation modes**:
  - ShuntLDO: constant input current Iin → local regulated VDD
  - LDO (Shunt is OFF) : external un-regulated voltage → local regulated VDD
  - External regulated VDD (Shunt-LDO bypassed)

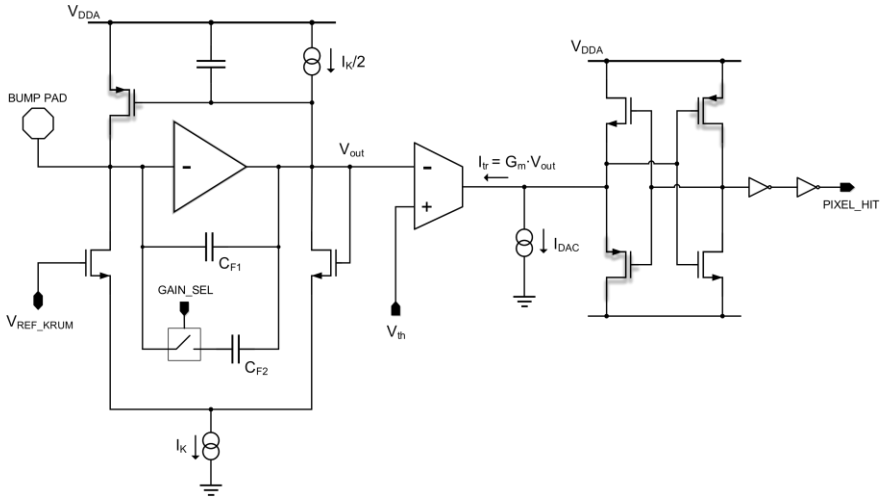


Analog front-ends

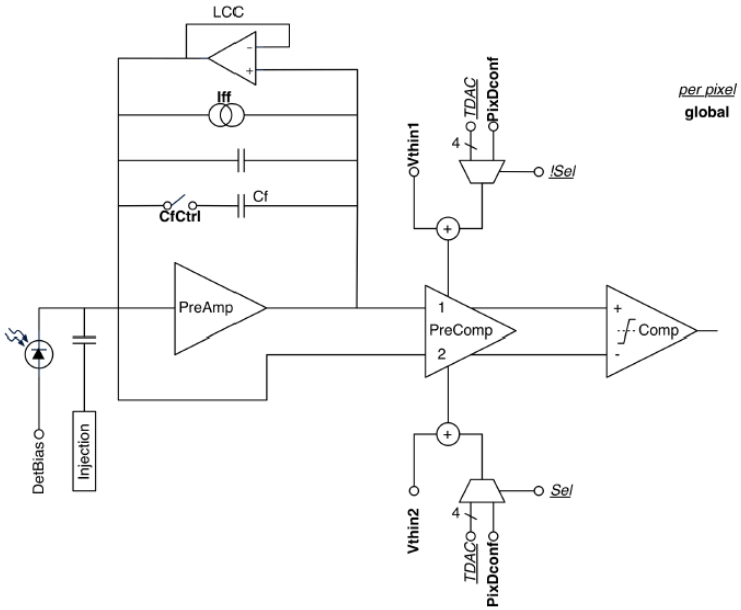
Synchronous AFE



Linear AFE

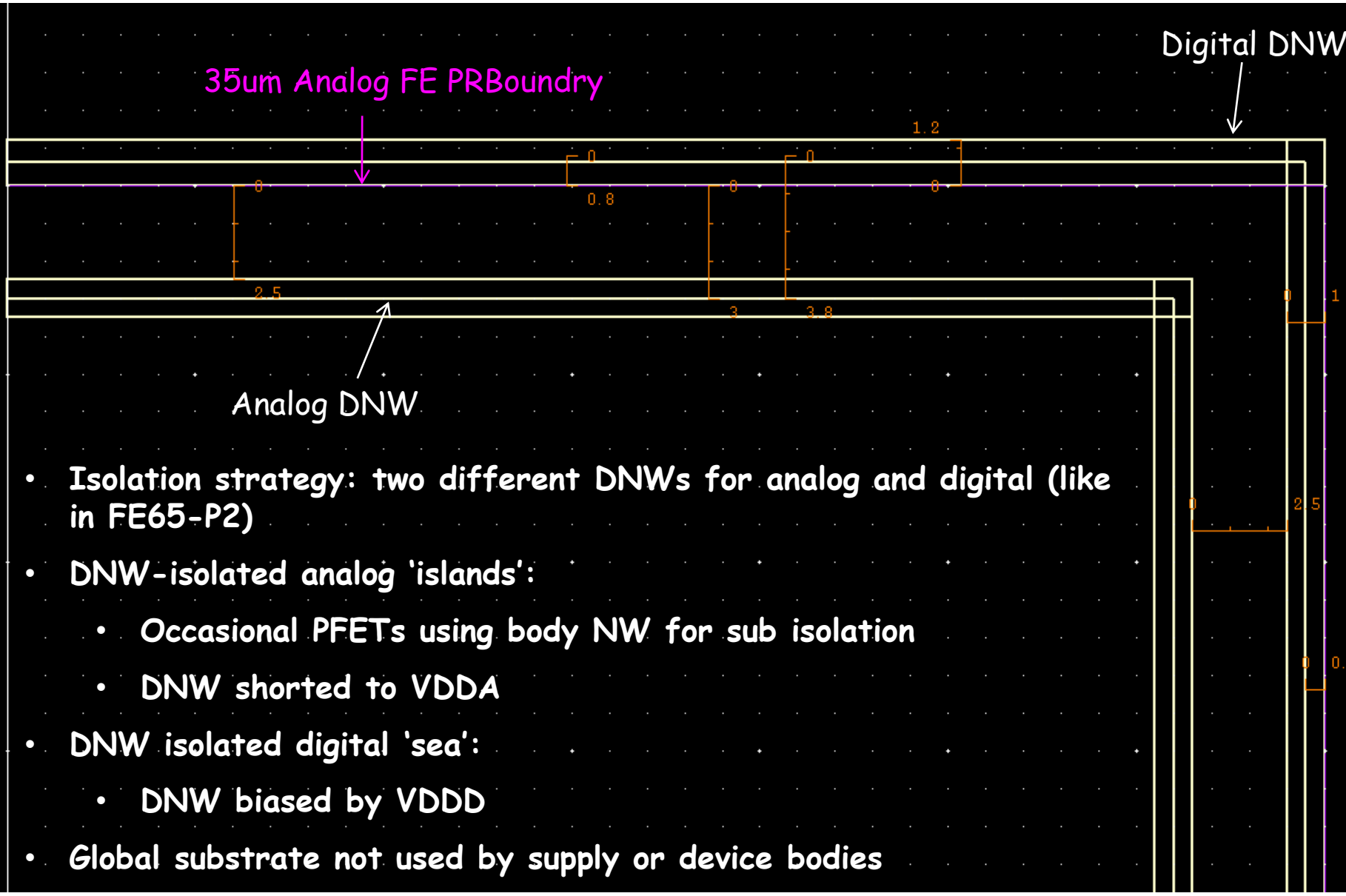


Differential AFE



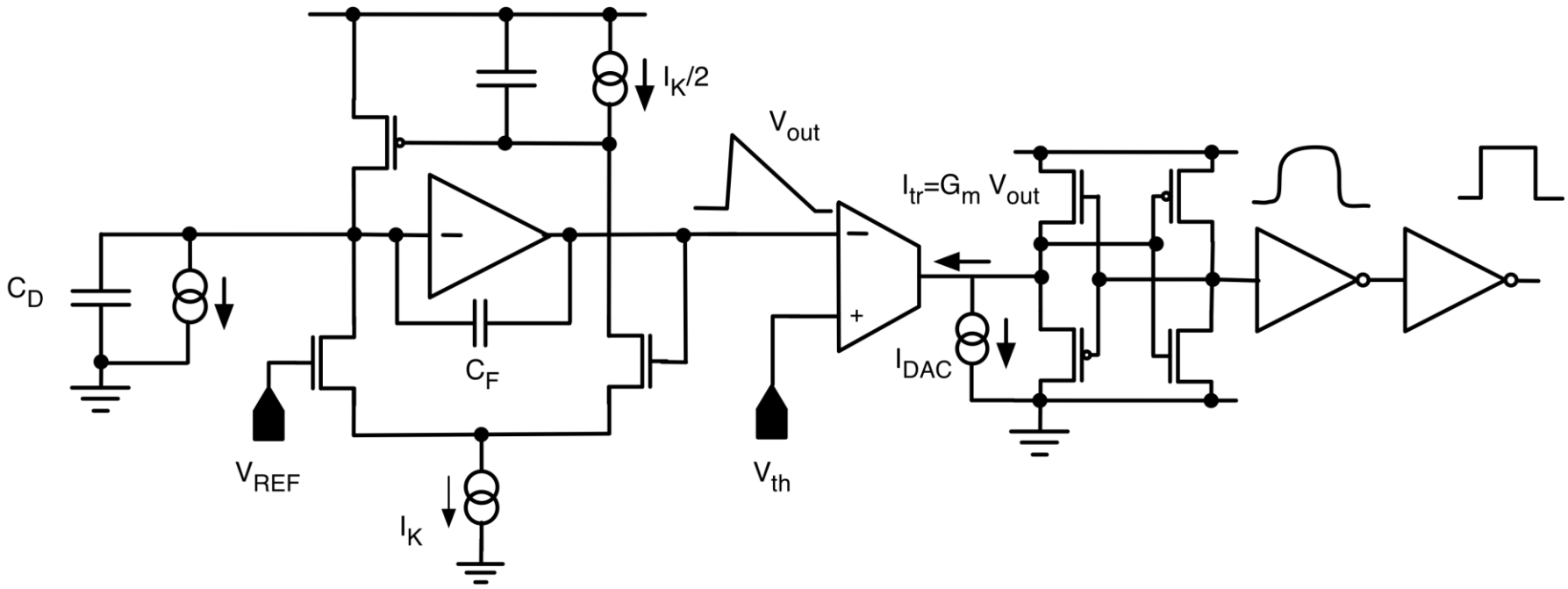
- **3 different version** of the analog FE (AFE) will be integrated in RD53A
- Three **design reviews** (the last one in March 28, 2017) have been carried out for the AFEs.
- **Final verifications** of the AFEs on-going

Isolation strategy



- Isolation strategy: two different DNWs for analog and digital (like in FE65-P2)
- DNW-isolated analog 'islands':
  - Occasional PFETs using body NW for sub isolation
  - DNW shorted to VDDA
- DNW isolated digital 'sea':
  - DNW biased by VDDD
- Global substrate not used by supply or device bodies

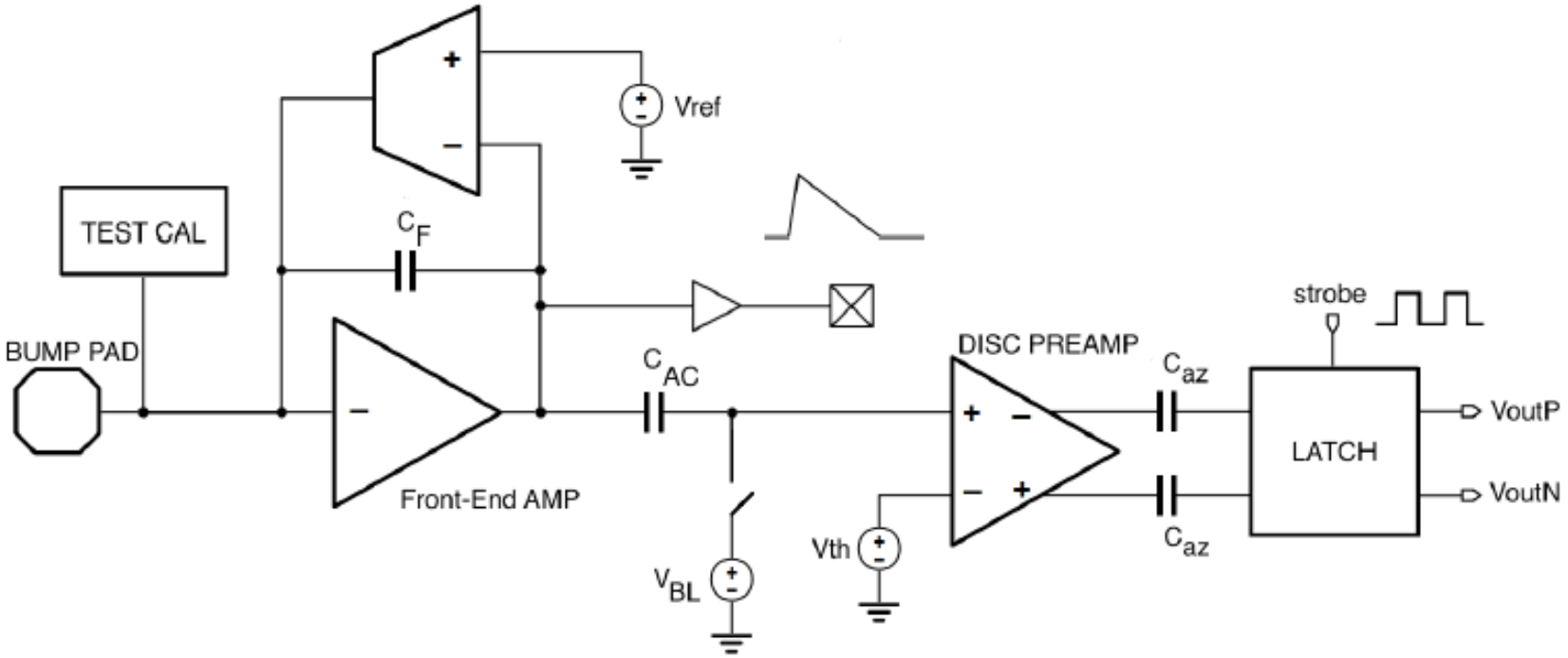
Linear Analog Front-end



- **Single amplification stage** for minimum power dissipation
- **Krummenacher feedback** to comply with the expected large increase in the detector leakage current
- High speed, low power **current comparator**
- **4 bit local DAC for threshold tuning**
- **In-pixel calibration circuit**

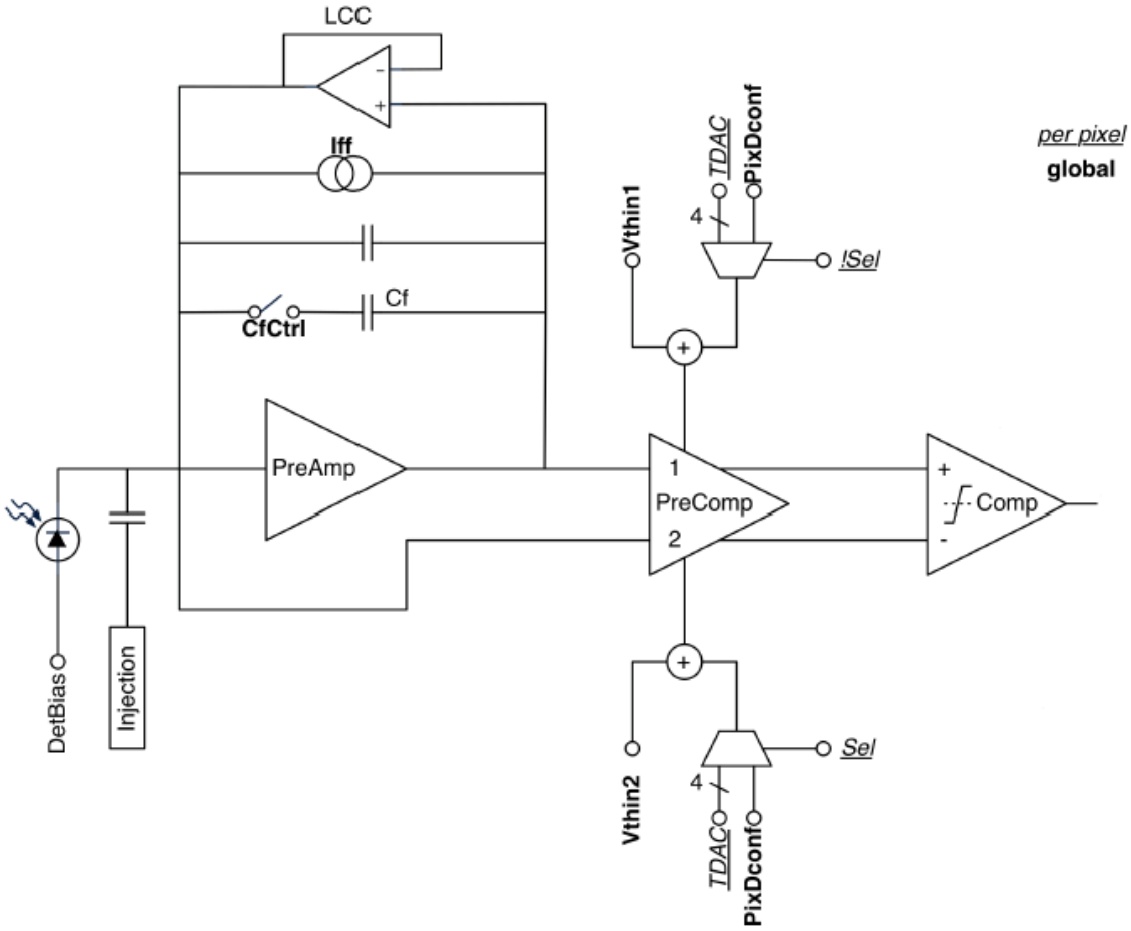
- Selectable gain (1 bit) and recovery current (per. Bias DAC)
- Overall **current consumption**: ~4 uA
- **Integrated/tested in CHIPIX65 (with slight modifications)**

Synchronous Analog Front-end



- **One stage CSA** with **Krummenacher** feedback for linear ToT charge encoding
- **Synchronous discriminator**, AC coupled to CSA, including offset compensated differential amplifier and latch
- Threshold trimming by means of autozeroing using capacitors
- **Fast ToT counting** with latch turned into a local oscillator (100-900 MHz)
- **Integrated/tested in CHIPIX65 demonstrator chip**

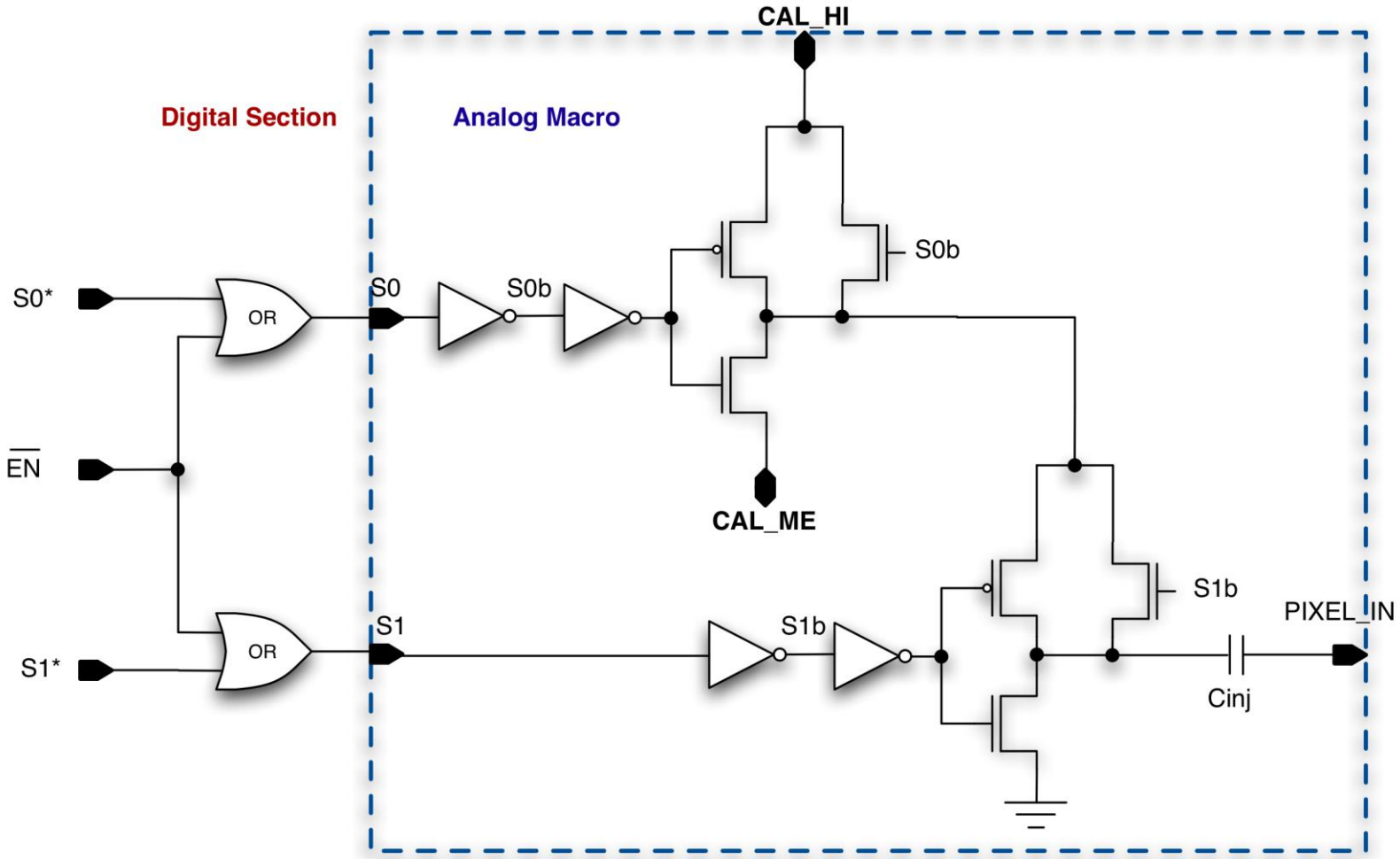
Differential Analog Front-end



- **Continuous reset integrator** first stage with **DC-coupled pre-comparator stage**
- Two-stage open loop, **fully differential input comparator**
- **Leakage current compensation** (not shown) a la FEI4
- **Threshold adjusting** with global 8bit DAC and two per pixel 4bit DACs

Calibration circuit

Common scheme for all the AFEs



- **Local generation** of the analog test pulse starting from 2 defined DC voltages CAL_HI and CAL_ME) distributed to all pixels and a 3rd level (local gnd)
- **Two operation modes** which allow to generate two consecutive signals of the same polarity or to inject different charges in neighboring pixels at the same time

AFEs main features (reported in March design review)

	Synch AFE	Lin AFE	Diff AFE*	spec
Charge sensitivity [mV/ke]	43	25	103	-
ENC rms [e]	67	83	53	<<126
Threshold dispersion σ(Qth) rms [e]	93	32	20	<<126
$\sqrt{(ENC^2 + \sigma(Qth)^2)}$ [e]	115	89	54	≤126
In-time overdrive [e-]	≤50	≤100	0	≤ 600
Current consumption [μA/pixel]	3.3[1]	4.3	3.5	≤ 4
Time over threshold [ns]	121	99	118	< 133

- Post-layout simulations (*except for the Diff AFE→ schematic level sim), CD=50fF, T=27° C, Qth=600e-.
- In-time overdrive→ relative to a Qin=30ke-
- Time walk → Qin=1200 e- (relative to a Qin=30ke-)
- ToT → Qin=6ke-
- [1] 5.1uA including the latch

Submission status

- **Analog Front-ends:**
  - Synchronous & Linear AFEs: final version ready → integrated with CORE
  - Differential AFE: final version ready → integration with CORE on going
- **Analog Chip Bottom (ACB)**: assembly ready (RD53 IP blocks). Simulation with analog and mixed-signal simulator ongoing
- **Digital**: RTL ready, verifications on-going
- **Shunt-LDO**: 2A version of Shunt-LDO submitted on 19th Oct. 2016
  - Test of prototypes just started and looks promising
  - Irradiation campaign carried out
  - Simulation of full power system ShLDO-Bandgap-POR ongoing
  - Integration in IO Frame: almost done
- **IO Frame**: bottom PADs frame almost ready → 199 PADs with 100um pitch; passivation opening: 58um x 86 um; TSV Compatible. Top PAD frame (test and monitoring) assembly on-going.

See H. Krüger talk

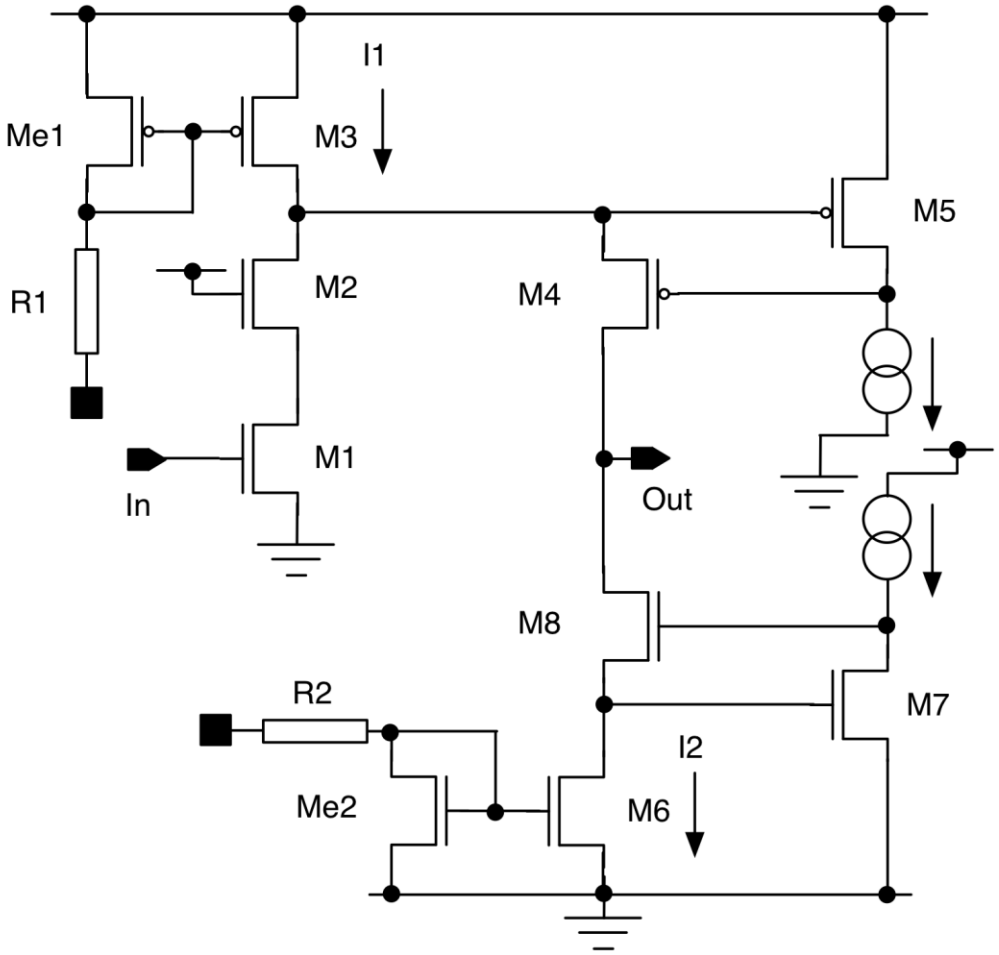
Conclusions

- The **RD53A demonstrator design** is being finalized in the framework of the RD53 Collaboration in a **65 nm CMOS technology**
- Goal of the RD53A chip is to demonstrate the feasibility of the 65 nm technology in facing the challenging requirements set by the **future experiment upgrades at the HL_LHC**
- The large-scale chip will be submitted at the end of **May 2017**
- The **final design** is almost ready, extensive verifications are on-going

Backup

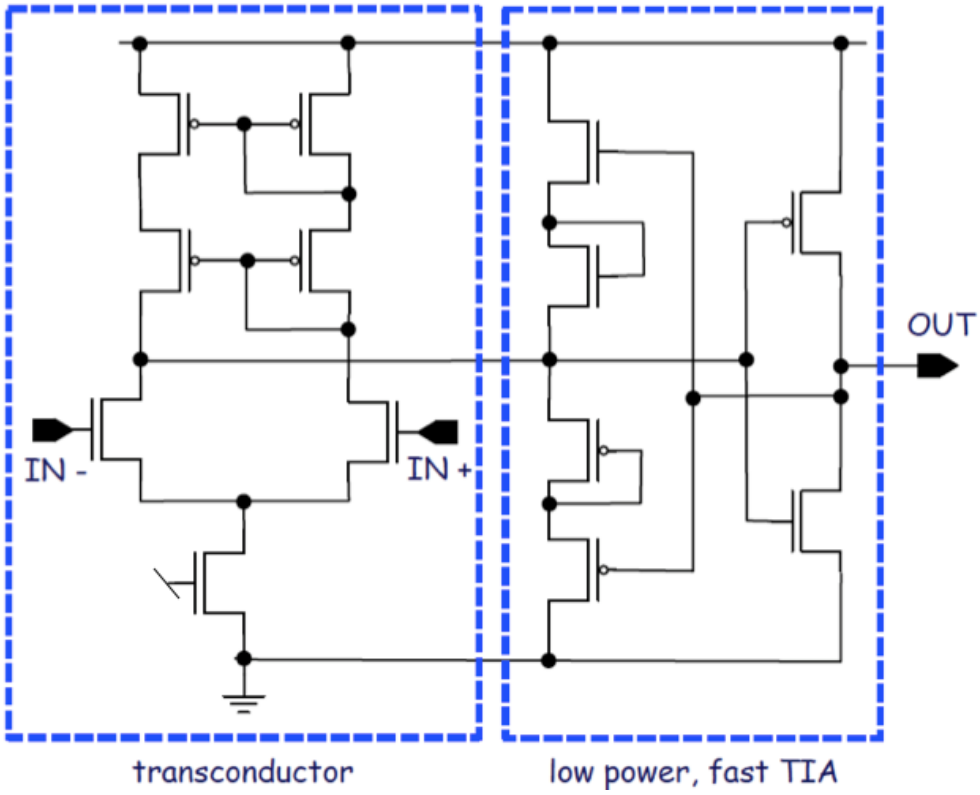
Lin AFE schematic diagrams

Preamplifier



- Gain stage based on a **folded cascode** configuration (~3 uA absorbed current) with a regulated cascode load

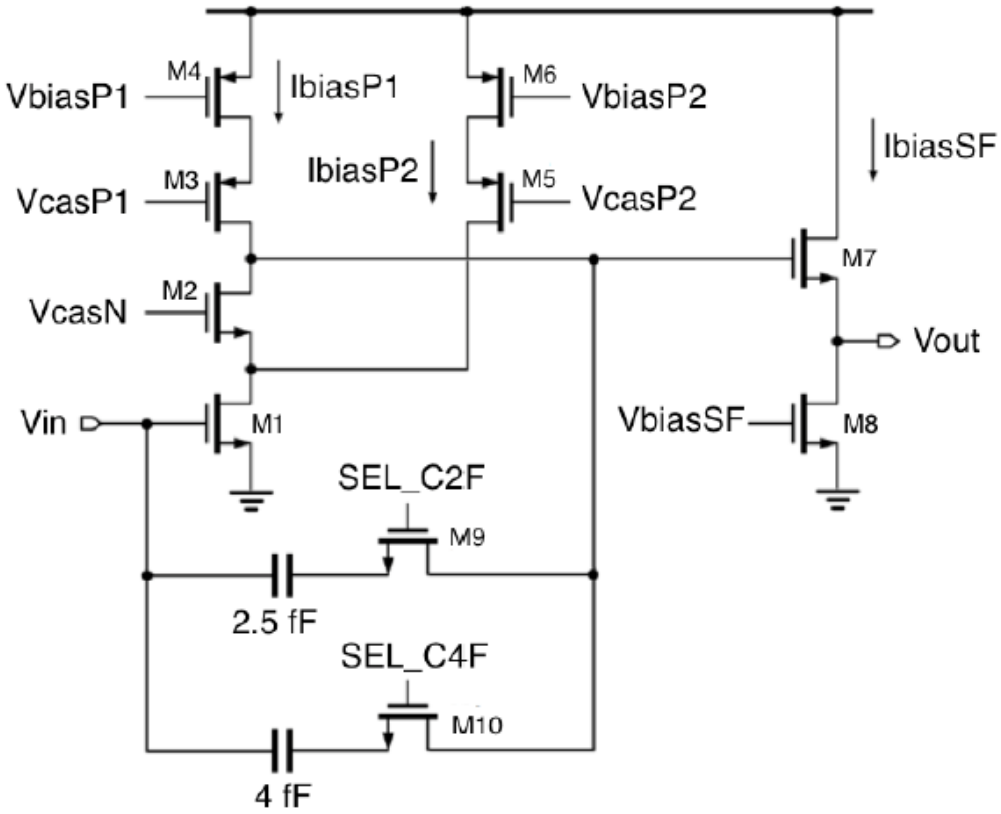
Comparator



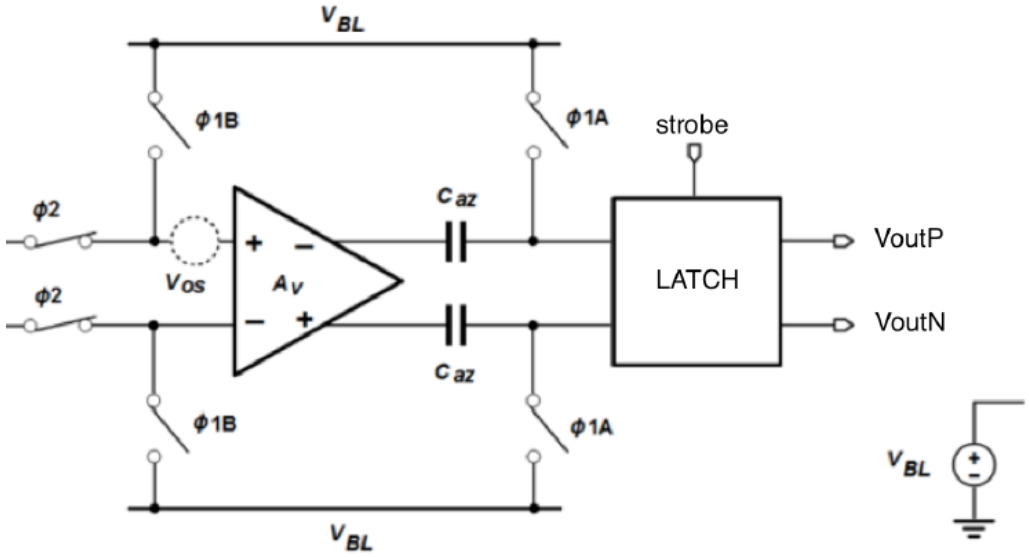
- Low power, **fast discriminator** (~ 1 uA absorbed current) including Gm stage and a transimpedance amplifier providing a low impedance path for fast switching

Sync AFE schematic diagrams

Preamplifier



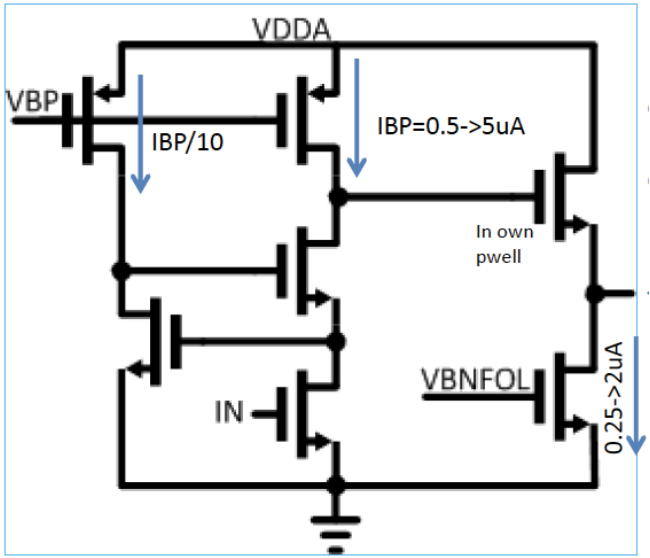
Comparator



- Telescopic cascode with current splitting and source follower
- Two switches controlling the feedback capacitance value

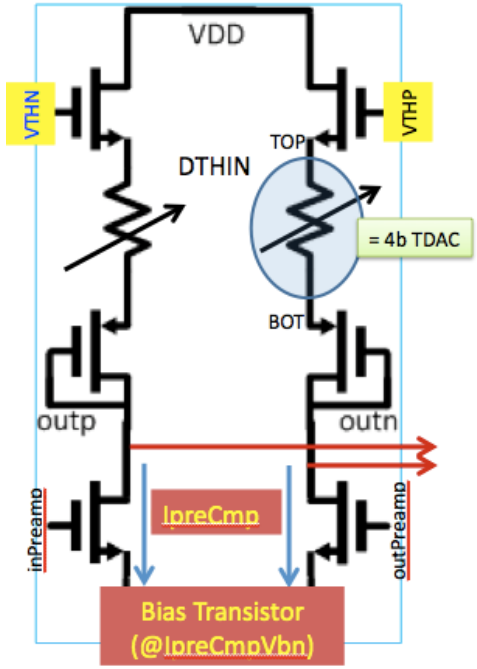
- Offset (and mismatch) cancellation based on **comparator autozero** (store offset on a capacitor, and then subtract it from signal + offset)

Diff AFE schematic diagrams



Preamplifier

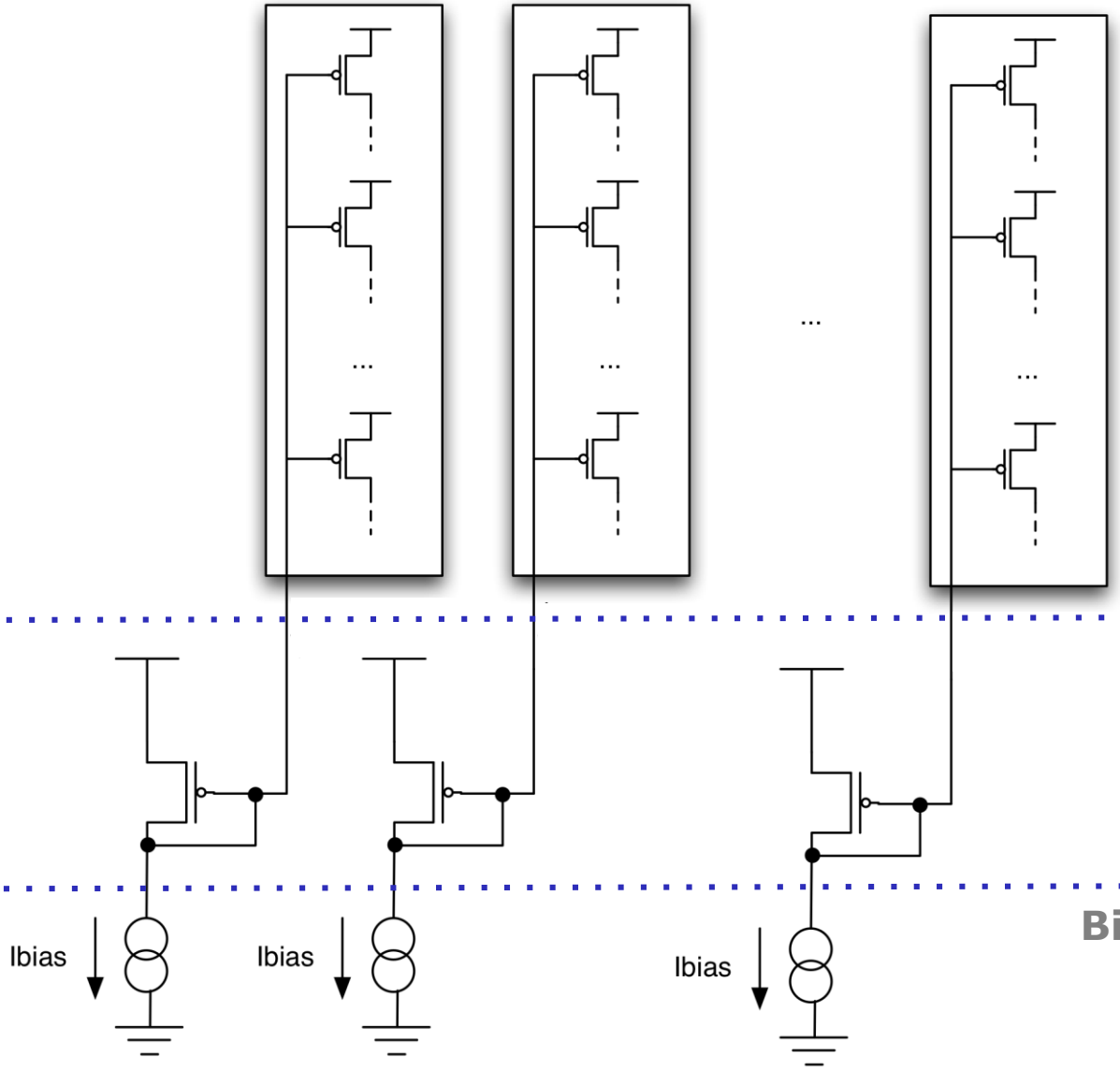
- Gain stage with active cascode
- Simple follower as buffer



Pre-comp

- Fully differential amp w/ resistive load
- Acts as single-to-differential converter
- Global Vth DACs generates effective differential supplies
- Local DTHn trims binary-weighted resistive load
- Sets output CM and differential OP for comp

Analog FE bias scheme



- Robust design
- Not sensitive to leakage
- "Double stage mirroring", biasing DACs and Bandgap refererences **already integrated/tested in CHIPIX65**

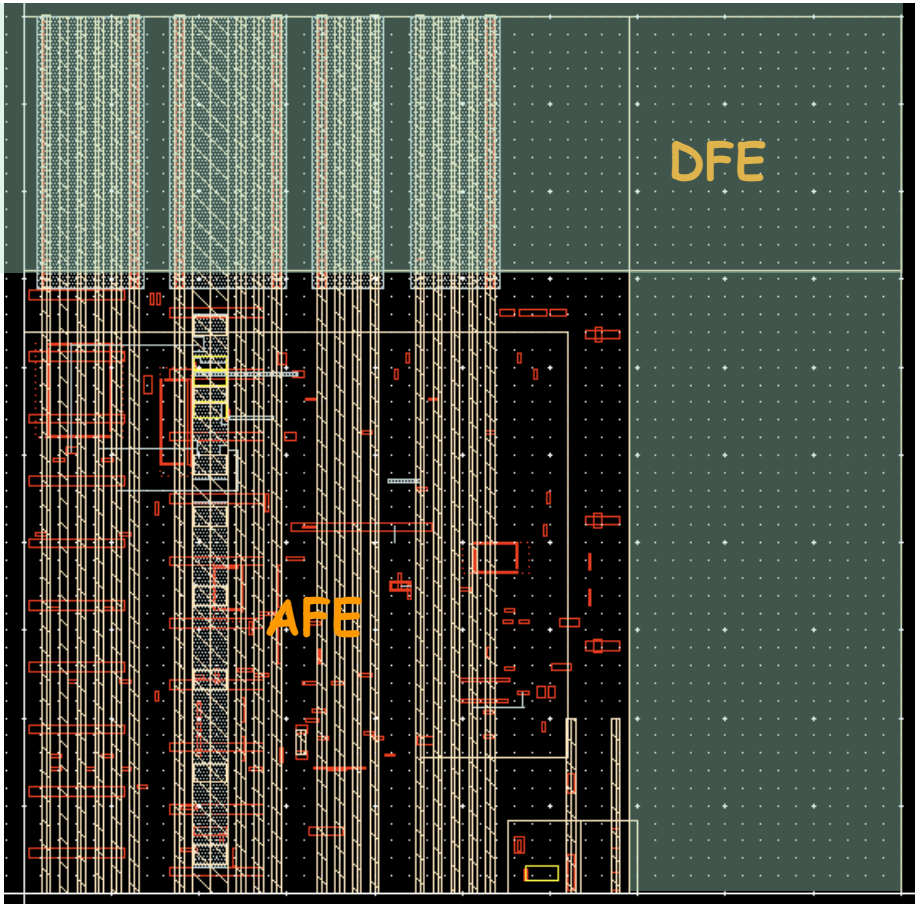
Pixel array

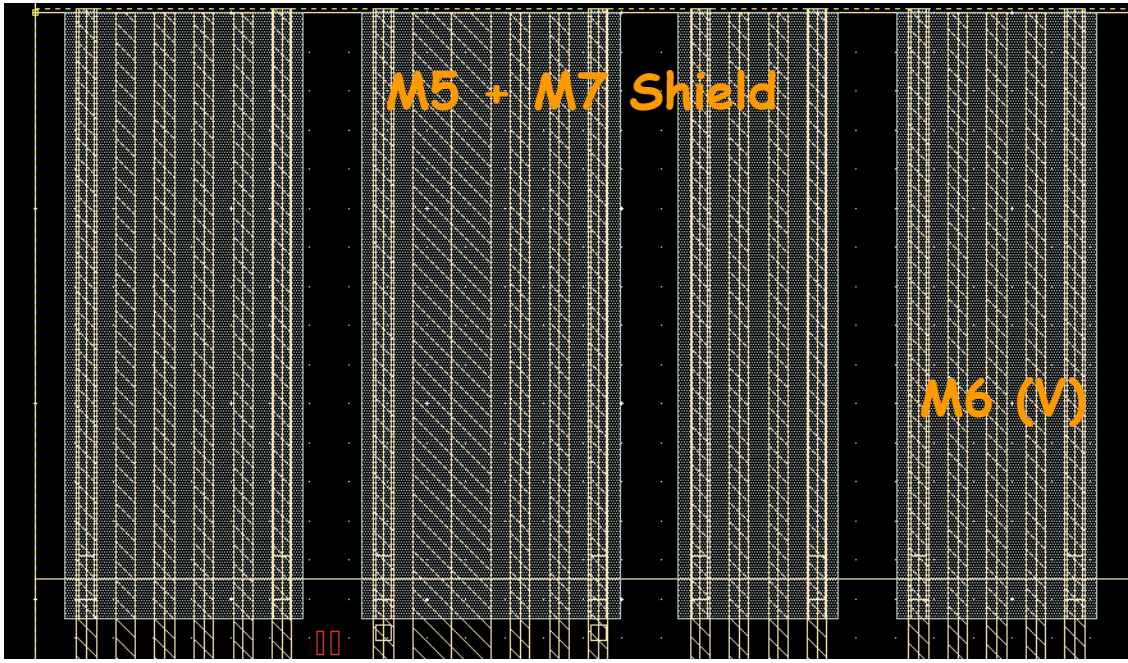
Second stage mirroring (Macrocol bias)

Biasing DACs + first stage mirroring (ACB)

Analog bias

- AFE **area & arrangement** → 35um x 35 um aspect ratio with "analog island" arrangement
- **Same bump PAD structure**
- **Common strategy** for power, bias distribution & shielding





- **M6 V lines** for the analog bias
- **M5/M7 shield** for bias lines in the digital section of the pixel
- **AP/M9/M8** V supplies

Pixel array logic organization

- Each Pixel Core receives all input signal from the previous core (closer to the Digital Chip Bottom)
- Regenerates the signals for the next core.
- The timing critical **clock** and **calibration injection** signals are internally delayed to have a uniform timing (within 1-2 ns)