AIDA/RD53 activities in Perugia

(AIDA-2020 2nd ANNUAL MEETING)

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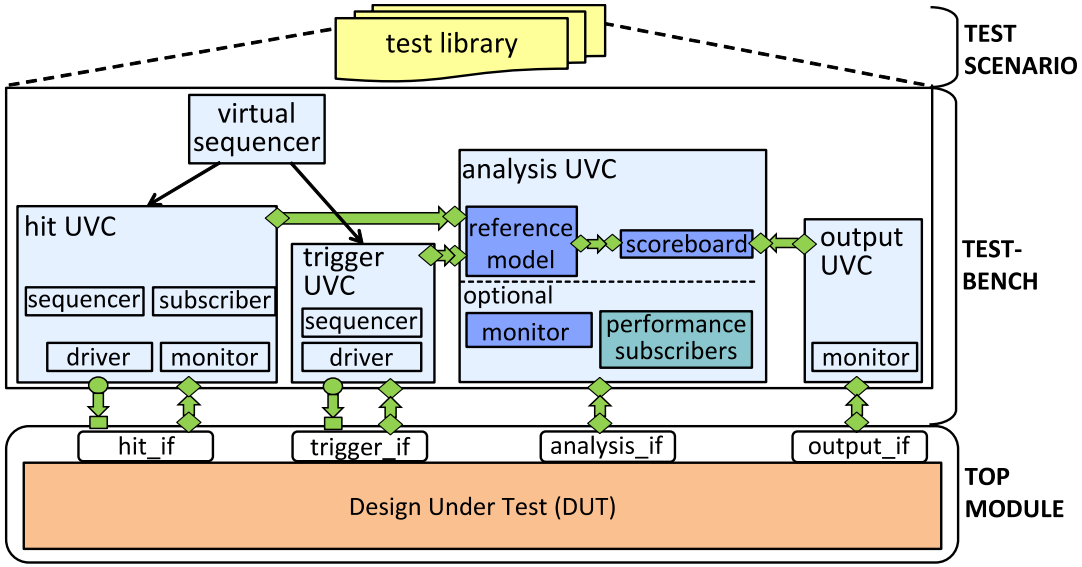
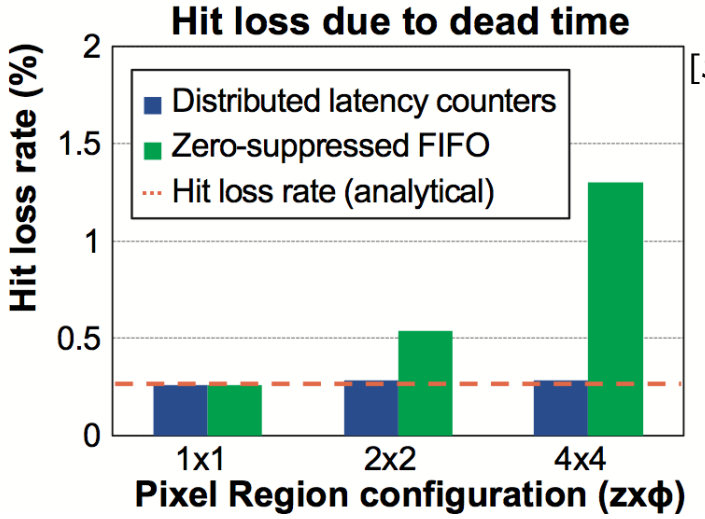
OUTLINE

- **Introduction**
  - Verification Environment for PIXel chips (VEPIX53)
  - Approach for reliability in radiation environments
- **Digital architecture comparison and choice**
- **Low-power methodology for serial powering**
  - Analysis and optimization
- **Conclusions and future work**

- **Verification Environment** for **PIXel** chips (*VEPIX53*) for:
  - **Modularity**, **reusability** of same testbench:
    - different tests
    - multiple design stages
    - different designs/design blocks
  - Extended **flexibility**: stimuli generation
  - **Automated verification**, **performance** assessment
  - **Test cases:**
    - simulation of previous pixel chips
    - architectural study on PR architectures (behavioral level)
    - for RD53A building blocks and/or full chip
    - in addition: used by different projects at CERN as starting point for verification

[*S.Marconi et al.*, Springer Lecture Notes, *2016*]





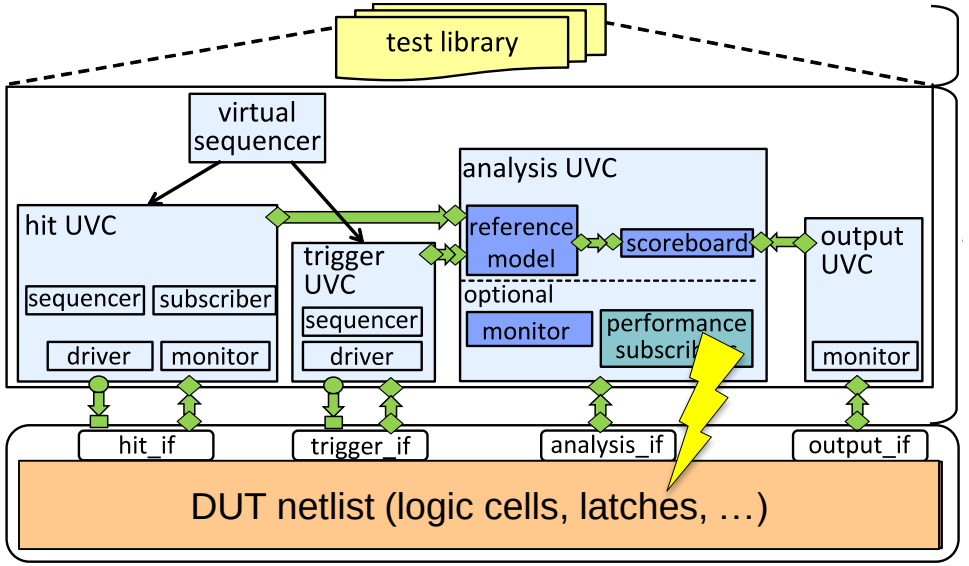
[*S.Marconi et al.*, JINST 2015]

Approach for reliability in radiation environments

In this presentation, **focus on SEUs for the pixel array logic**

- Based on estimated cross-section ($5 \cdot 10^{-14}$ cm^2):
  - **protection** strategy is **needed for pixel configuration** latches
    - ~ 1% pixels already affected after 20s of operation
    - → hardening by cell design, special latches (CPPM, Marsiglia) and/or re-freshing configuration
  - **finite state machine protection not required if capable of recovering automatically** after a transient of non-functionality
    - to be proven with simulations under operating conditions
  - no protection is needed for hit data during trigger latency
    - corruption probability during latency < 10^{-8}

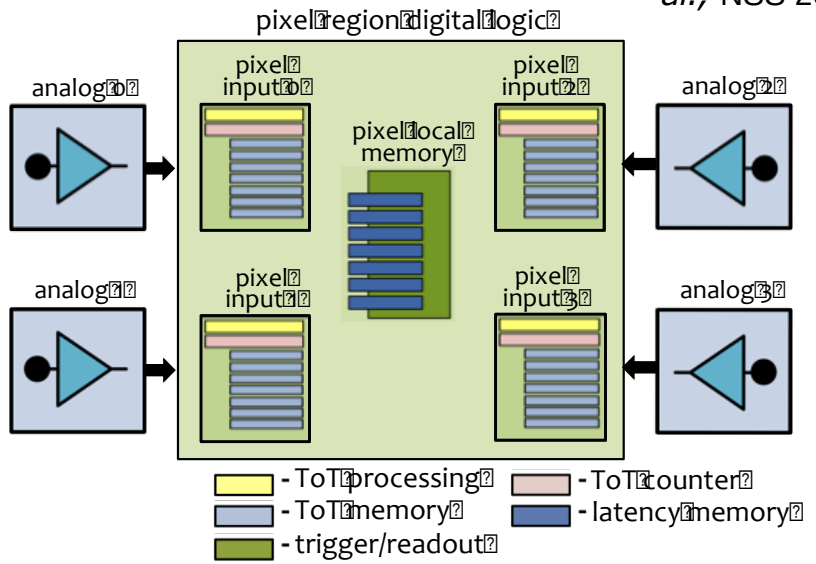
- **How to simulate SEU injection**?
  - Integrate random **bit-flip in sequential elements** during simulations of the gate-level or post P&R **netlist in VEPIX53**
    - **automated verification** to identify eventual persisting effects
    - initial simulations have shown no persistent error



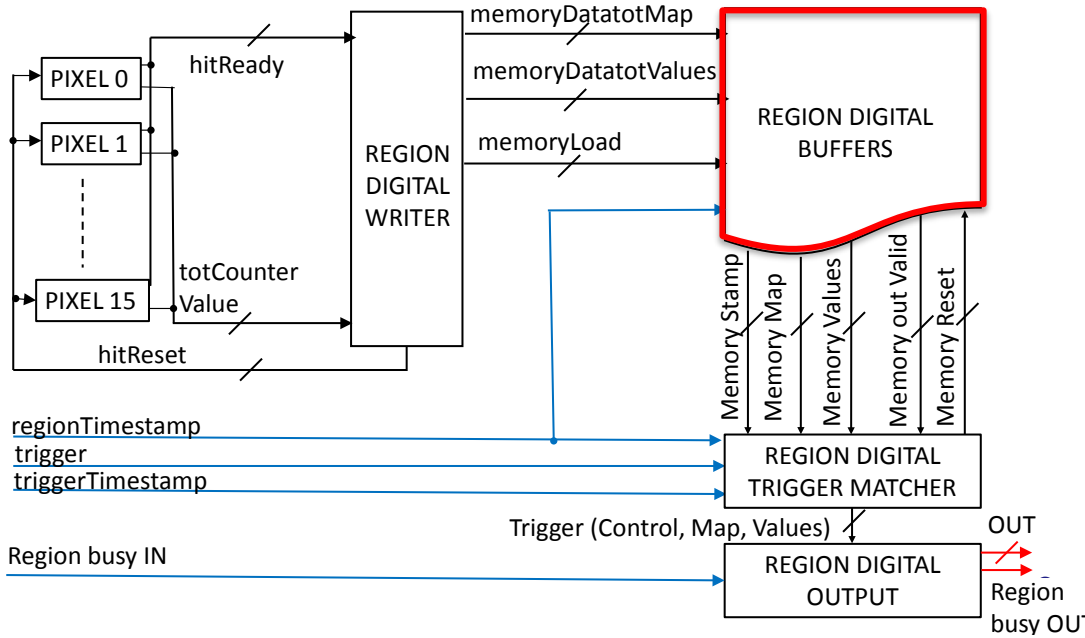
Architecture optimization and comparison by means of the VEPIX53

[*S.Marconi et al.*, NSS 2016]

- ***1st architecture:*** *distributed 1x4 pixel region*
  - Logic resources shared in PR composed of 1x4 pixels
  - Distributed buffering (i.e. hit storage) scheme
    - shared timestamp memory
    - distributed memory for charge information (4-bit ToT = Time Over Threshold)

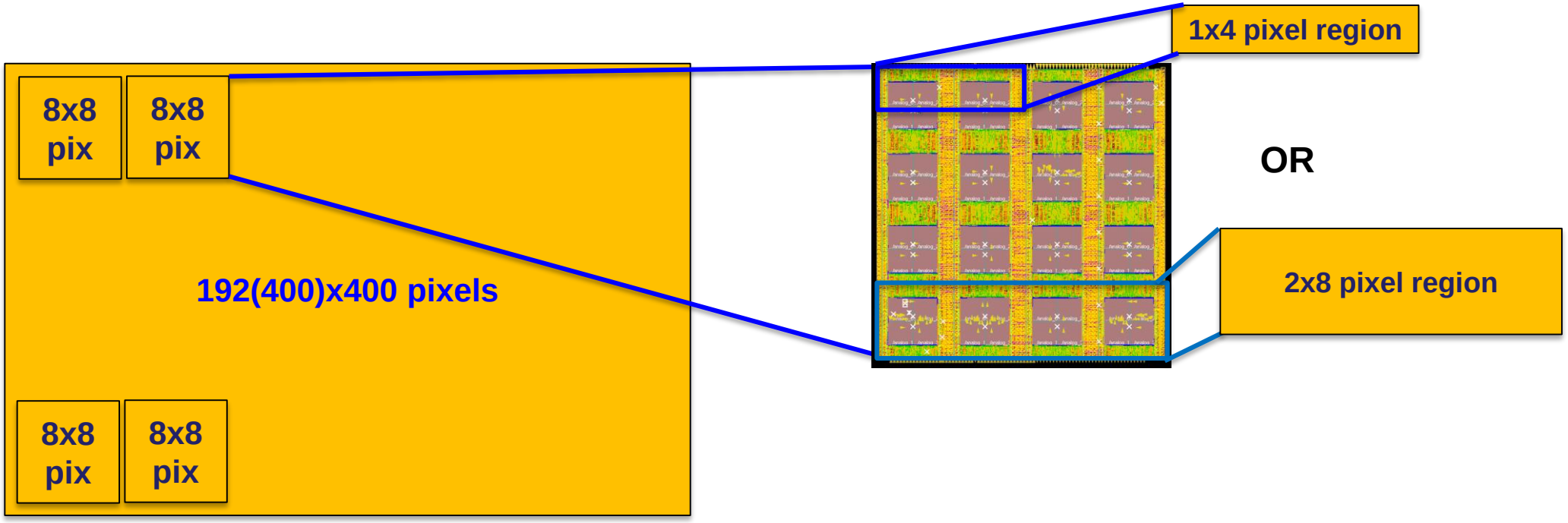


- ***2nd architecture:*** *centralized 2x8 pixel region*
  - Logic resources shared in PR composed of 2x8 pixels
  - Centralized buffering scheme
    - shared timestamp
    - shared ToT information
  - Data stored in buffer are reduced



Digital architectural choices for RD53A

- both architectures have advantages, design optimization ongoing on both sides
- as RD53A is a prototype chip both are being integrated: 1x4 with asychronous front-ends and 2x8 with the synchronous front-end
- the choice on the pixel region shape is aimed to reduce buffer losses (elongated clusters)



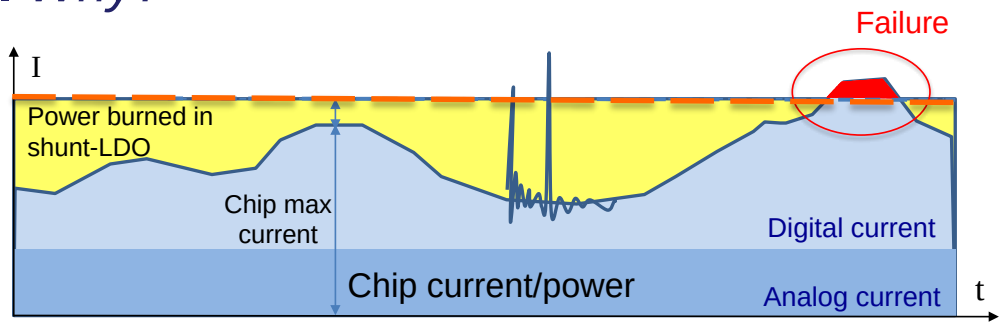
– *RTL simulations*: after recent optimizations, **both architectures featuring similar deadtime losses**

– *Area*: **centralized architecture has area advantages** (with potential lower digital losses thanks to additional memories)

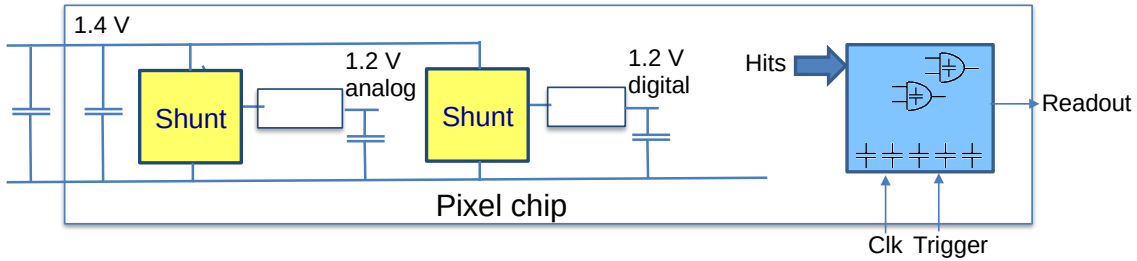
– *Power*: **similar order of magnitude,** with distributed architecture possibly lower (at current stage)

Low-power analysis and optimization methodology

- In this context, **"concept" of low power** is **not obvious.** *Why?*
  - **Serial powering** across modules **to reduce material** → constant current is provided from the powering system
  - The **regulator circuit** (combination Shunt and LowDrop Out regulator → **Shunt-LDO**) **will burn "surplus" current** to keep the serial power current constant



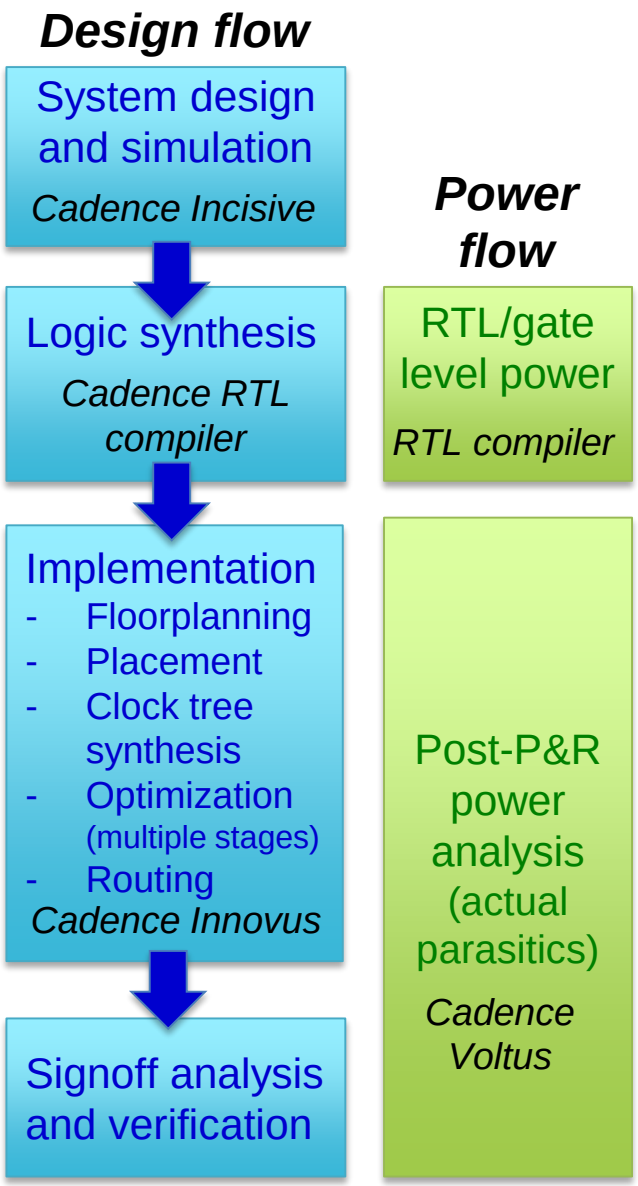
  - **Need** to know **maximum current/power visible to the powering system**
  - **Low-pass filtering** from chip to serial power network: **power variations** are **averaged over a time window** (comparable with **decoupling time constant**)



- Different "definitions" of power:
  - **average** (over long simulation, with realistic operation) → **"usual" target** for low power designs
  - **peaks** (look **power evolution over time**, i.e. **power profile**):
    - short time scale (~ps-25ns): should be filtered by on-chip decoupling
    - **longer time scale (~1us):** power averaged over such time window **seen at the powering system level**

      → **Optimization target** → **need for a methodology to guide optimization**

Low-power analysis and optimization methodology



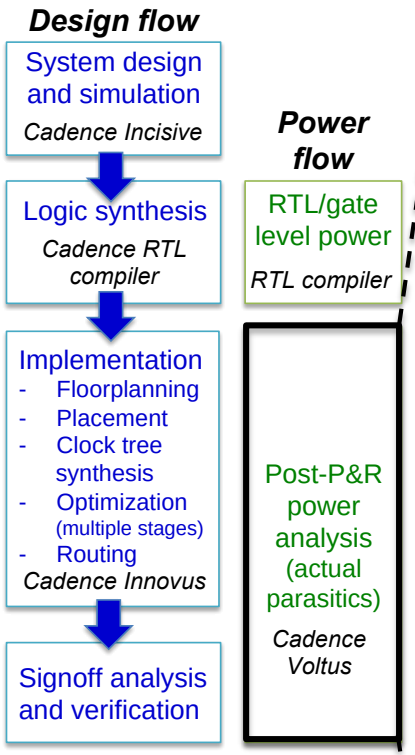
Main steps:

1) **power analysis at gate-level (i.e. after synthesis to gates):**
   - drive architectural choices
2) **accurate post Place&Route (P&R)** power analysis

Application: detailed design optimization and choices

Remark: **realistic digital activity** based on **simulations run with VEPIX53**

Low-power analysis and optimization methodology



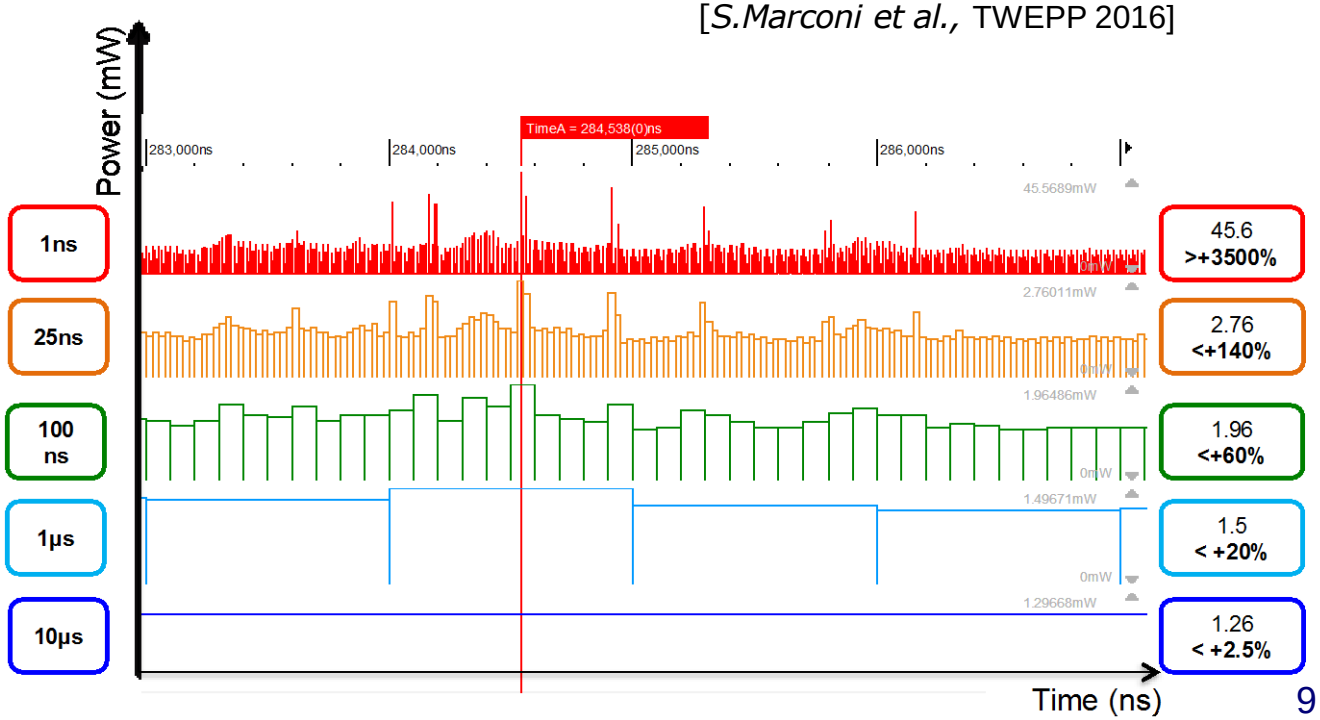
2) accurate post Place&Route (P&R) power analysis and optimization:

a. **average power estimations** under different activity conditions to assess power impact of different factors

a. **dynamic power variations** analysis under the variety of operating conditions and at different time scales (1ns, 25ns, 100ns, 1µs, 10µs):
   a. simulations with Shunt-LDO confirmed decoupling effect

Activity conditions	single pixel, digital	Final chip (400x400)
hits (3 GHz/cm^2) and triggers (1 MHz/cm^2)	4.8 µW (52% clk tree)	0.774 W
only clock (~ -20%)	3.8 µW (62% clk tree)	0.610 W
hits (3 GHz/cm^2) and no trigger(~ - 2.5%)	4.7µW (53% clk tree)	0.752 W

[*S.Marconi et al.*, TWEPP 2016]



Low-power analysis and optimization methodology

- Presented methodology used for optimization of the pixel array logic:
  - **Example**: 1x4 distributed architecture → most techniques applied to both digital architectures
  - Metrics:
    - **area** (density)
    - power → "**peak power**" is obtained assuming 1 μs averaging time constant
    - hit loss (for memory overflow)

8x8 digital core, hits and triggers activity TYPICAL corner	Average Power per pixel (μW)	Peak Power per pixel (μW)	Area Utilization
1. TOT counters, flip-flops for TOT storage, 7 mem, asynch read	4.8	**6.26**	**89%**
2. No TOT counter, latches for TOT storage, 7 mem, asynch read	5.6	6.54	85%
3. TOT counters, latches for TOT storage, 7 mem, asynch read	4.98	5.8	80%
4. TOT counters, latches for TOT storage, 7 mem, synch read	4.84	5.6	80%
5. TOT counters, latches for TOT storage, 8 mem, synch read	5.2	6.1	82%
6. Same as 5. with **Integrated Clock Gating cells**	4.68	**5.38**	**80.5%**

[*S.Marconi et al.*, TWEPP 2016]

- *Results*: **area improved, hit loss reduced** (additional memory)**, power variations reduced**
- **Further optimizations ongoing** (multi-bit latches, clock tree optimisation, etc …)

CONCLUSIONS AND FUTURE WORK

- **Conclusions**
  - High-level simulation and verification framework with enhanced reusability available
  - Selected architectures for the pixel array logic:
    - performance assessed and compared
    - architectures further optimized for area, power and efficiency
    - power methodology used to guide design choices
  - Radiation: SEU to be taken into account in the verification process (TID not discussed in this presentation)
- **Main further developments:**
  - Finalize pixel array logic for RD53 big scale prototype
  - Possibly: further power optimisation to reduce system budget
  - Extensive verification under radiation: design to meet timing with TID and simulate SEUs

BACKUP

Low-power analysis and optimization methodology

Design flow

System design and simulation
Cadence Incisive

Logic synthesis
Cadence RTL compiler

Implementation
- Floorplanning
- Placement
- Clock tree synthesis
- Optimization (multiple stages)
- Routing

Cadence Innovus

Signoff analysis and verification

Power flow

RTL/gate level power
RTL compiler

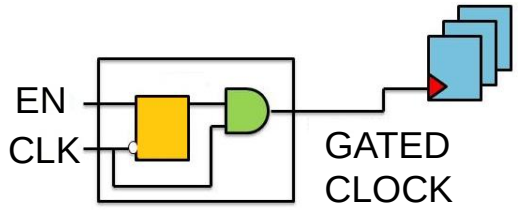
Post-P&R power analysis (actual parasitics)
Cadence Voltus

Main steps:

1) **power analysis at gate-level (i.e. after synthesis to gates):**
   - **drive architectural choices**

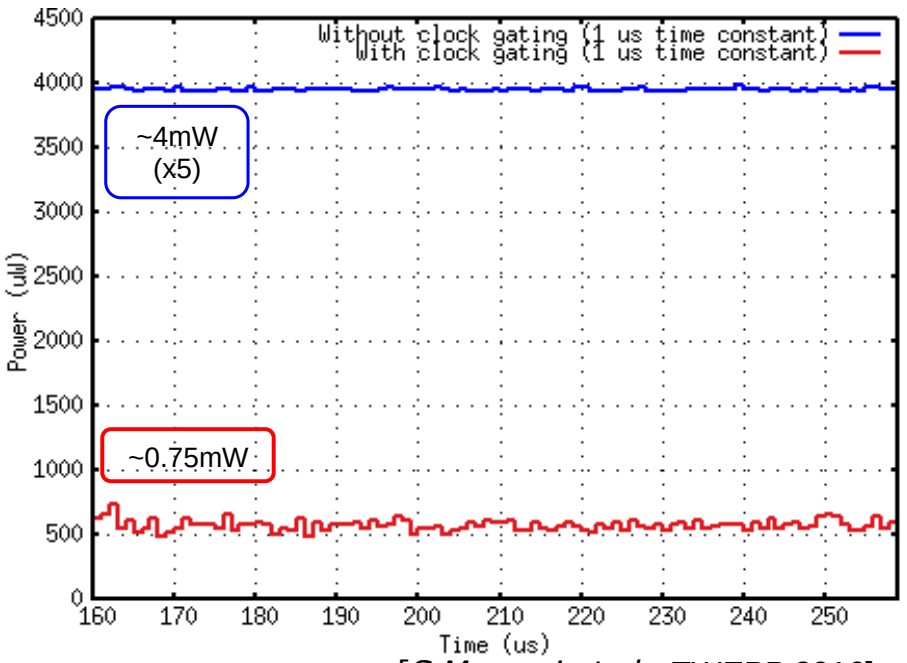
One fundamental architectural choice **use of the clock gating technique**

- source of power variations
- **initially discouraged to keep power more constant**



Power variations at gate-level description (64x4 array):

- **more than x5 power increase to keep power constant can not be tolerated** based on chip specifications
- **power variations** seen from the powering system **acceptable**



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