Results on CHIPIX65 demonstrator: a prototype of New Generation Pixel ROC in 65nm CMOS technology

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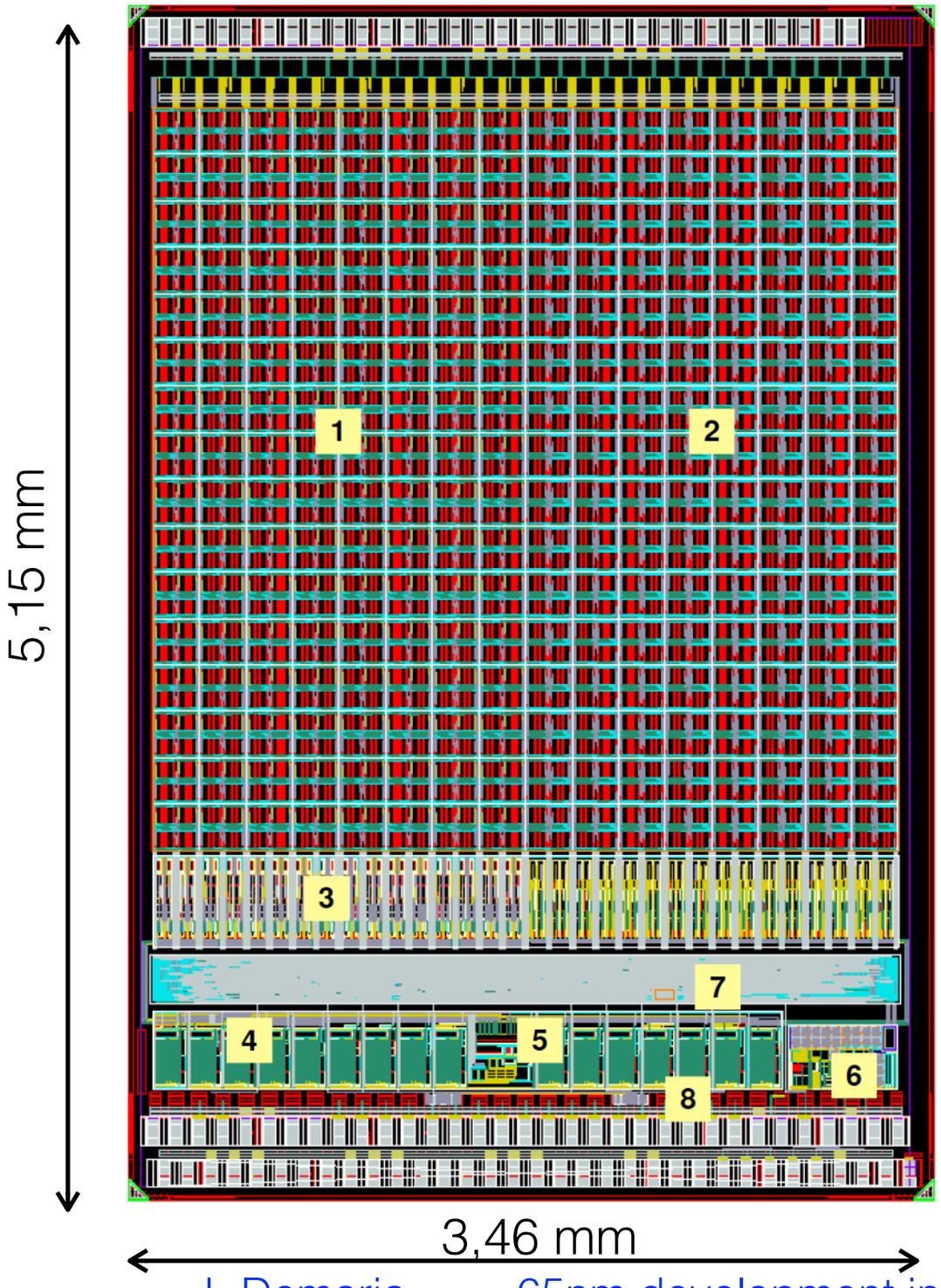
CHIPIX65 demonstrator



1) (32x64) pixels with Synchronous FE architecture

2) (32x64) pixels with Asynchronous FE architecture

3) replicated Bias Cells with current mirrors

4) 10-bit biasing DACs

5) Bandgap voltage reference

6) 12-bit monitoring ADC

7) readout/configuration digital block and High-speed Serializer at the chip periphery

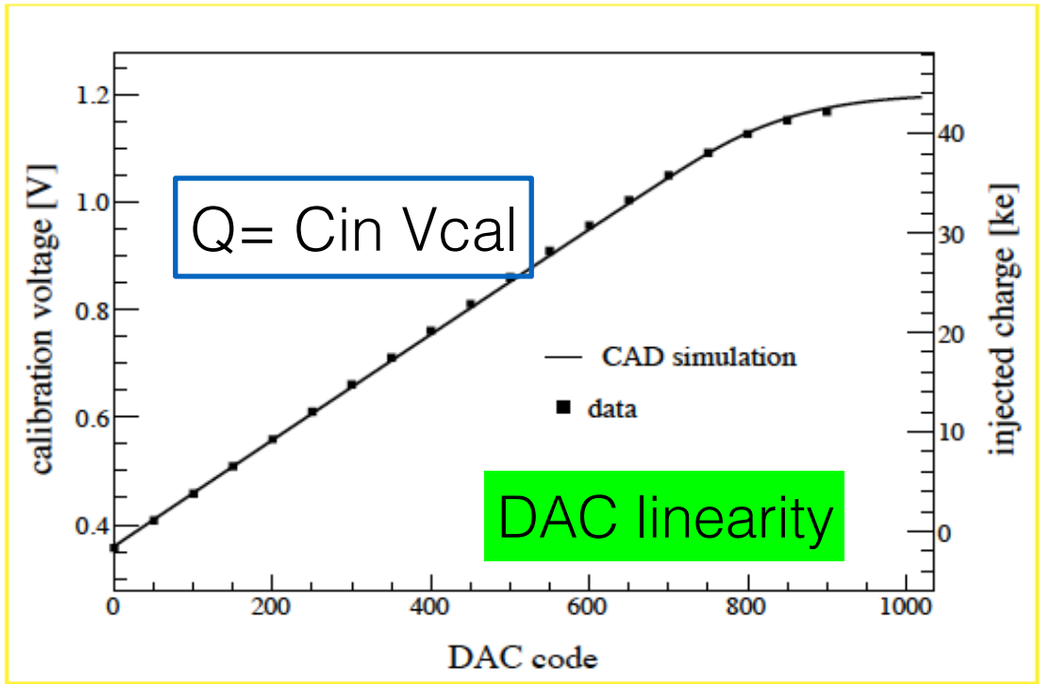
8) SLVS transmitters/receivers and I/O cells

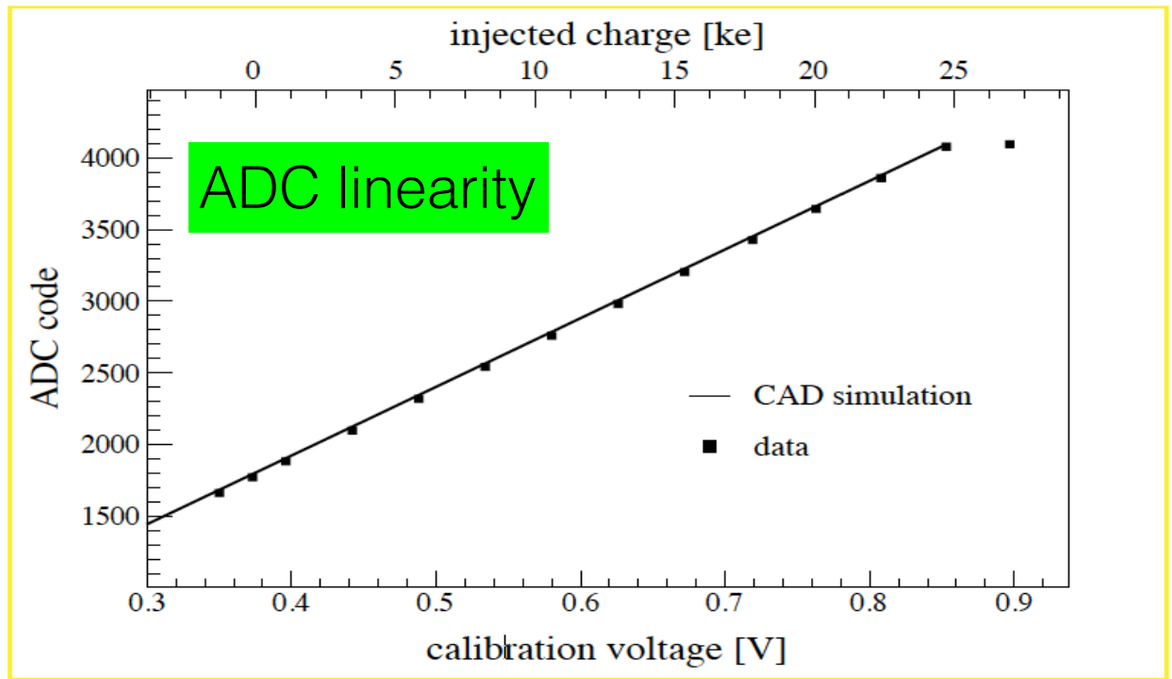
submitted: 5/7/2016
Arrived: 26/9/2016

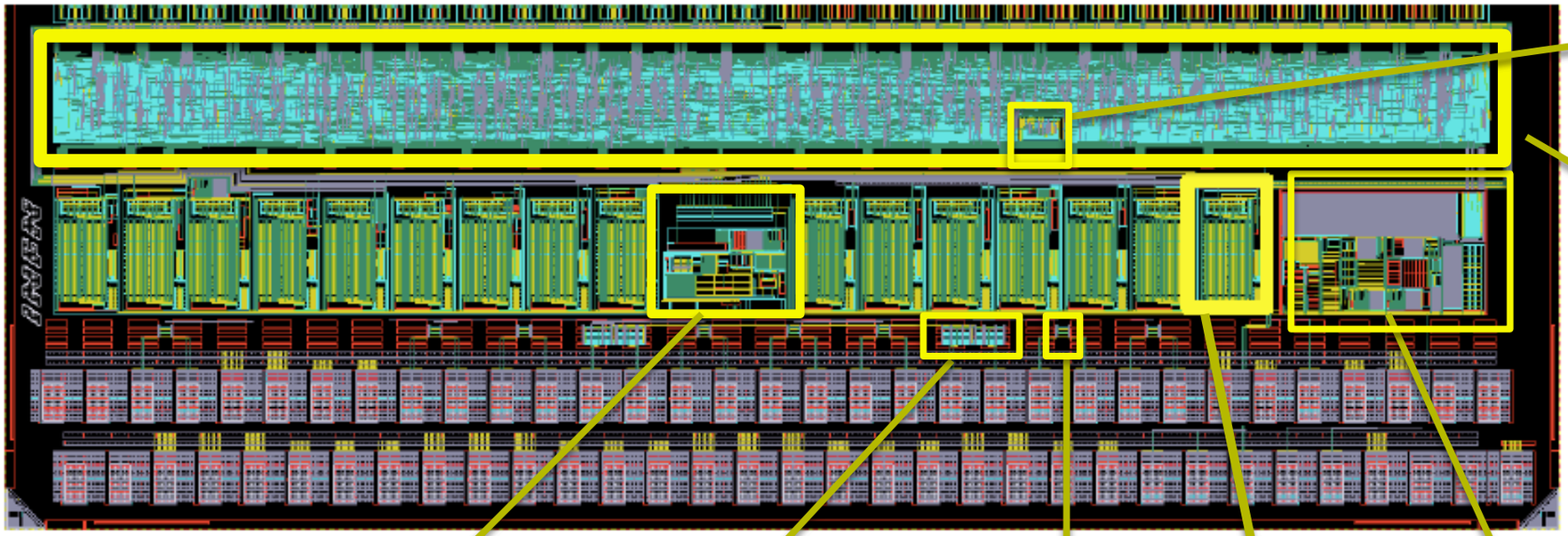
Building Blocks made by CHIPIX65: summary table

BLOCK	DIMENSIONS	POWER	Performance / Main-Characteristics
Band-Gap	$100\times270\ \mu m^2$	65 μW	based on MOS only
10-bit DAC	$140\times240\ \mu m^2$	150 μW	DNL $<$ 0.4 LSB, INL $<$ 1LSB
12-bit ADC	$308\times535\ \mu m^2$		1V, 16-ch, 5kSample/s
SER	$100\times56\ \mu m^2$	2.3 mW	2 Gbps
DES	$180\times56\ \mu m^2$	17.8 mW	2 Gbps
sLVDS-TX	$160\times160\ \mu m^2$	2 mW	1.2 Gbps
sLVDS-RX	$70\times80\ \mu m^2$	0.2 mW	1.2 Gbps
Dice S-RAM	$1.8\times3.3\ \mu m^2$		SEE recover in 2.5ns
VFE-syn	$25\times40\ \mu m^2$	5μW	ENC $<$100 fF; Thr-trimm: offset-comp ToT(30ke$^-$) = 270ns, $\leq$7-bit with local oscill
VFE-asyn	$25\times50\ \mu m^2$	5μW	ENC $<$100 fF; Thr-trimm: 4-bit DAC comp ToT(30 ke$^-$) = 400ns $\leq$ 5-bit ext-clock 80MHz

CHIPIX65 periphery







Serialiser

Digital-Chip-bottom

EndOfColumn FIFOs, CentralFIFO, 8b10b Encoder, Auto-zero, SPI-protocol

BandGap

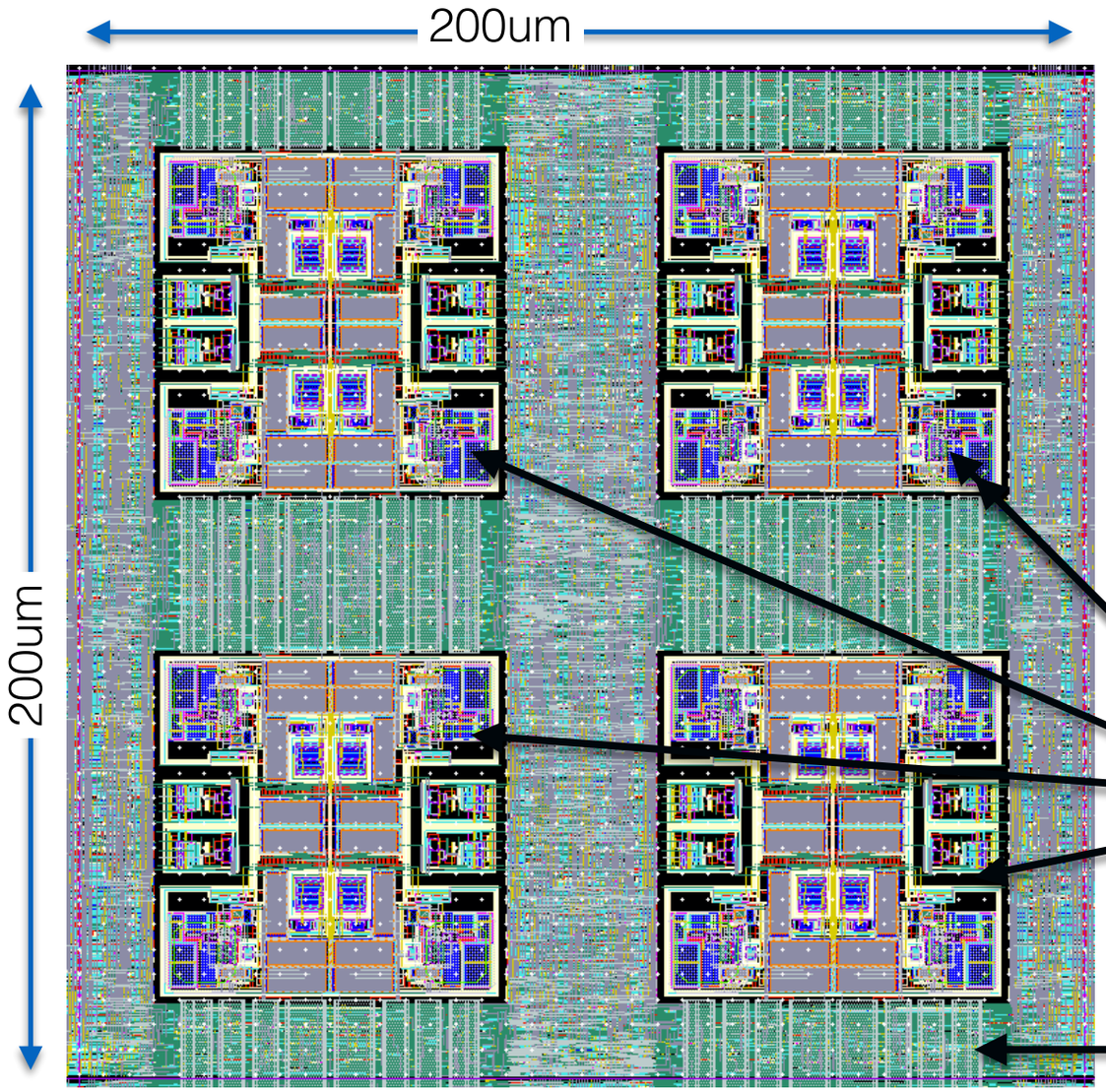
sLVS-Tx

sLVS-Rx

DAC
(16 in total)

ADC

CHIPIX65 Regional architecture extended to (4x4) pixels



Pixel region provides :

- pixel configuration register
- ToT counting
- Local storage waiting trigger
- Trigger matching (zero-suppr)
- Readout to end-of-column

Analog VFE in four (2x2) islands

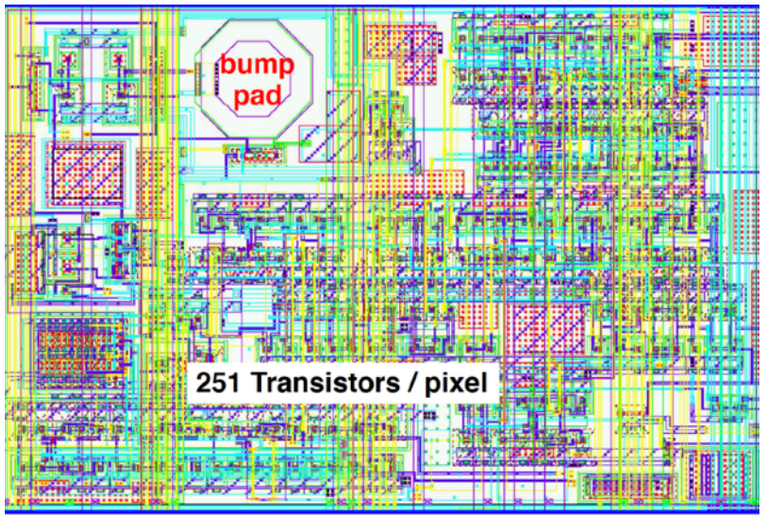
Digital architecture logic distributed in the (4x4) Region

AREA for digital is tight: idea is to make real use of sharing digital resources among more pixel

- FEI4 architecture NOT convenient for regions larger than (2x2)
- NEW architecture developed by CHIPIX65 based on (4x4)

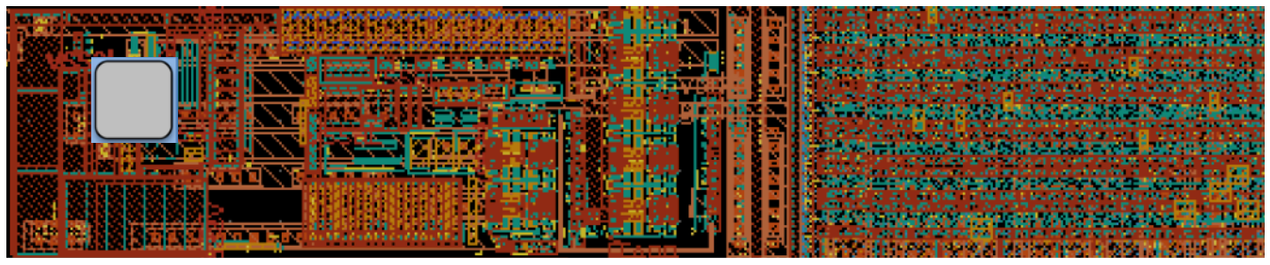
Some comparison…

PSI46 (150um x 100um)



- 250nm CMOS tech
- **251** transistors/pix

FEI4 (50um x 250um)

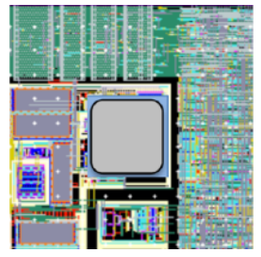


- 130nm CMOS techn
- ~**2500** transistors/pix
- ~0,5 trans/um^2

YES !

65nm technology allows to design a smaller pixel capable to sustain extreme particle fluxes and long latencies

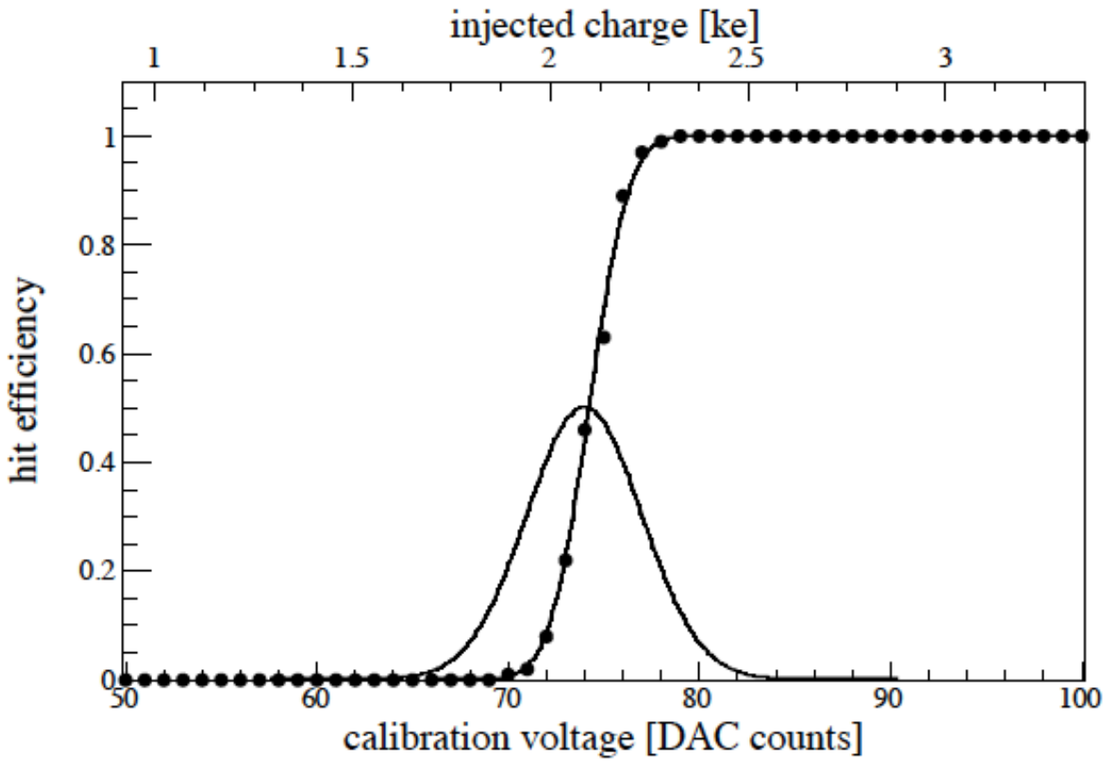
CHIPIX65 (50um x 50um)

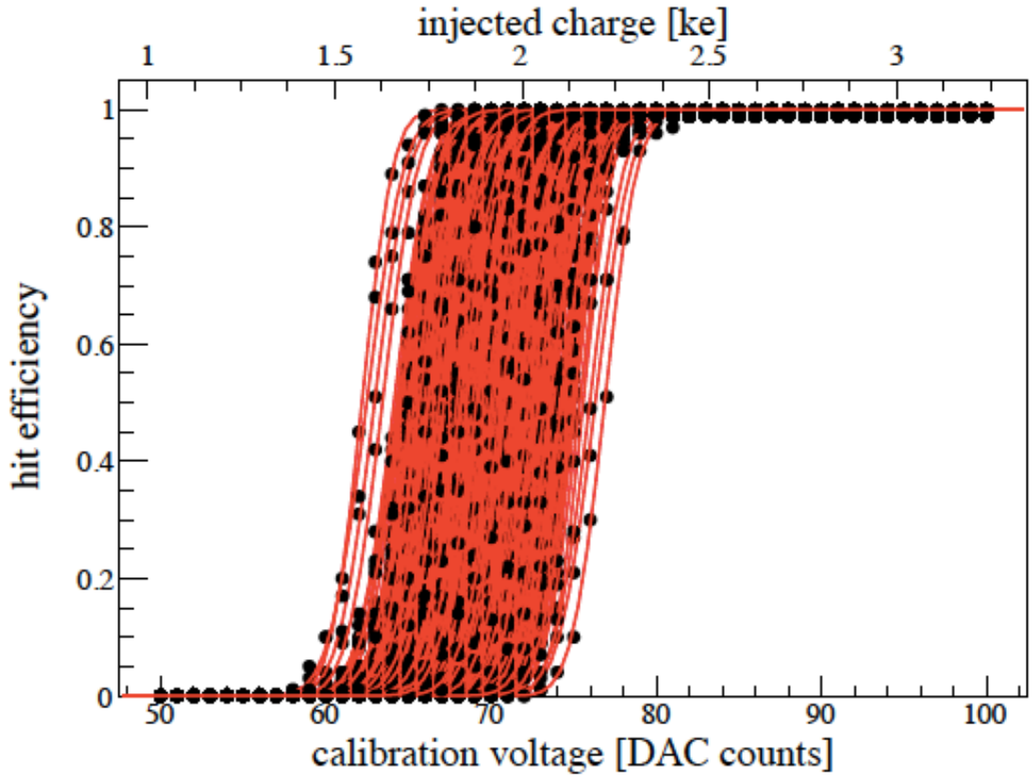


- 65nm CMOS tech
- ~**2500** transistors/pix
- ~2 trans/um^2

50% of area to digital

Measurement of Threshold and noise
S-Curve: Charge scan

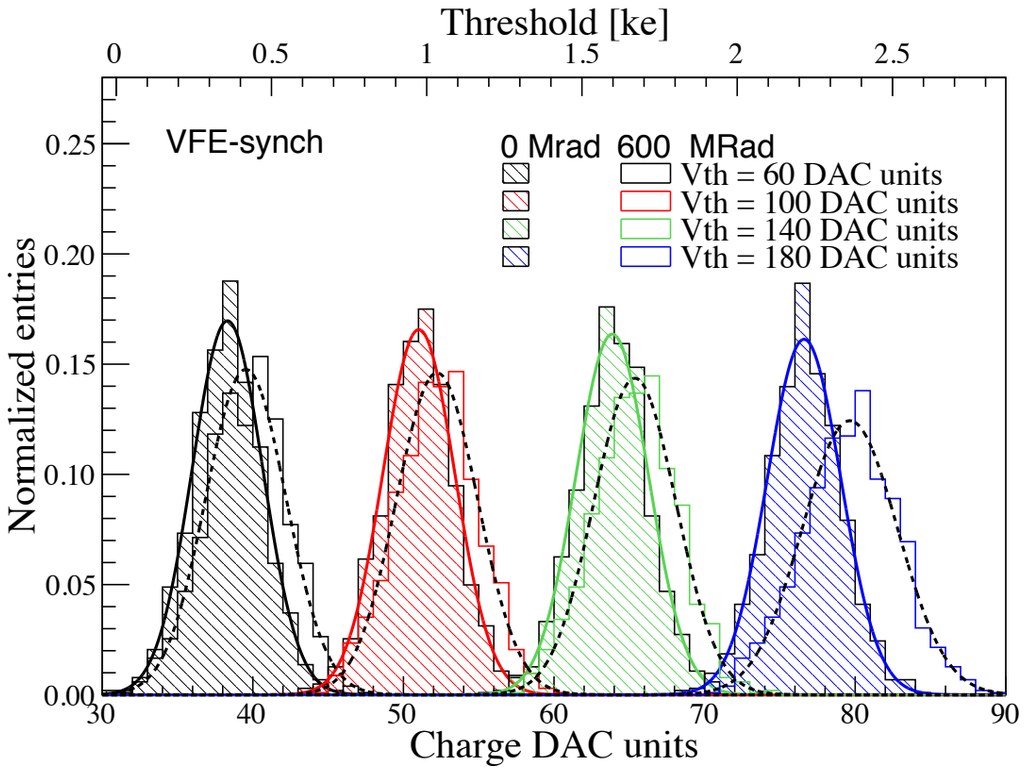




- all pixels tested and fully working
- autozeroing performed each 200 μs
- effective NOISE and THRESHOLD values determined by means of S-curves
- measurements performed with CHARGE SCANS and FIXED THRESHOLD
- HIT EFFICIENCY recorded for 100 charge-injection pulses
- measured points fitted using an error function (sigmoid)
- noise and threshold values extracted from means and variances distributions

Synchronous VFE (Torino)

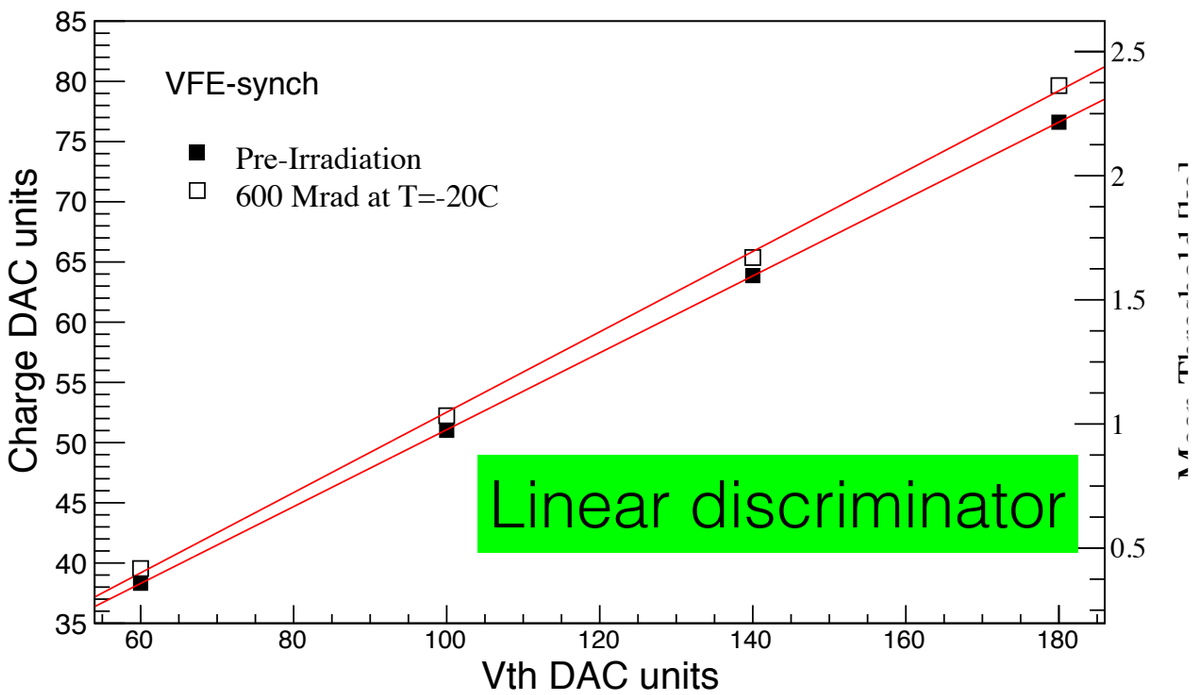
Low Threshold

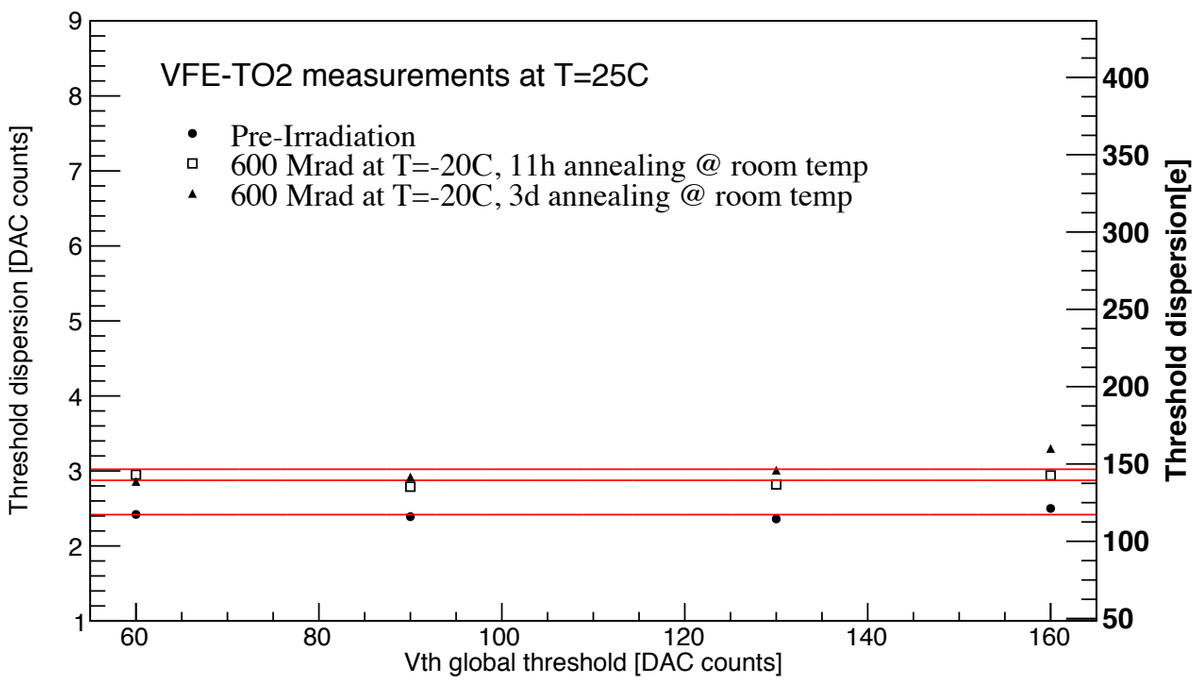


- Low threshold possible, **250-300e**- for bare chip
- The **auto-zeroing** is working well

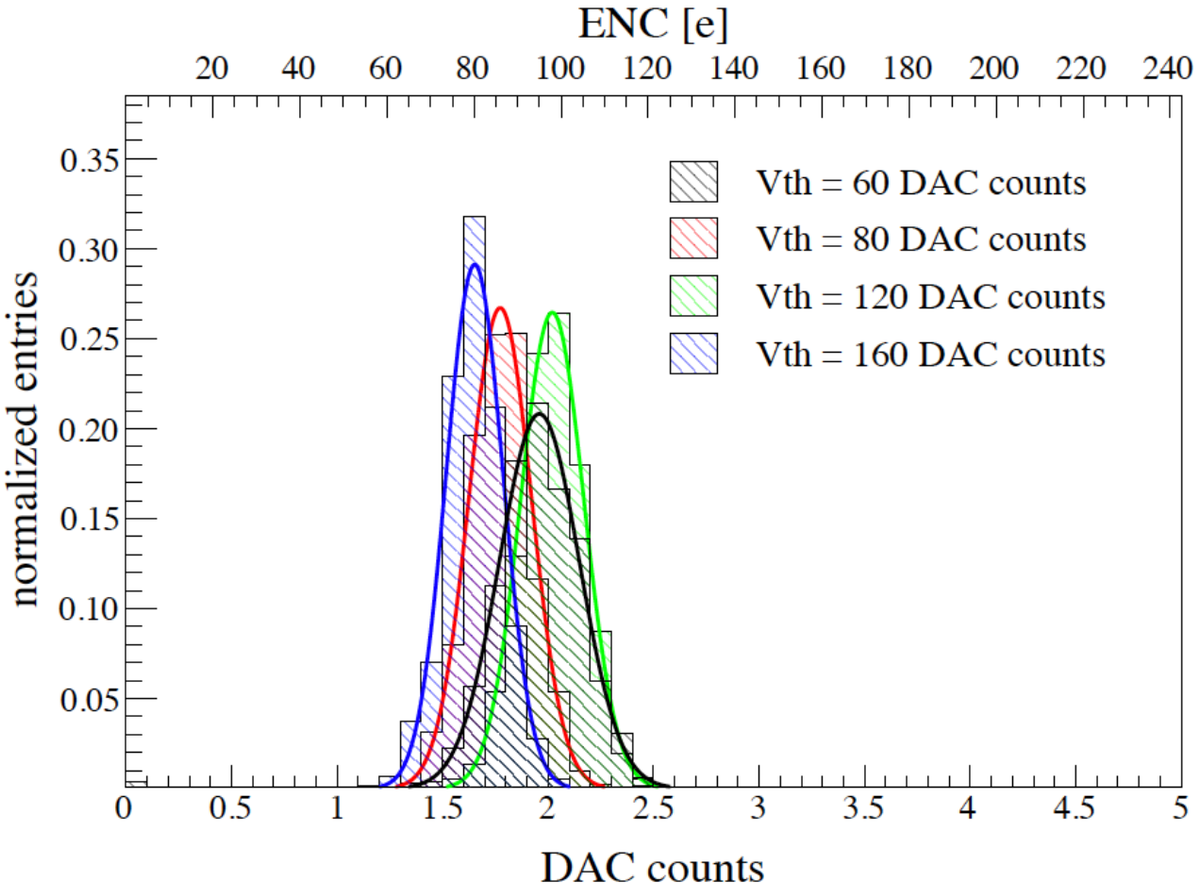
- The measurements have been repeated after a TID = 600 Mrad has been reached with X-ray irradiation at -20°C with the chip in working conditions.**The irradiated chip is still fully operational**

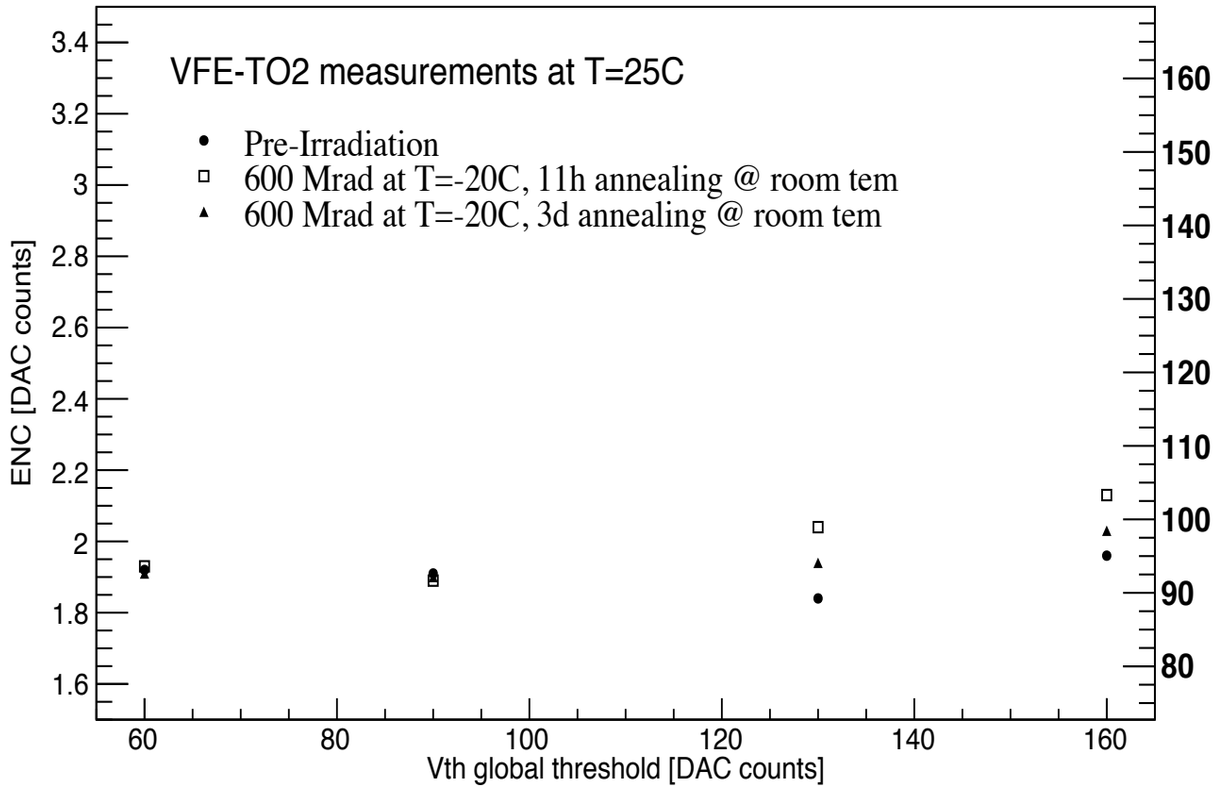
- For thresholds below 1 ke$^-$, which is the region of interest, the increase of the dispersion with radiation is below 10%





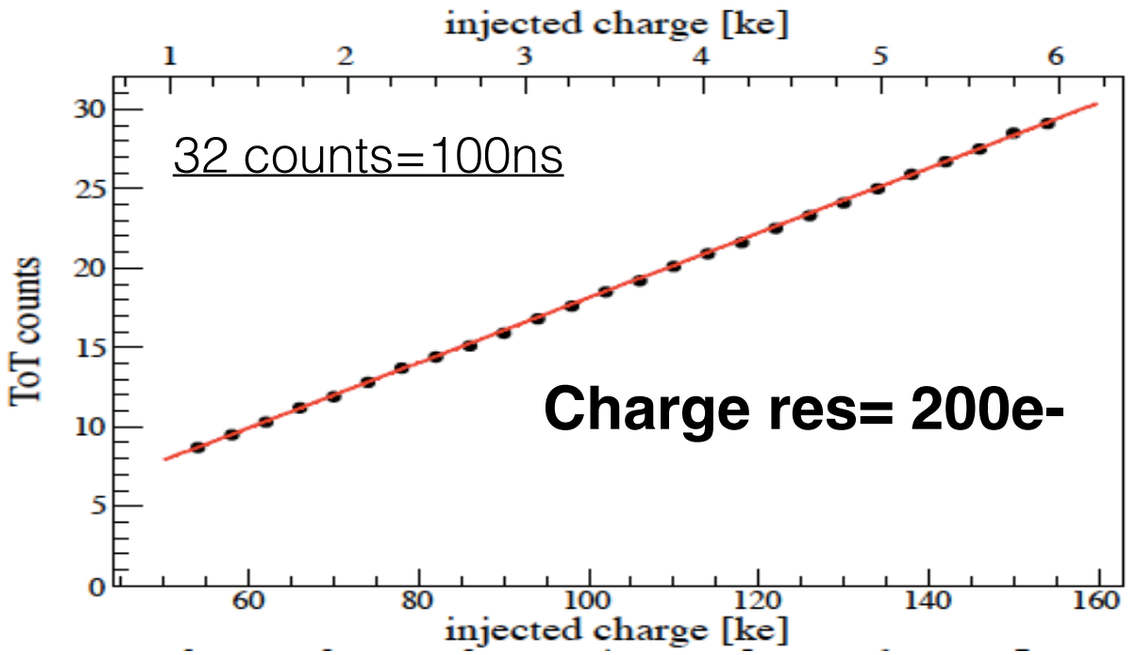
ENC



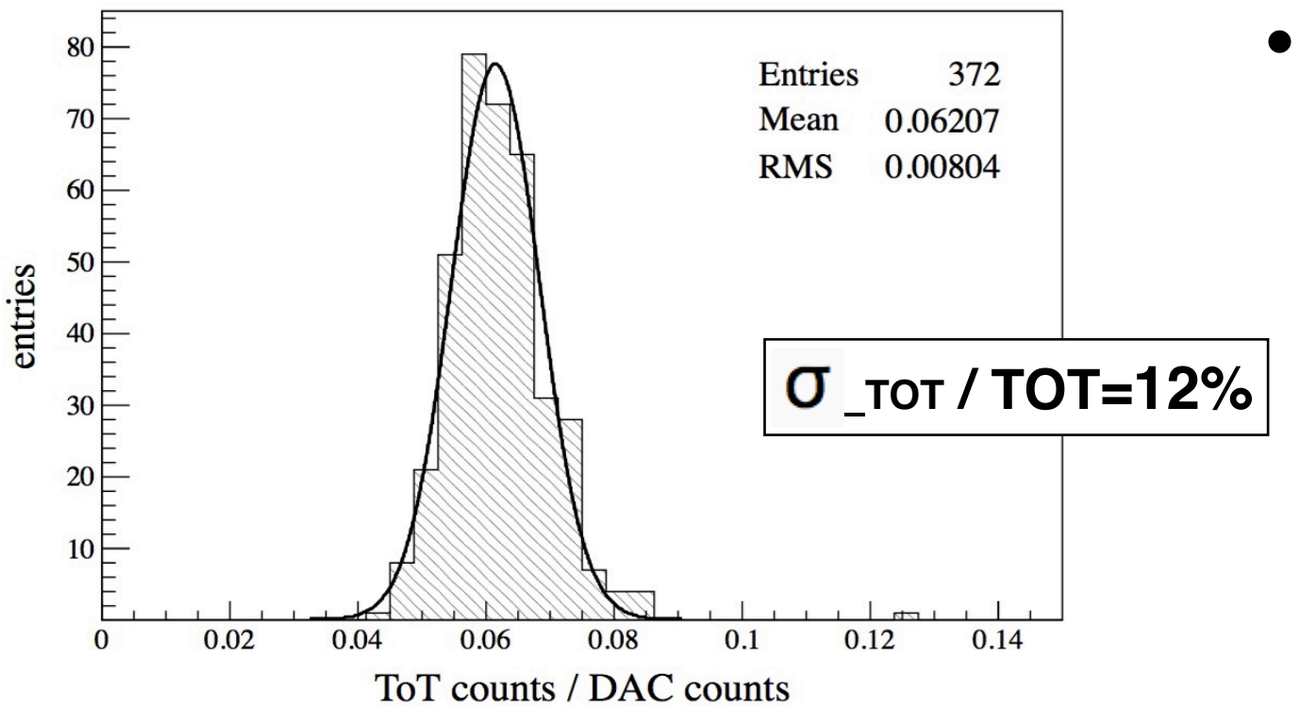


- ENC ~ 90e- : very low noise performance despite digital activities
- Almost no increase of noise after irradiation. Value for Vth=60-90 are relevant

Fast ToT measurements



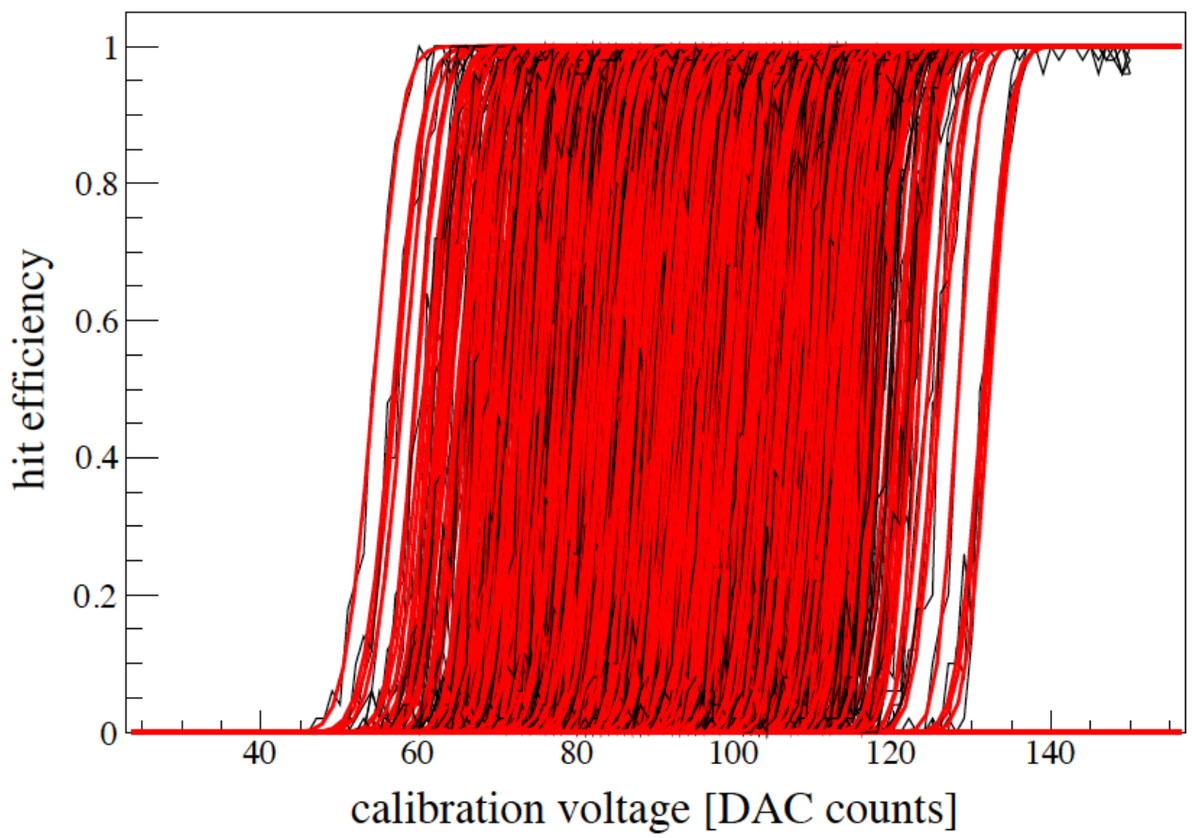
- **Good ToT Linearity - 5 bit ToT**
- Measurement with **320MHz Fast ToT**

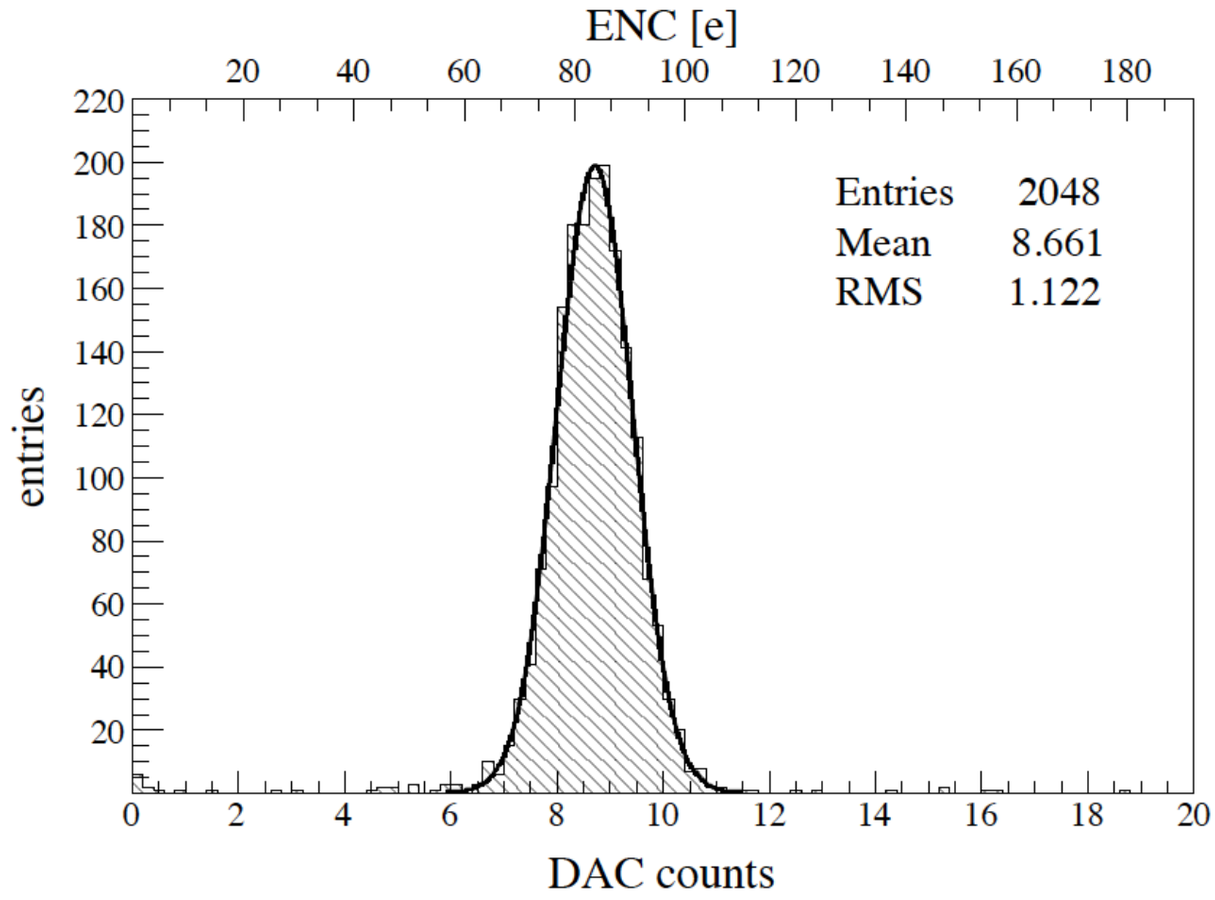


- Decrease of <20% in frequency after 600 Mrad irradiation

Asynchronopus VFE (Pv/Bergamo)

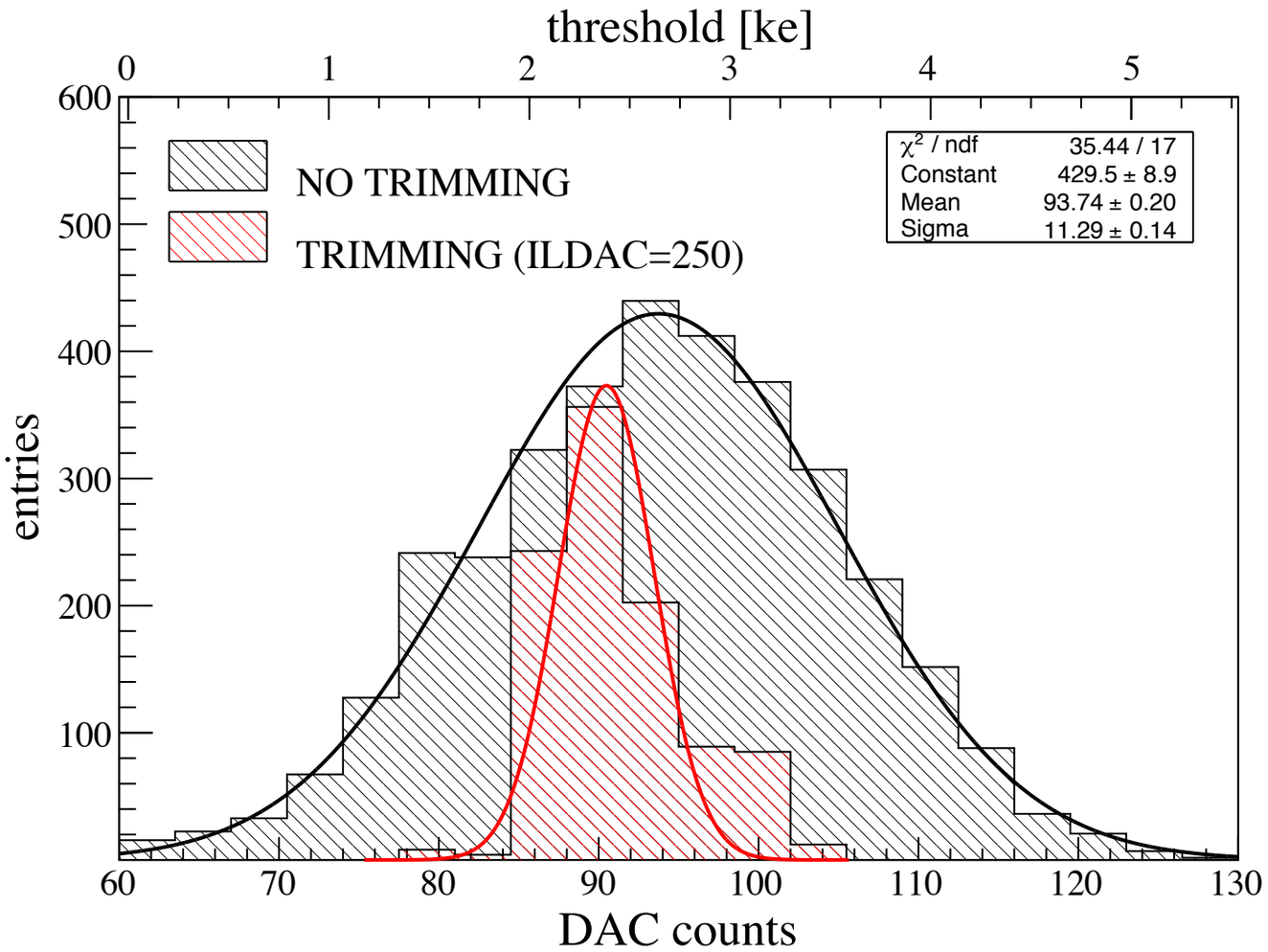
Threshold & Noise





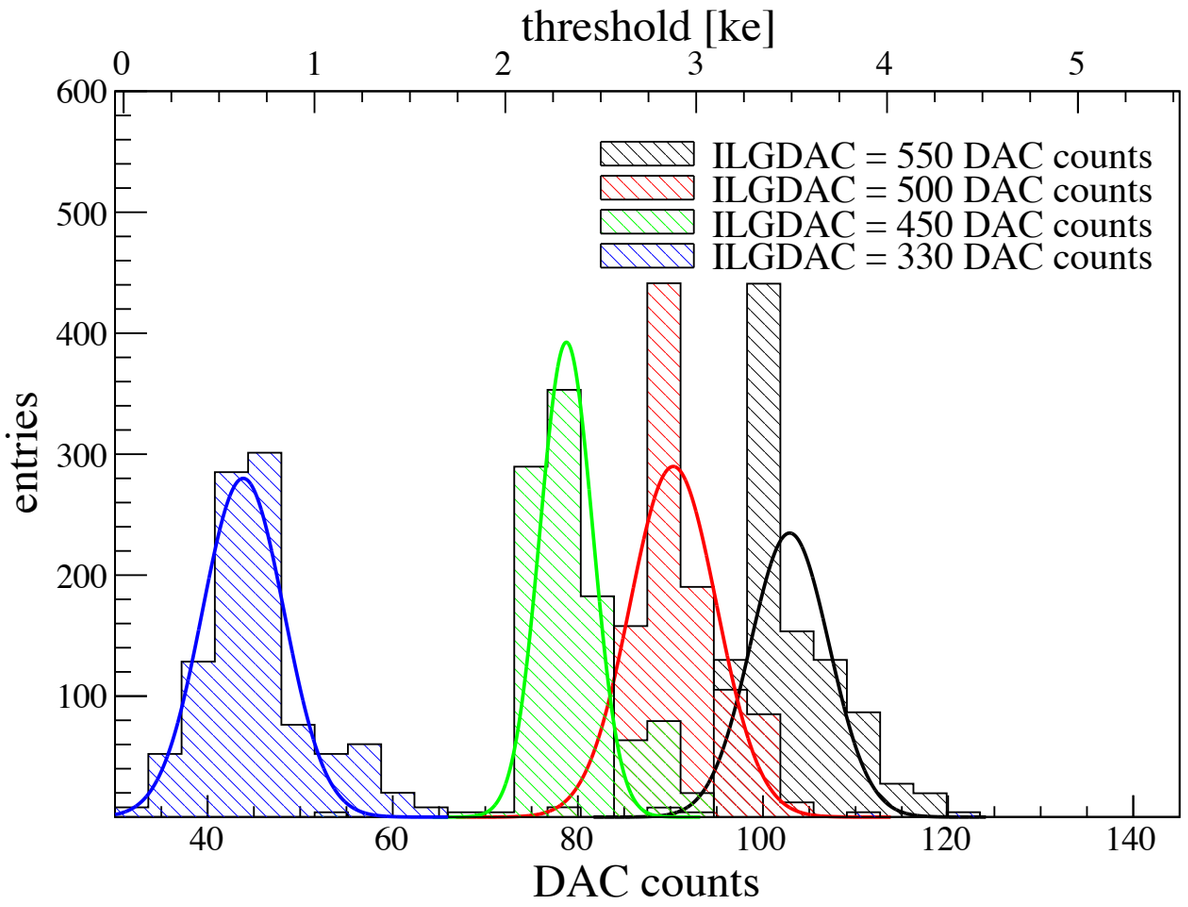
- About 450e- threshold dispersion before trimming
- Noise compatible with simulations ~ 90e-

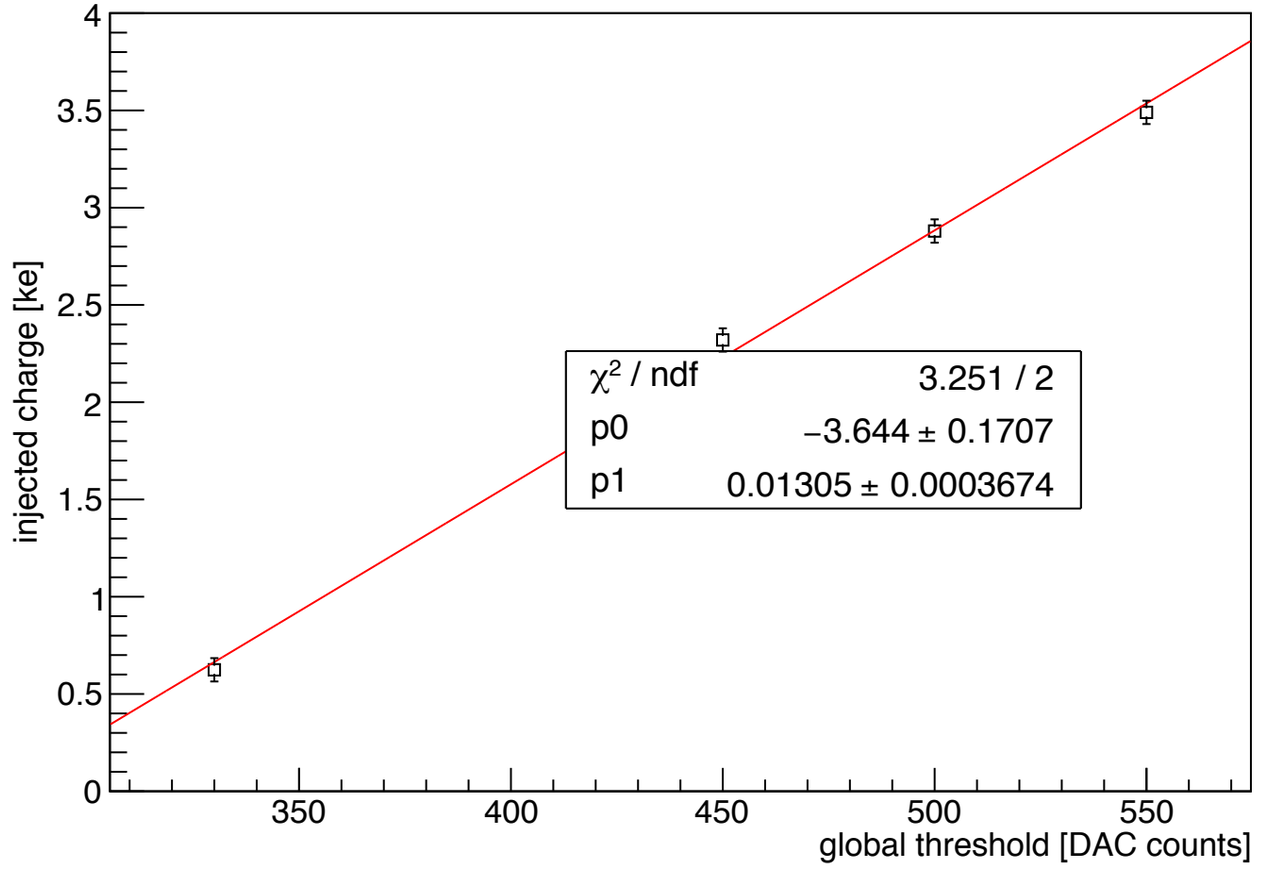
Threshold trimming



- The local DAC for trimming works fine,
- Here preliminary results: trimming tuning algorithm not optimised

Threshold





- Linear behaviour of Discriminator

Conclusions

- The CHIPIX65_demonstrator is a very sensible intermediate step before moving to the big prototype of RD53A. Several solution studied in CHIPIX65 have been introduced into RD53A.

- CHIPIX65-FE0 is respecting the requirements imposed by Phase 2 HL_LHC pixel detectors : high efficiency for high particle flux, low-noise, high granularity

- The chip works fine, nothing found not to function well.

- CHIPIX65-FE0 resisted very well an irradiation test up to 600 Mrad (made at cold, -20C). Also digital logic, readout works perfectly. This is very promising !

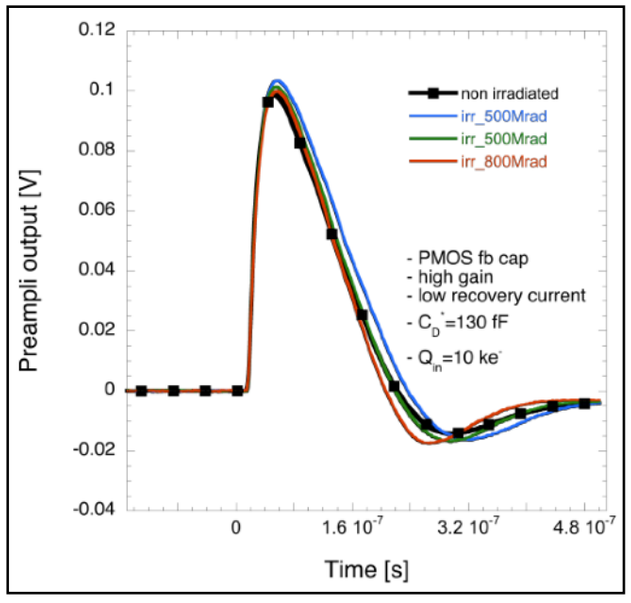
- Excellent performance of Analog-VFE obtained.

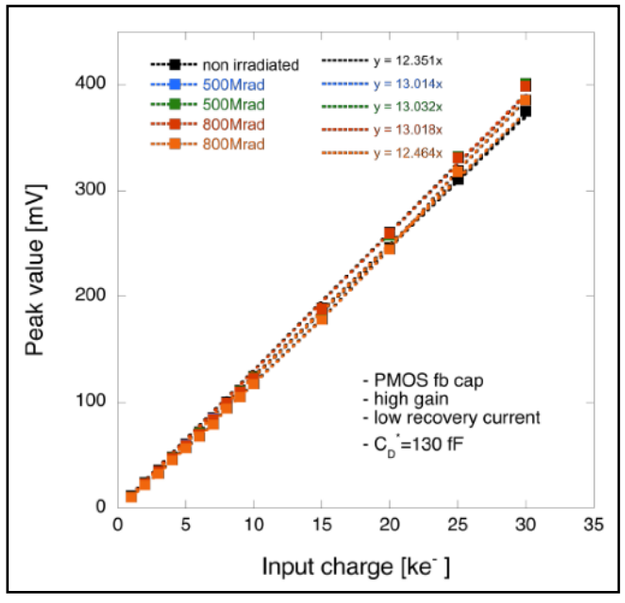
- Next step will be to do bump-bonding with sensors (planar and 3D)

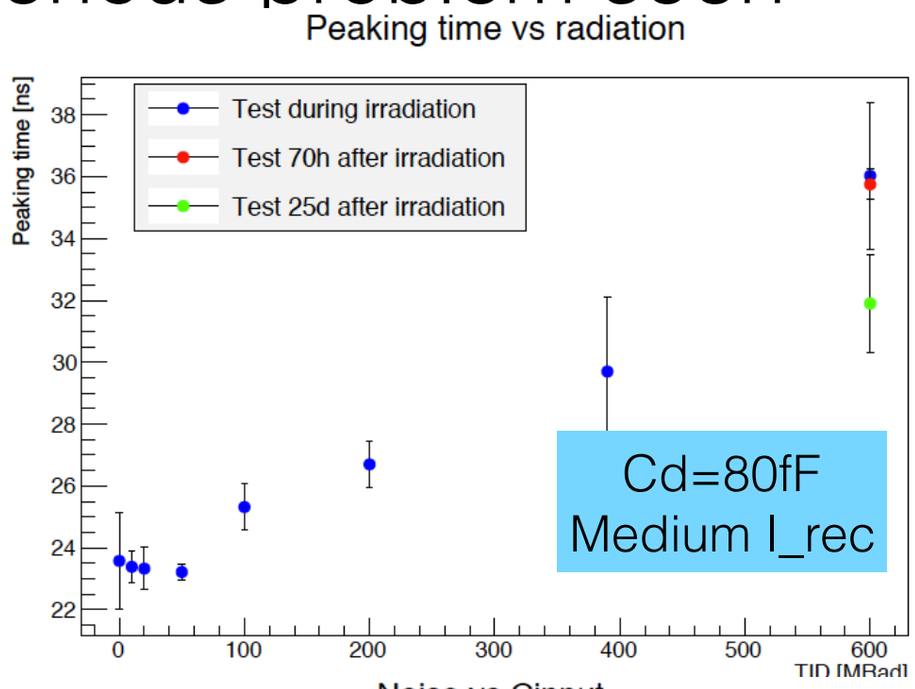
BackUp Slides

Radiation: Analog VFE

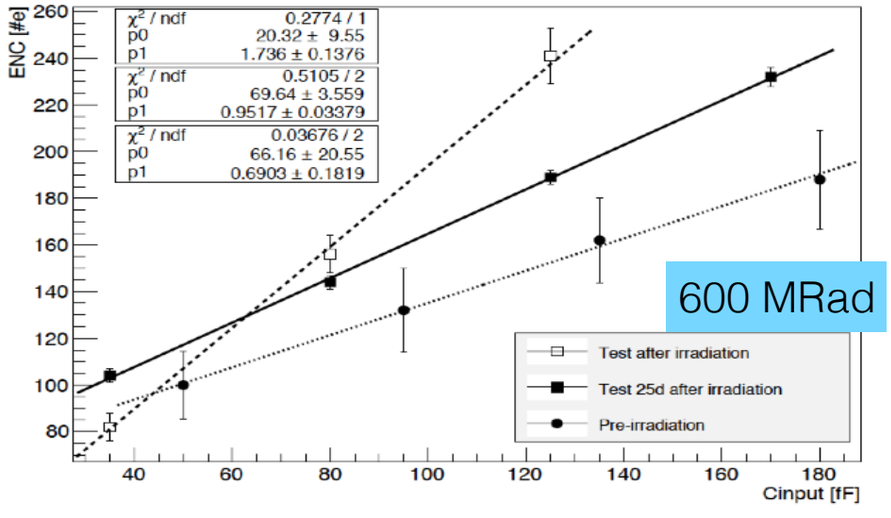
- No major worry: **two out of four analog-architectures tested under radiation** and no serious problem seen





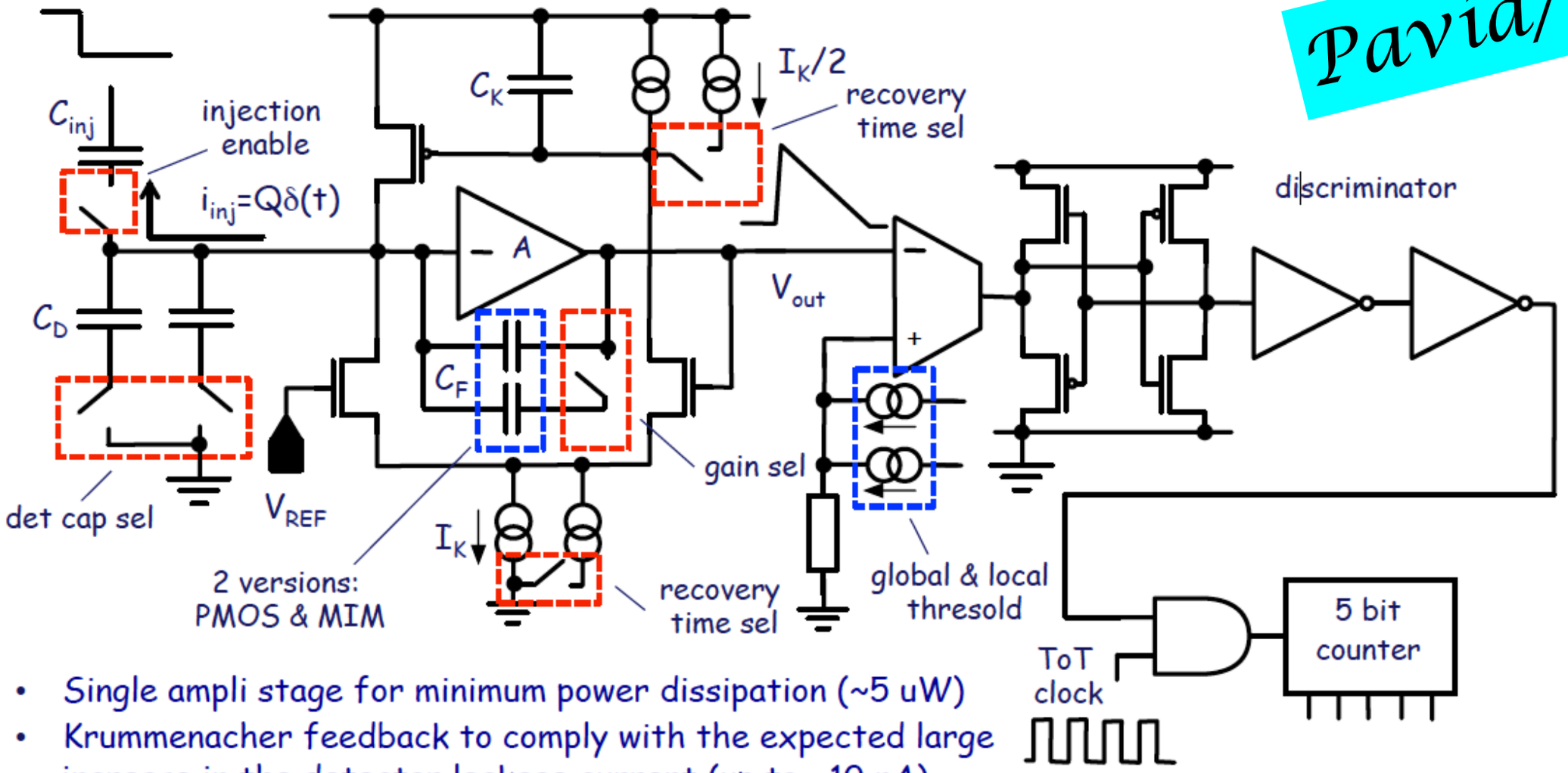


- Gain decrease of ~5%
- Slower signal but looks ok
- 10-20% increase of noise



Asynch Analog FE

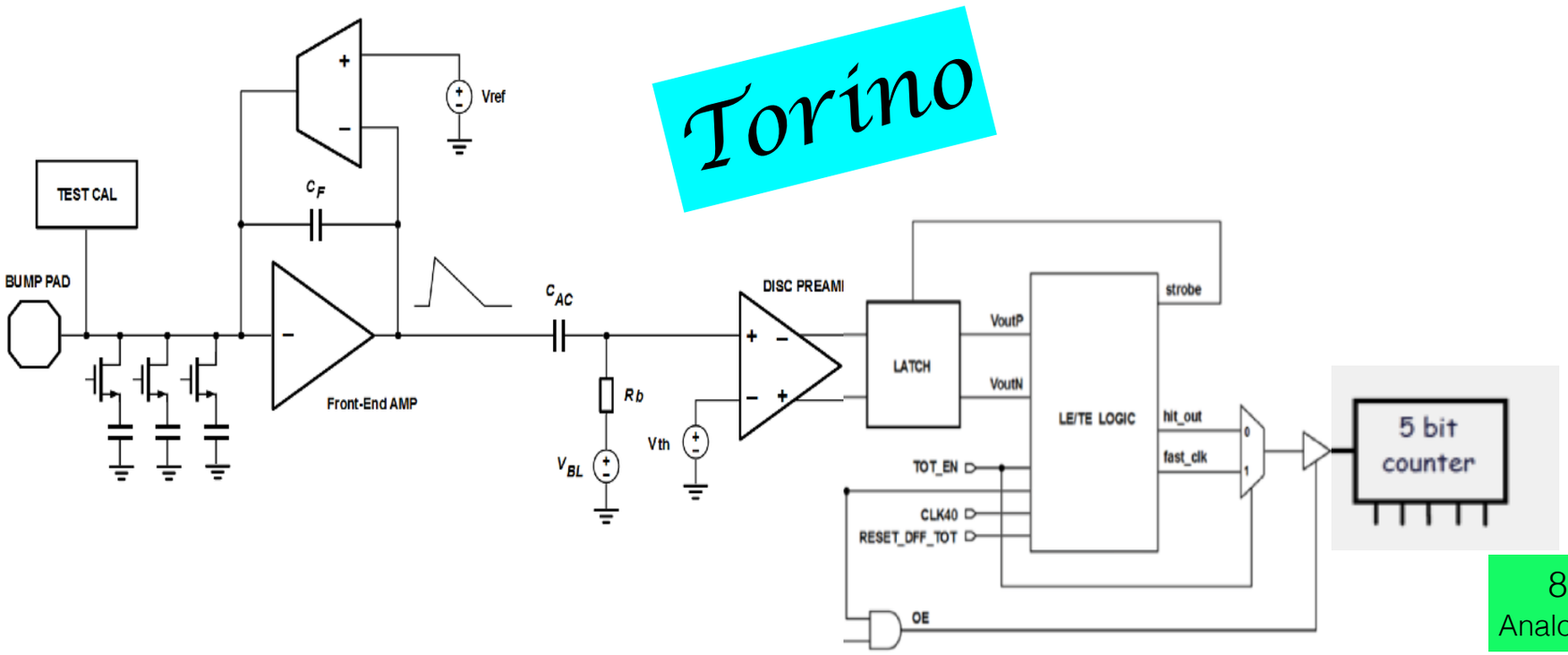
Pavia/Bg

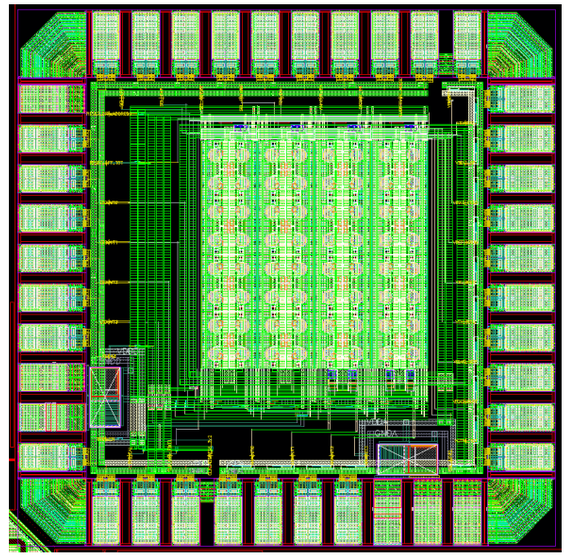


- Single ampli stage for minimum power dissipation (~5 uW)
- Krummenacher feedback to comply with the expected large increase in the detector leakage current (up to ~10 nA)
- 30000 electron maximum input charge expected, ~450 mV preampli output dynamic range
- Selectable gain, recovery current and detector emulating capacitance
- 40 MHz clock, 5 bit dual edge counter, 400 ns maximum ToT

TESTED after IRRADIATION

Synchronous Analog FE





8x8 pixel matrix submitted and tested
Analog readout of CSA and Discriminator (via buffers)

- **PREAMPLIFIER**
  - One stage CSA with Krummenacher feedback
- **Synchronous DISCRIMINATOR**
  - (AC coupled to CSA)
  - off-set compensated diff.amplif. + latch;
  - **FAST Time-over-Threshold**
    - Local oscillator strobing Latch (to 800MHz
- **Calibration circuit**
  - digital signal + DC calibration leve

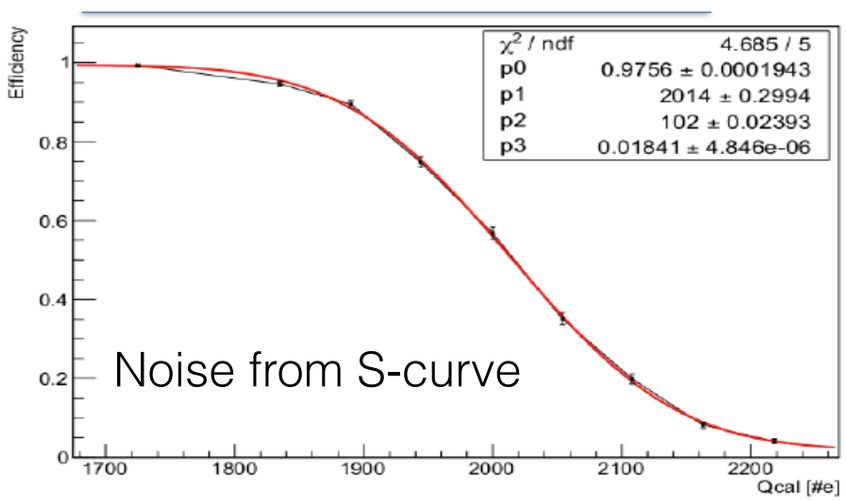
TESTED after IRRADIATION

Performance SUMMARY

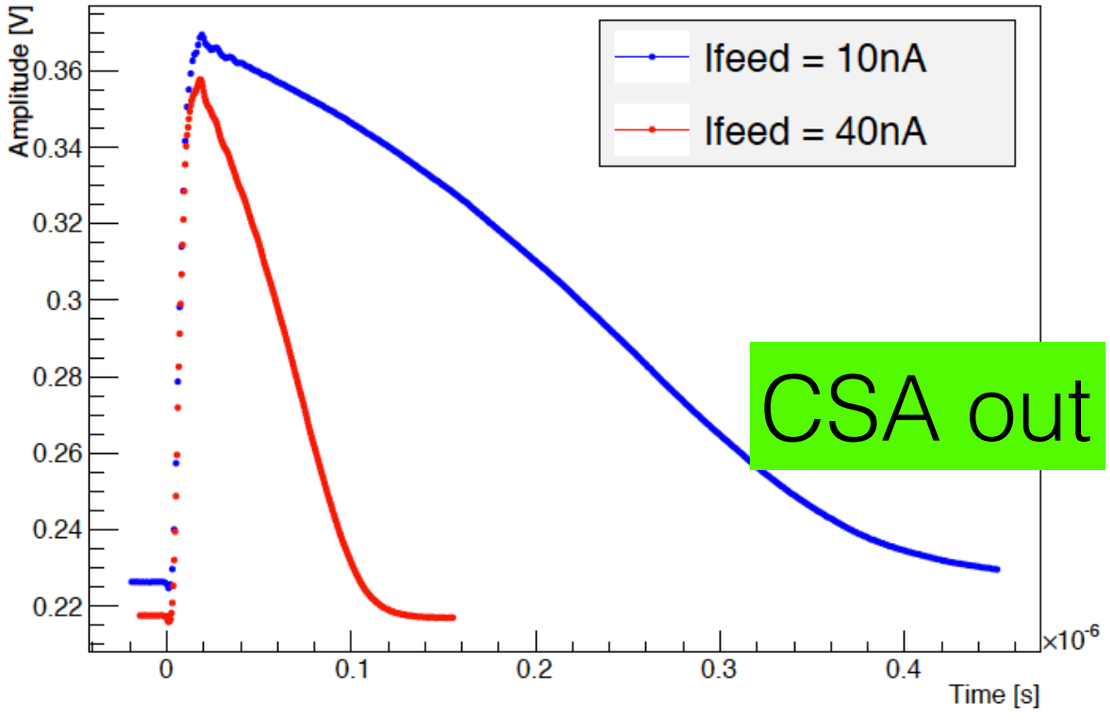
- Compact: ~25um x 40 um
- Low power: < 5.5 uW (with ToT logic)
- Low noise: ENC=100e @C_{det}=100 fF
- Leakage compensation: up to 50nA/pixel
- Fast Charge measurement:
  - 10 ke in : 90 / 180 / 360 ns (Fast/Medium/Low recovery current)
  - up to 7-8bit (125-250e /ADC) - no ext clock
- NO Threshold-Trimming:
  - autozeroing made by hardware

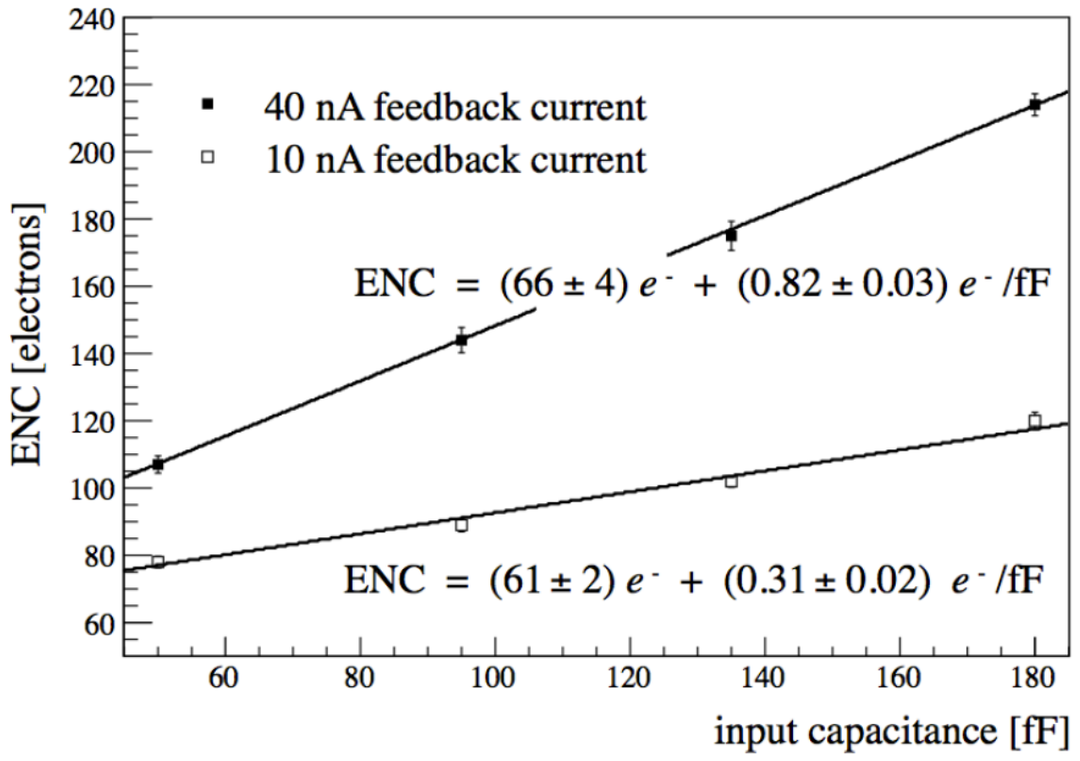
Synch AFE

- CSA: Triangular shape, discharge time (=dead-time) can be set. Krummenaker can stand up to 50nA.
  - 40nA = 90ns for 10ke => <0.3% ineff (FAST) ; ENC=110e-
  - 10nA = 360ns for 10ke => ~1% ineff (SLOW)

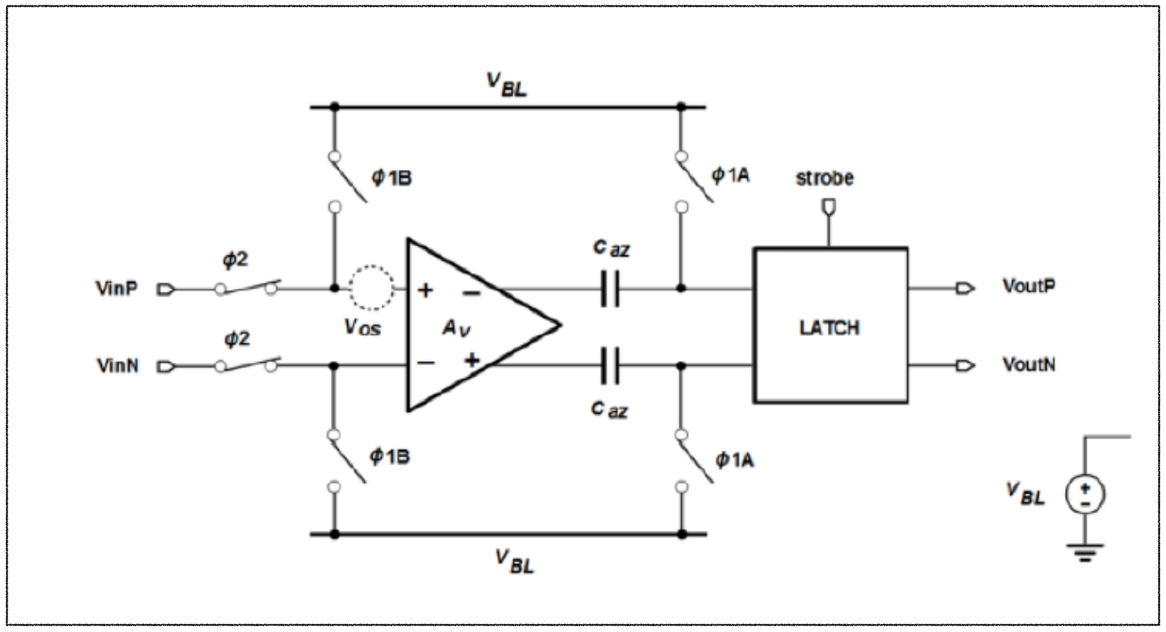


Analog signal (oscilloscope)

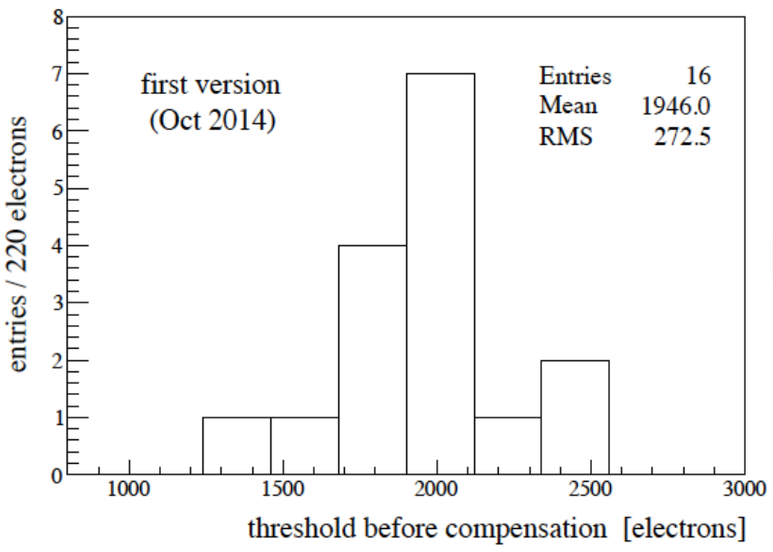




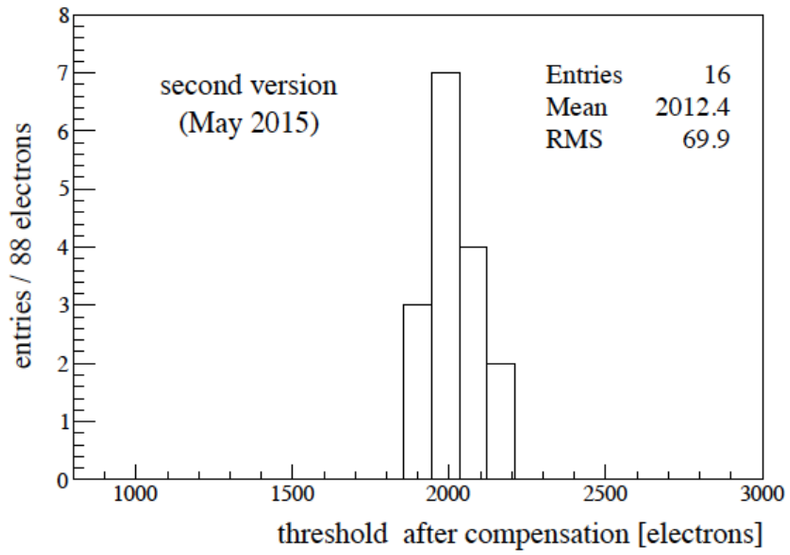
Synch AFE: Threshold variations



- Comparator is AC coupled to CSA
- Differential amplifier is offset compensated every 100usec (still true after irradiation)
- **NO NEED for TRIMMING !**
- Latch dynamic offset dominates but is low: 70e-



offset compensation

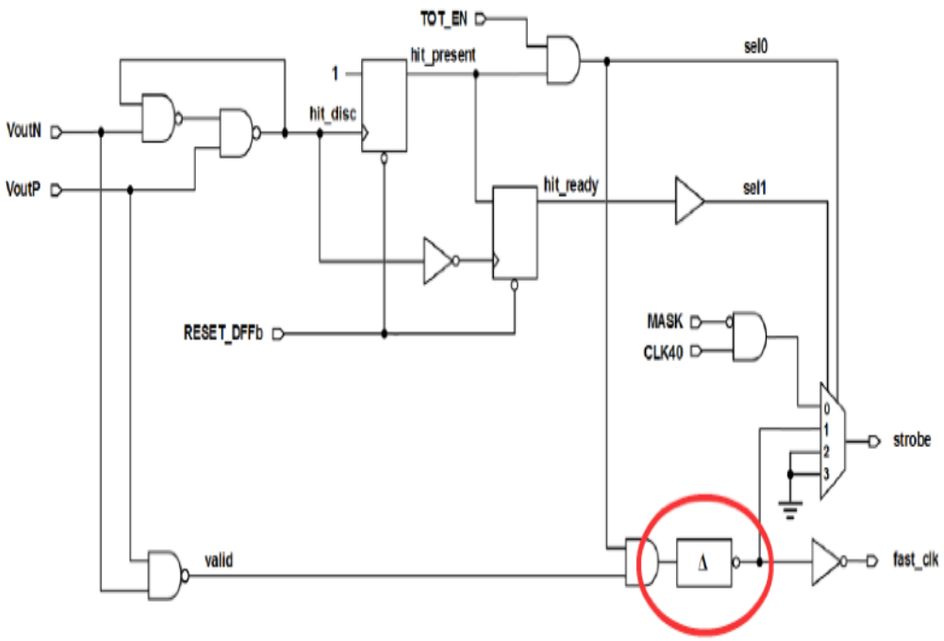


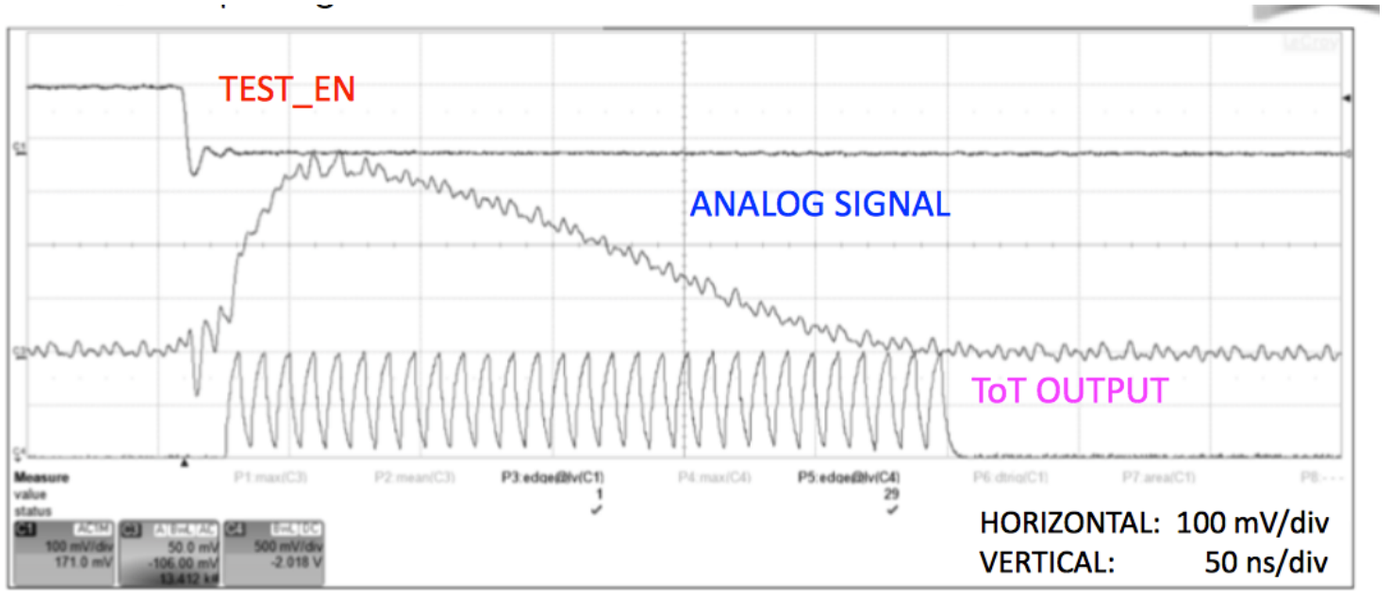
(a) Uncompensated

(c) Compensated - Second prototype

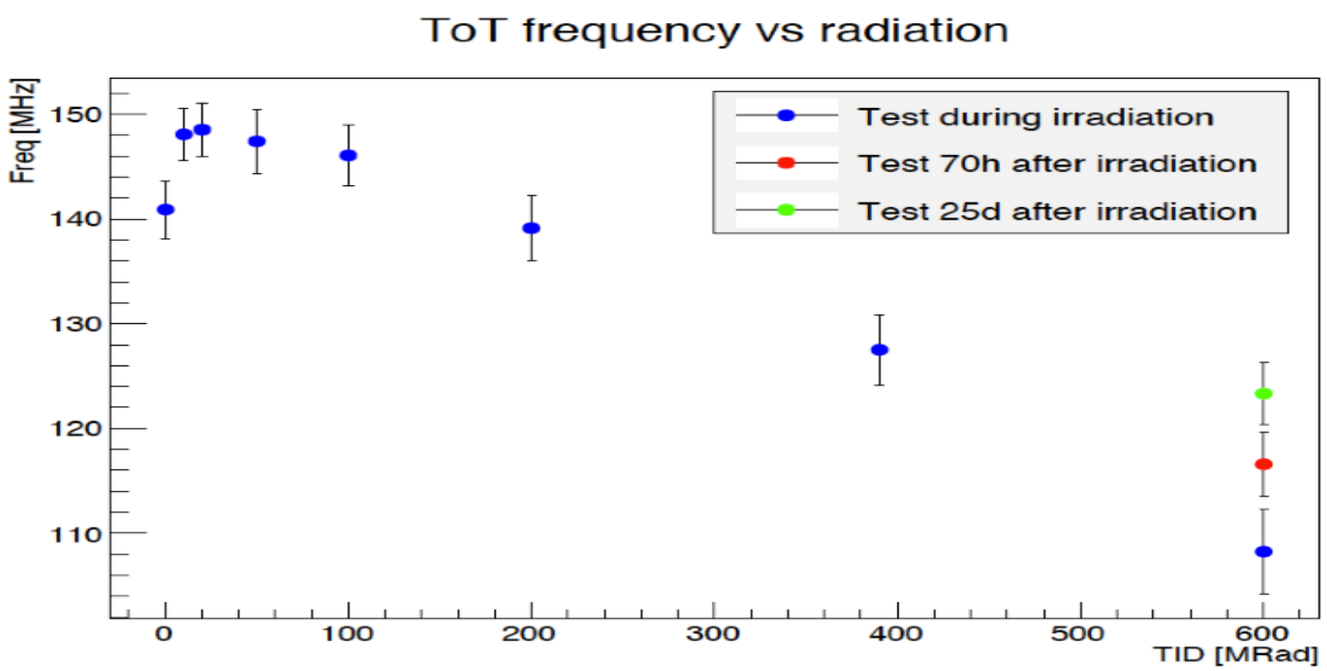
No change after 600 MRad and 25d annealing

Synch AFE: Fast Oscillator

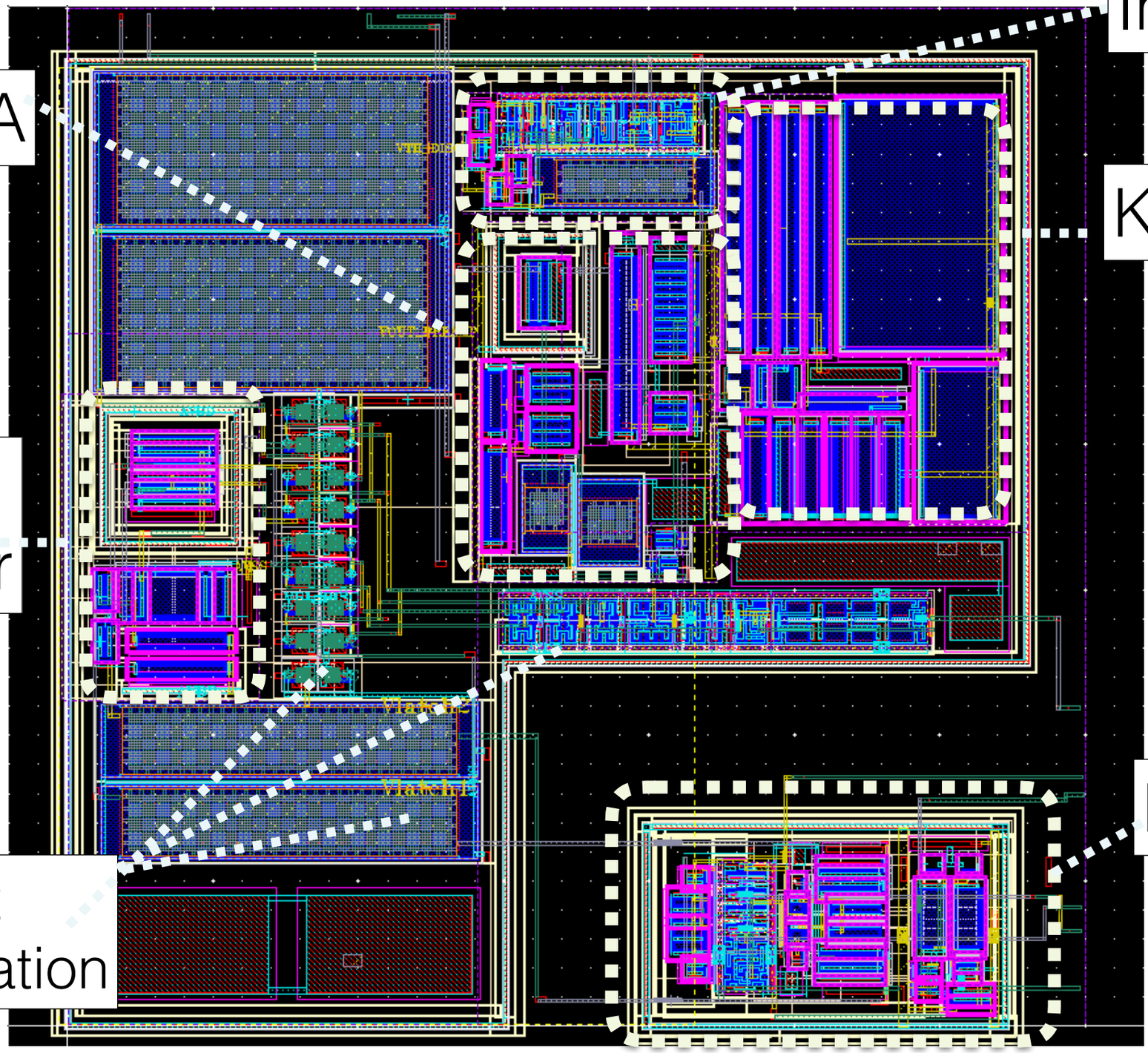




- Local oscillator set to 140 MHz
- Slow down with TID
- Partial recovery with time (annealing)
- Freq. rms ~ 1,8%
- Reminder: Freq. can be set to higher values



Synch VFE



AREA: 35um x 35um to fit with other designs, but could be made smaller

AFE and Latch in different deep n-well