Update on CPPM activities towards development in 65nm

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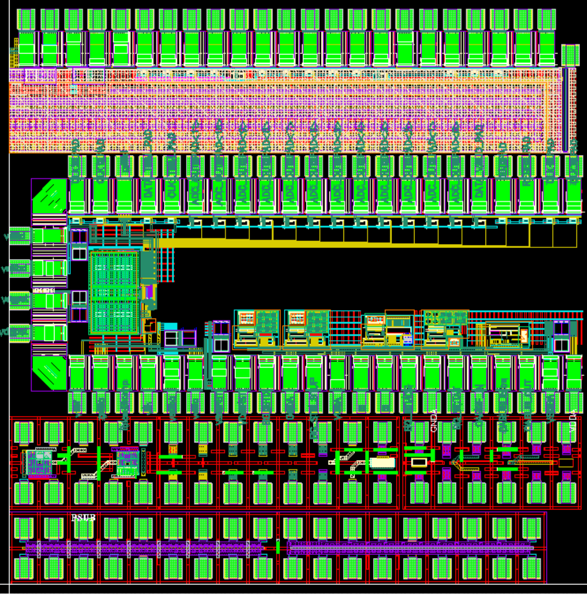
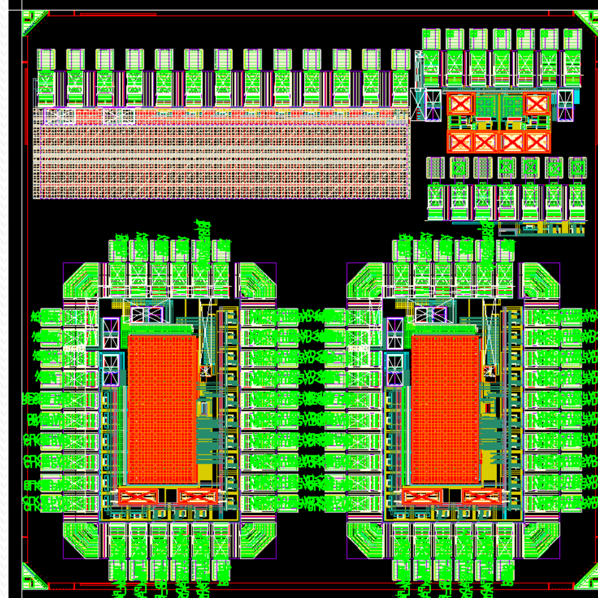
CPPM activities



PROTO65_V1
Submitted June 2014



PROTO65_V2
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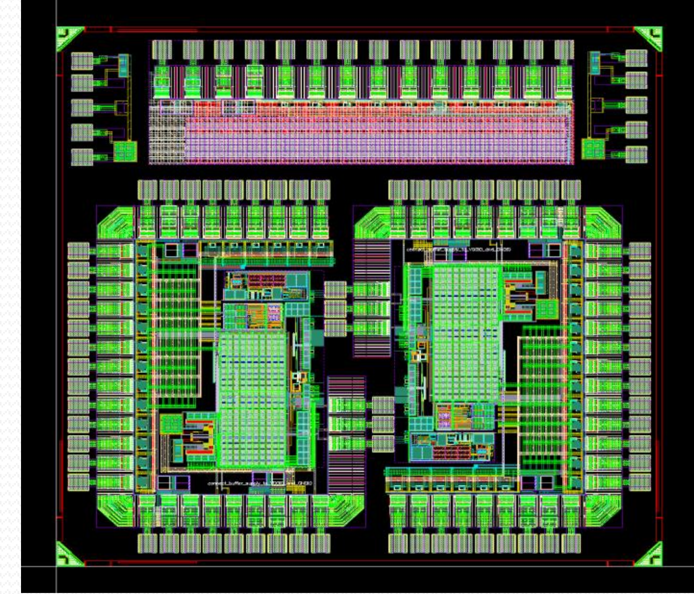
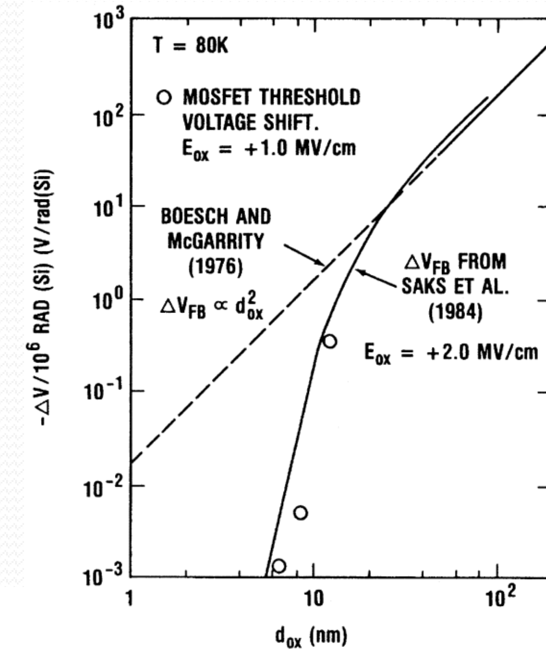


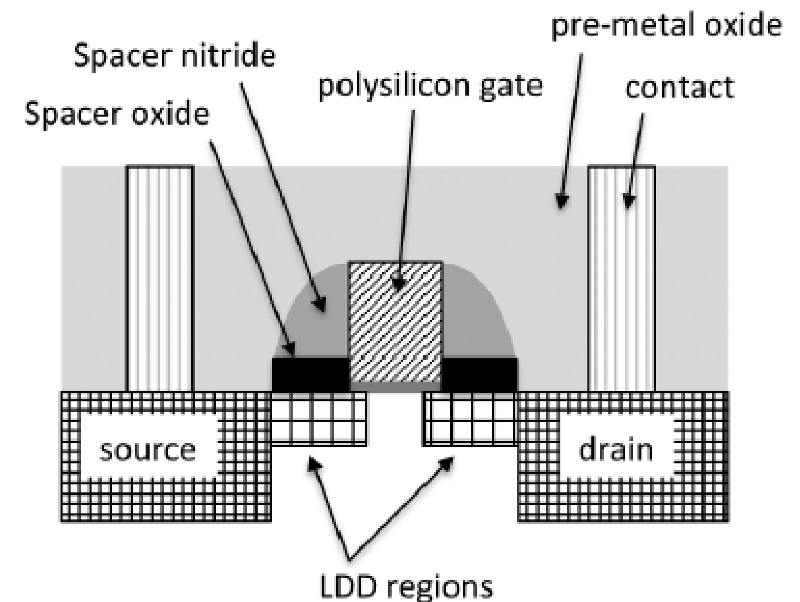
PROTO65_V3
Submitted Feb 2017

- Transistor devices, SEU memories, Bandgap, ADC, Monitoring block, Temperature and radiation sensors ..
- Design, test and qualification of the 65nm devices and IP blocks for a dose level of 500 Mrad
- The work is done in coordination with CERN RD53 program

Radiation effects in CMOS

- Baseline technology : 65nm CMOS for the RD53 project
- The TID-induced charge in the thin oxide decreases with the thickness of the oxide
- In highly scaled processes
  - The thin gate oxide is very tolerant to the TID
  - Thick oxide used for isolation : Thick Shallow Trench Isolation Oxide (STI)
  - Thick oxide exists everywhere around the device
- Radiation Induced Leakage Current (RILC)
- Radiation Induced Narrow Channel Effect (RINCE)
- Radiation Induced Short Channel Effect (RISCE)





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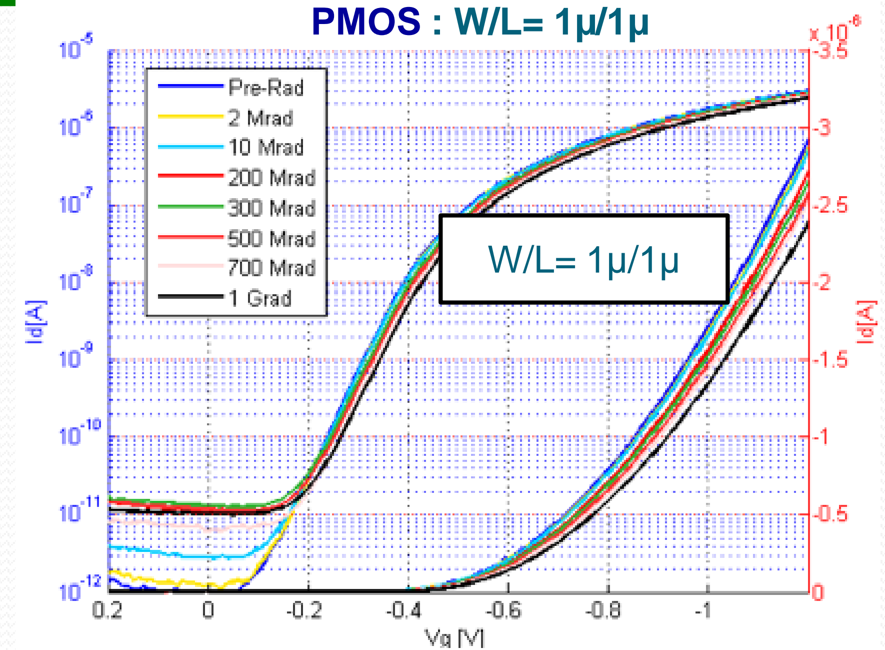
TID effects on the 65nm devices

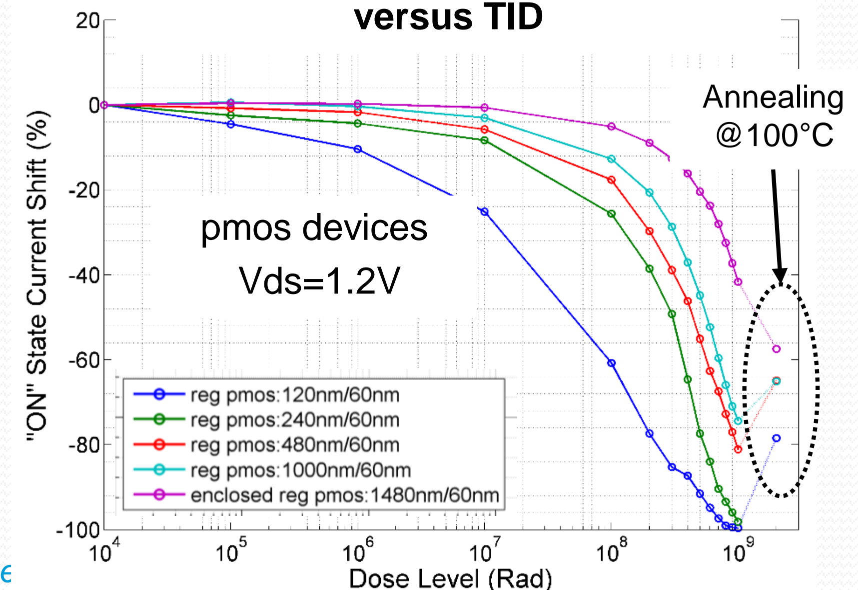
- The increase of the leakage current is very limited
  - Factor 100 for the worst case
- The enclosed layout is not needed
- PMOS devices more sensitive than NMOS
- TID effect on large and long devices (NMOS and PMOS) is limited
- Analog Design : Avoid the use of narrow or short transistors
  - Analog designs following these rules showed a good radiation tolerance up to 1 Grad
  - Irradiation damage depends on the bias. This affect the matching and can be an issue
- Digital design :
  - Requires High integration density
  - Digital cells are designed with minimum size devices and so are subject to RINCE and RISCE effects

PMOS : W/L= 1µ/1µ



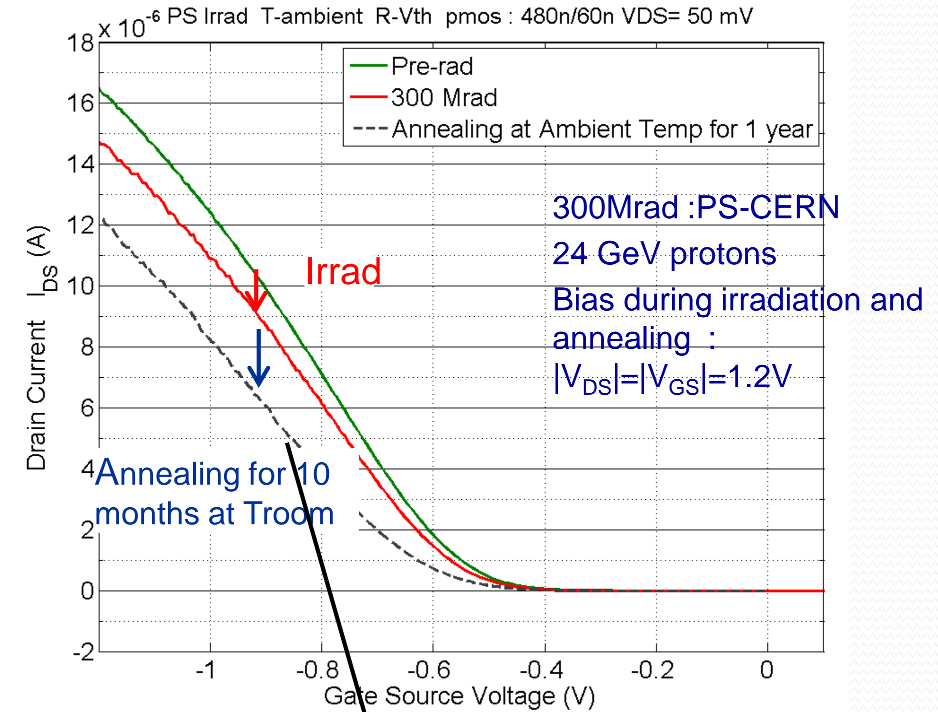
Supplier A - Temp=20°C

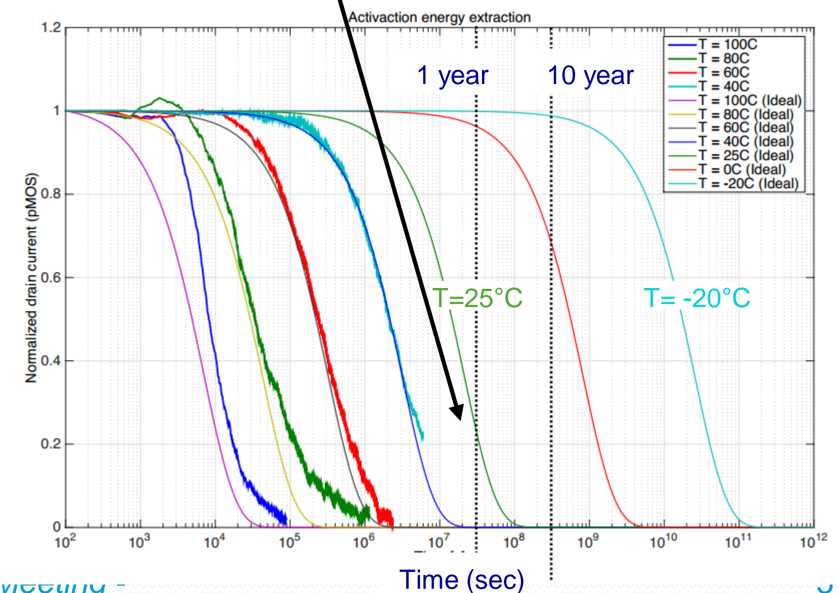
Pmos devices :ON state current versus TID



Temperature and annealing Effect

- Less damage for the PMOS and NMOS when Irradiation is done at low temperature
- High temperature annealing (100 °C for 7 days) degrades strongly the DC parameters and show a high Vth shift
- A long term annealing at room temperature was done for ~1 year on irradiation devices at the PS-CERN -> more degradation
- Qualification and annealing for different temperature were done at CERN
- The Vth shift of the PMOS device is a thermally activated process
- Extrapolation for lower temperatures
- For the RD53 Front end chip, this temperature effect can be avoided by keeping the system :
  - In cold environment : -20°C for 5 years
  - Unbiased at room temp for few months





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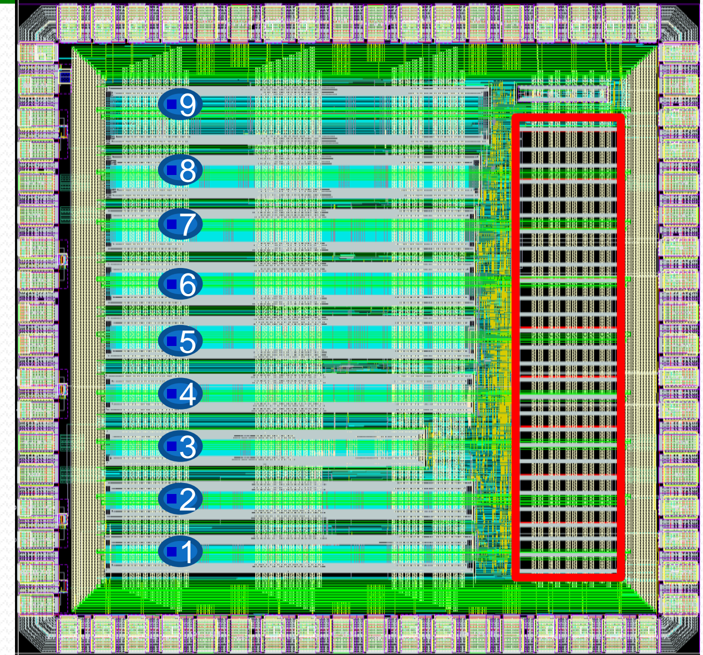
Irradiation effects Modeling

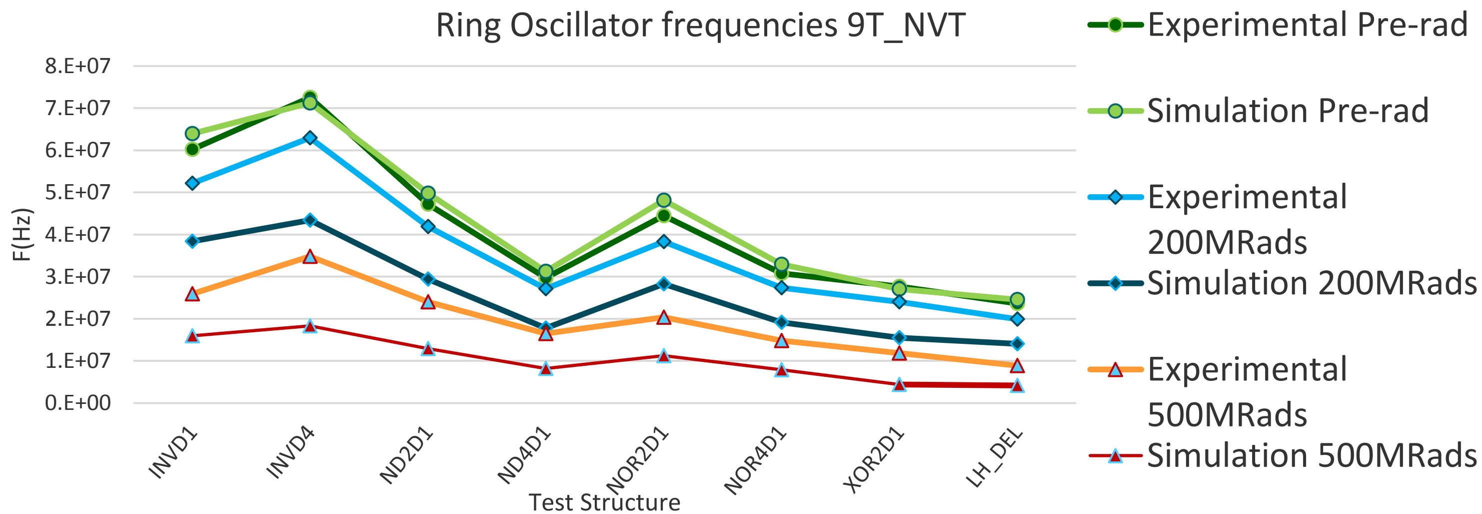
- The current drive loss depends strongly on the device width W and on length L
- Spectre Model Corners were developed based on the irradiation tests : 200 Mrad and 500 Mrad and the dependence on W and L is included:
  - Transconductance degradation
  - Threshold voltage increase
  - Leakage current is implemented for NMOS
  - Short channel effect and Subthreshold swing change are included for small size NMOS (60nm<L<240nm)
- HVT and LVT models were extrapolated from RVT devices measurements
- Assumptions :
  - Room temperature irradiation
  - Worst case biasing (VDS=VGS=1.2V)
  - Annealing effect not included
- Largely used for RD53A chip simulation, optimization and dose effect estimation
- Analog designs : Directly done under Spectre virtuoso
- Digital Designs : 200 Mrad, 500 Mrad Liberty files for synthesis based on the current model
  - digital models extracted (Liberate) : Timing (delay …) and power (Leakage and internal power)
  - Timing verification and digital simulation

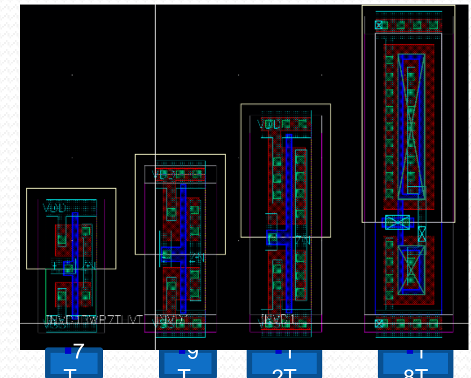
DRAD Chip : Test chip for digital design

- DRAD chip is designed at CERN :
- To study the effect of radiation on digital standard cells for the 65nm TSMC technology
- To test the efficiency and the validity of the digital simulations with the irradiation corner model
- Simulation results goes in the same direction than irradiation tests but the model overestimates the TID damage level
  - Models were done for worst case of biasing
- NOR gates should be avoided since show a strong degradation



ANNEALING NOT INCLUDED IN THE MODELS





CELL HEIGHT
7 Track: 1.4 uM
9 Track: 1.8 uM
12 Track: 2.4 uM
18 Track: 3.6 uM

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SEU tolerant Cells for configuration

- Cross section for the standard latch : σ = 2.8e-14 cm2/bit
- High energy hadrons producing SEE in pixel barrel layer0 (3.7 cm) estimated : 0.5 E9 /cm2/s
- 160 000 pixels per FE chip and 8 configuration bit per pixel
  - ~ 18 upsets/s per FE chip
- Number of global configuration bits : 1 kbit

	Mean time between errors (1 FE chip)	
	Pixel Config	Global Config
Memory size	1.28 Mbit/chip	1 Kbit/chip
Single latch	55 ms	71 s

- The cross-section of pixel and global configurations should be decreased by factor ~1000

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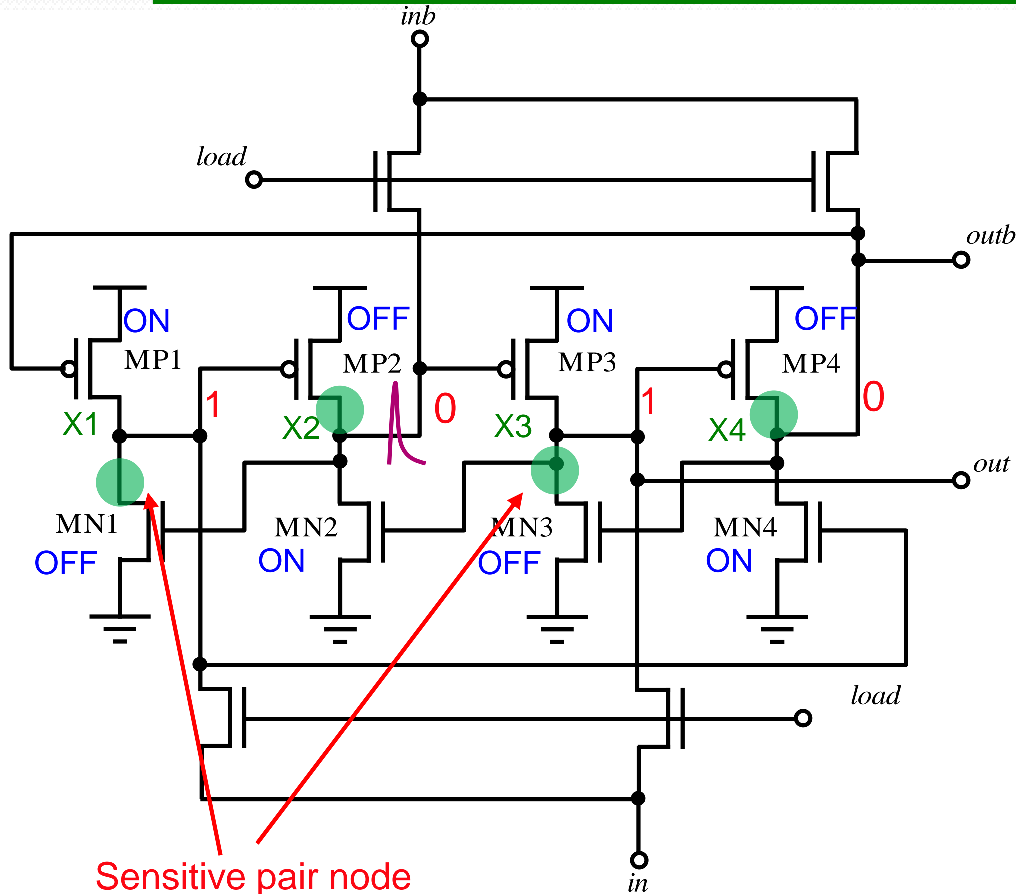
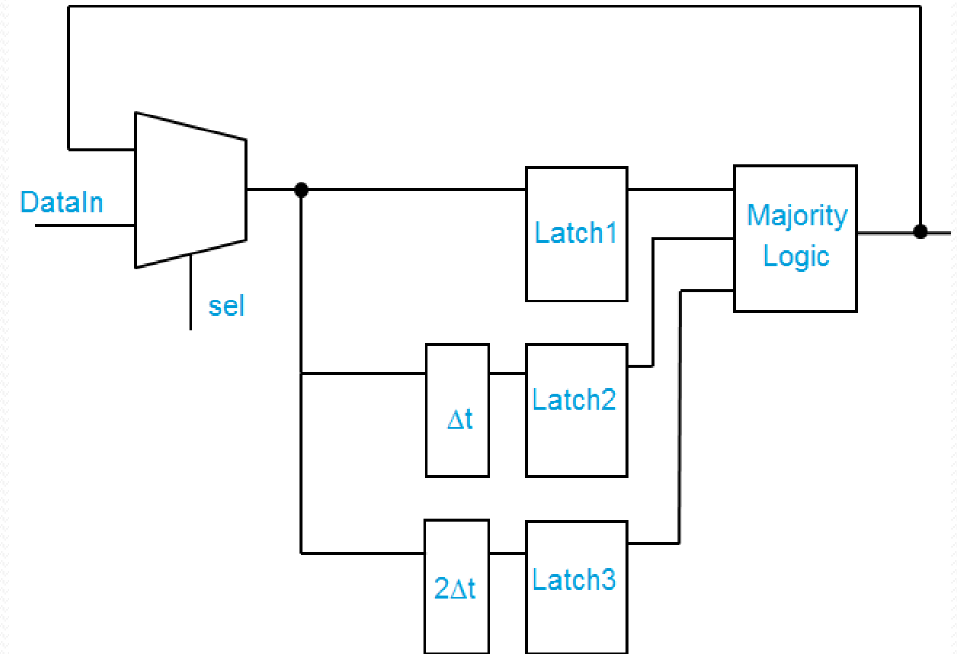
Pixel configuration memories





- Structures tested intensively for the SEU tolerance at PS-CERN with 24 GeV proton beam :
- DICE Latch : Dual Interlocked Cell
- TRL : Triple redundancy Latch with error correction

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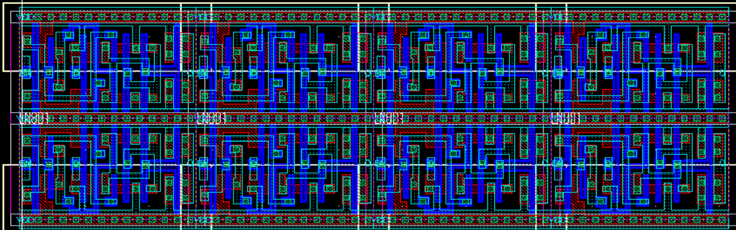
DICE Latches SEU test results

	Number of errors/ spill			Cross section (cm^2)
	0 to 1	1 to 0	All	
Single latch	2.58	2.29	2.43	2.8 E-14 cm^2/bit
DICE latch interleaved layout	0.26	0.29	0.27	3.1 E-15 cm^2/bit

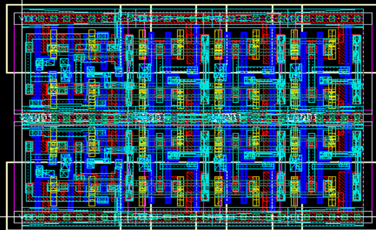
- Enough Statistics for SEU
  - 640 cells for each tested cell and > 20 000 spills
- Cross section single latch ~ 2.8E-14 cm^2
- With interleaved layout, improvement of the SEU tolerance : 9 x more tolerant than the Single latch -> cross section = 3.1E-15 cm^2

Area comparison

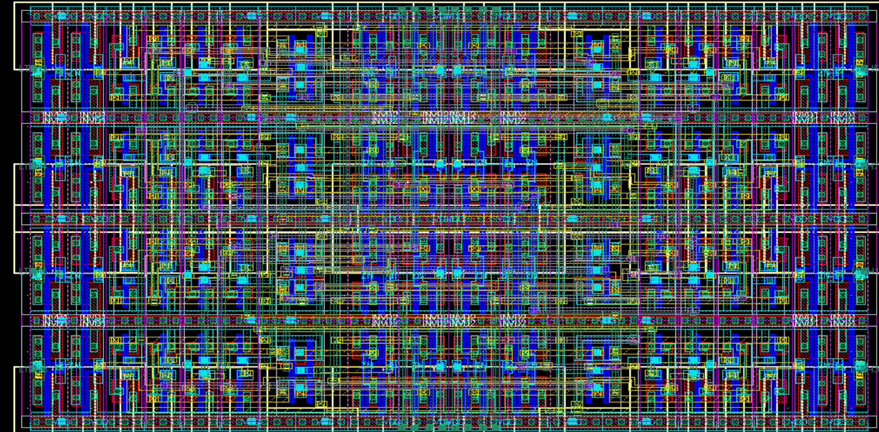
8 bit LNQD1 –VCAD



8 bit LNQD1shrink –VCAD



8 bit DICE LATCH



Interleaved DICE version

Critical distance between 2 sensitive nodes = 7µm

	Area (8bits)	Area/pixel	Routing
Single latch	11.2µm × 3.6µm	1.6 % (40 µm²)	M1/M3
Shrinked latch	5.4µm × 3.6µm	0.8 % (20 µm²)	M1/M3
DICE latch	13.2µm × 7.2 µm	3.8 % (96 µm²)	M1/M4

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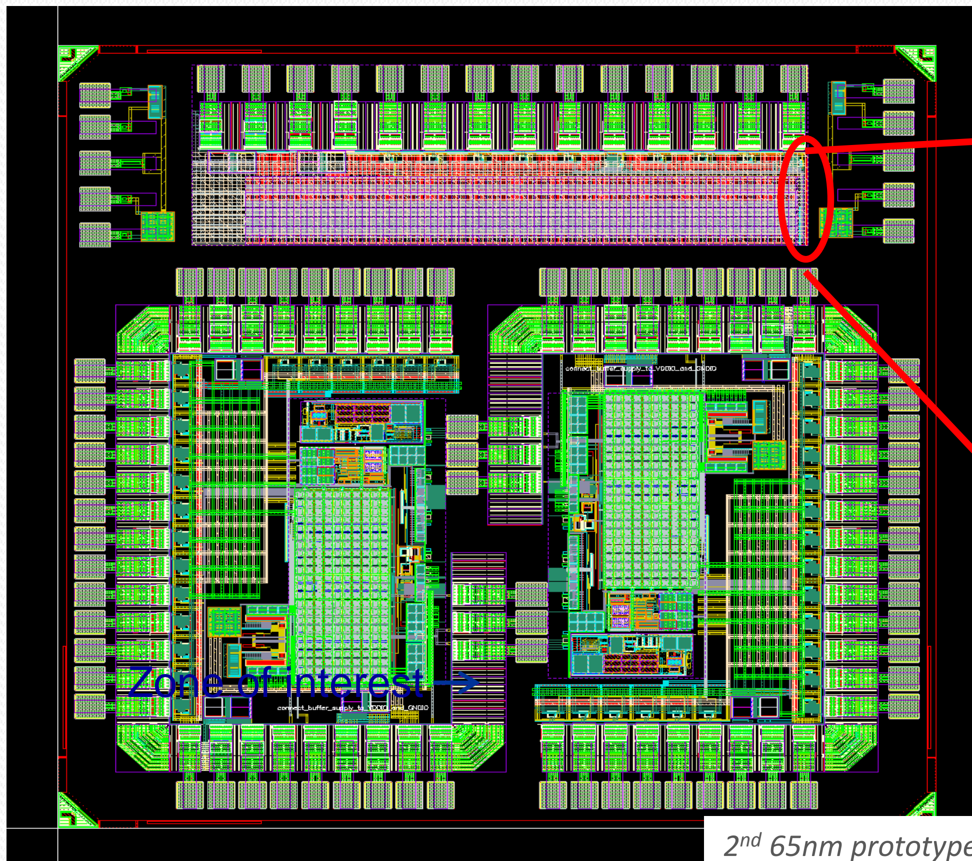
TRL Latches results

	Number of errors/ spill			Cross section (cm²)
	0 to 1	1 to 0	All	
Single latch	2.58	2.29	2.43	2.8E-14 cm²
Ref TRL Latch	20E-3	1.8E-3	11E-3	1.26E-16 cm²
TRL with load triplication	4E-3	1.9E-4	2.1E-3	2.3 E-17 cm²
TRL with load triplication and interleaved layout	1.2E-3	4.6E-5	6.2E-4	6.8 E-18 cm²

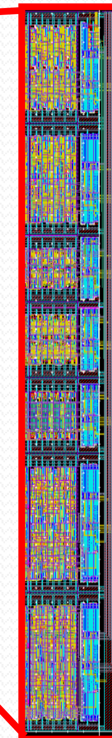
- TRL latch without optimisation is ~200x immune to SEU than single latch
- Interleaved layout in plus of the load signal triplicate improves the SEU tolerance by a factor 18
- Optimized TRL is 3600 x tolerant than the single latch
- RD53A : TRL used in the digital chip Bottom – Synthesis tool used

Test Chip

- Prototype chip just submitted the February 20 this year
- Study the effect of the DNW on the SEU tolerance
  - The digital part of the RD53A chip is placed in a DNW to reduce the crosstalk
- Test and qualify the Monitoring block as it is implemented in the RD53A chip

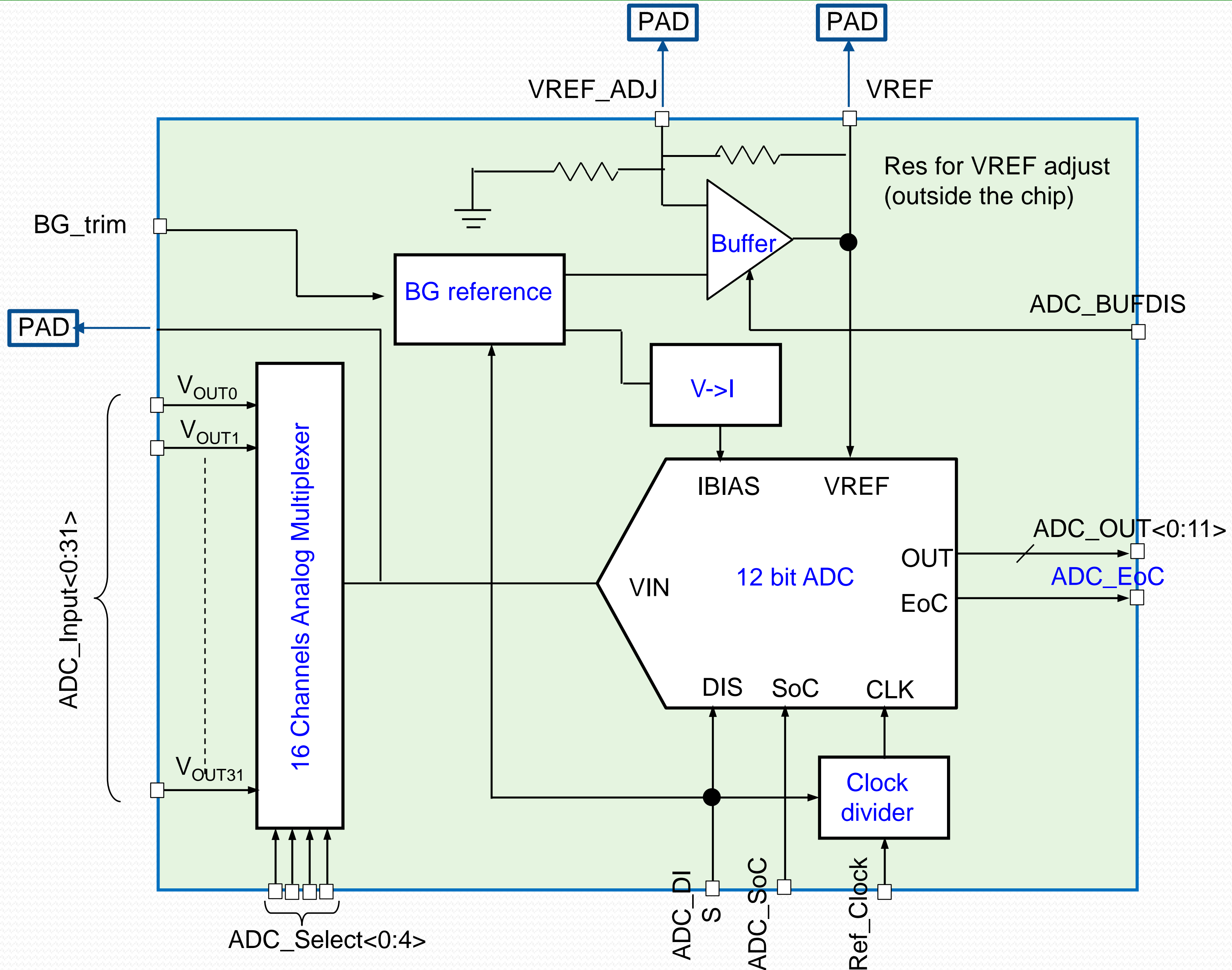


2nd 65nm prototype



- Clmn1
- Clmn2
- Clmn3
- Clmn4
- Clmn5
- Clmn6
- Clmn7

Monitoring block



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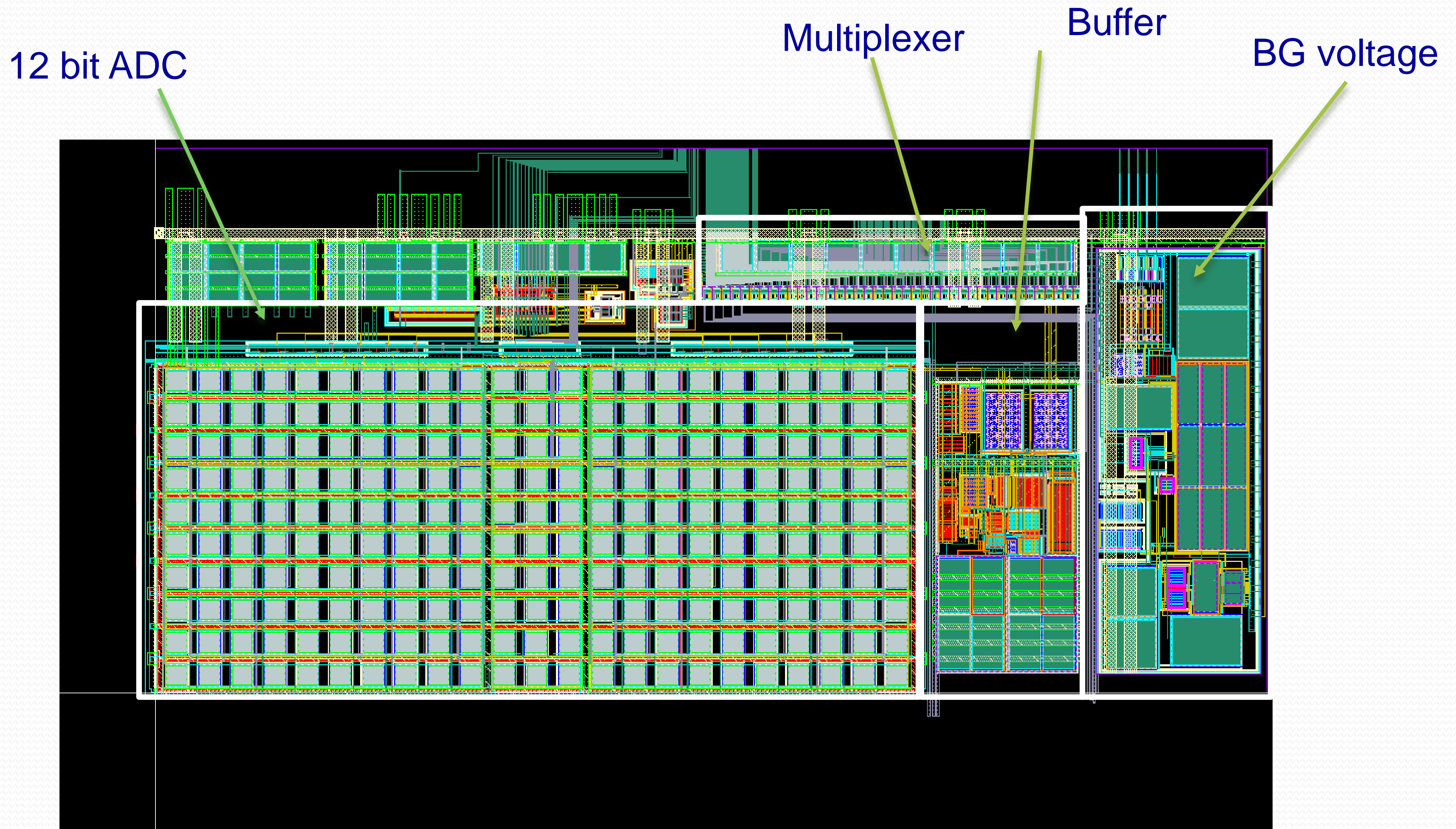
Monitoring block layout



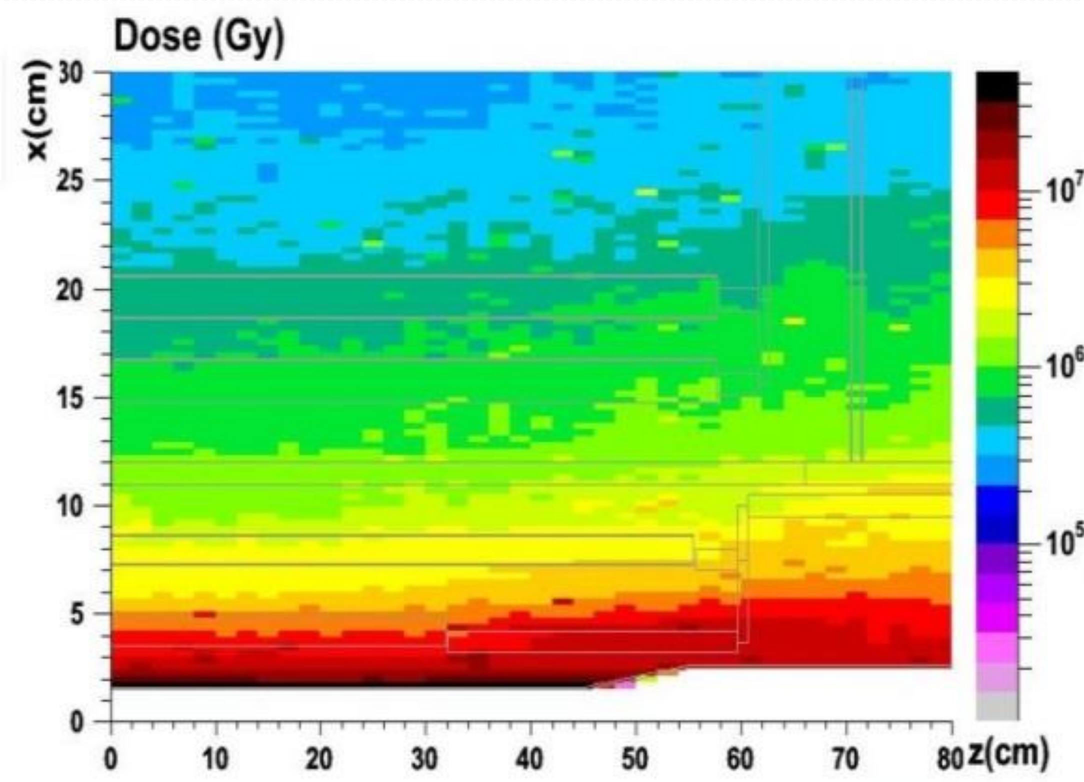
Conclusion

- The 65 nm process qualified for 500 Mrad
  - Limited leakage current
  - A strong drive loss for small size pmos devices and the damage increases with the temperature
  - RD53 Front end chip (pixel environment)
    - Avoid the use of narrow or short transistors for analog design
    - Corner Models developed for 200 Mrad and 500 Mrad and used to characterize digital cells
    - DRAD chip designed by CERN group indicates which digital libraries can be used
    - The temperature effect can be avoided and delayed by keeping cold : -20°C for 5 years and keeping unbiased at room temp for few months
- SEU tolerant latches for pixel and global configurations were designed and tested
- A new prototype designed to test the effect of the DNW on the SEU tolerance and will be used to test and qualify the Monitoring block, temperature and irradiation sensors as it is implemented in the RD53A chip

Thank you for your attention
Thank you for your attention

Backup

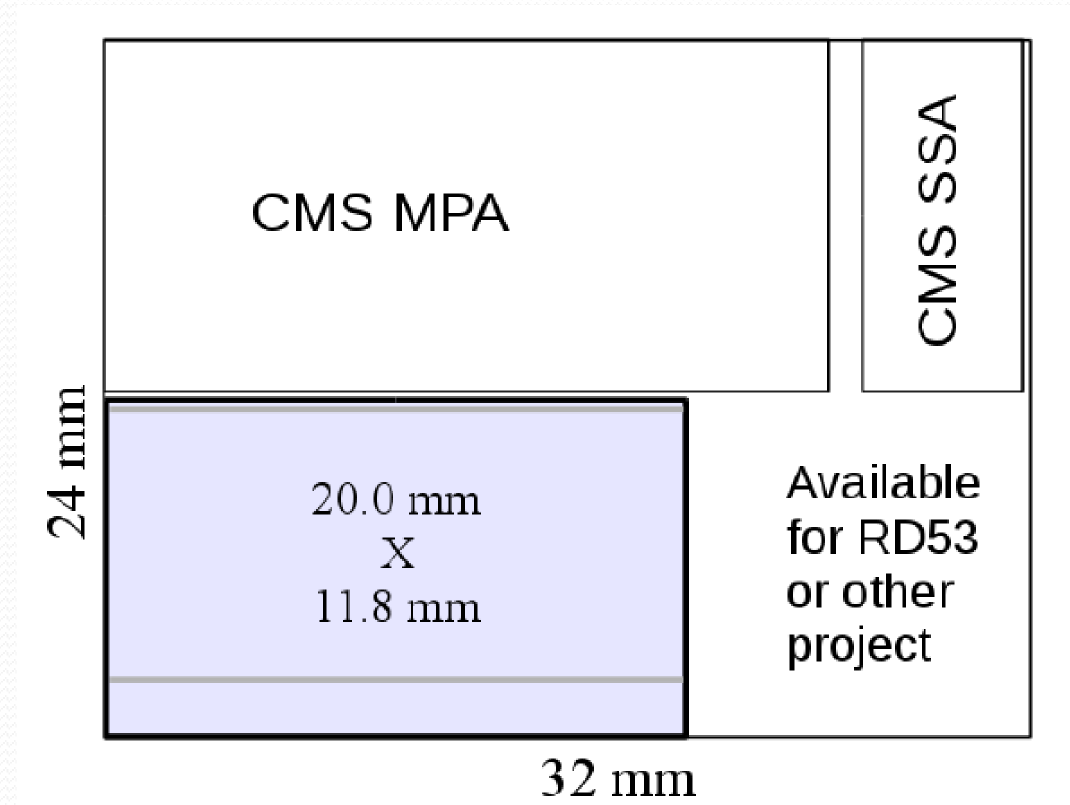
Introduction



- The HL-LHC upgrades are planned for 2022
- Consequences for the pixel detectors :
  - Extreme particle flux
    - From 200 MHz/cm2 in the current system to 2 GHz/cm2
    - 50 kHz per pixel for a 50 x 50 µm2 pixel
  - Extreme radiation levels. Up to 1 Grad & 2.10^{16} neq/cm2 for the innermost layers (~5 cm)
- RD53 collaboration :
  - "Development of pixel readout IC for extreme rate and radiation" : ATLAS-CMS-CLIC working group on small feature size electronics
  - 6 working groups, among which one working on radiation effects
  - Test and evaluate the 65 nm technology for a dose level of 1 Grad
- The work presented here essentially done in this framework

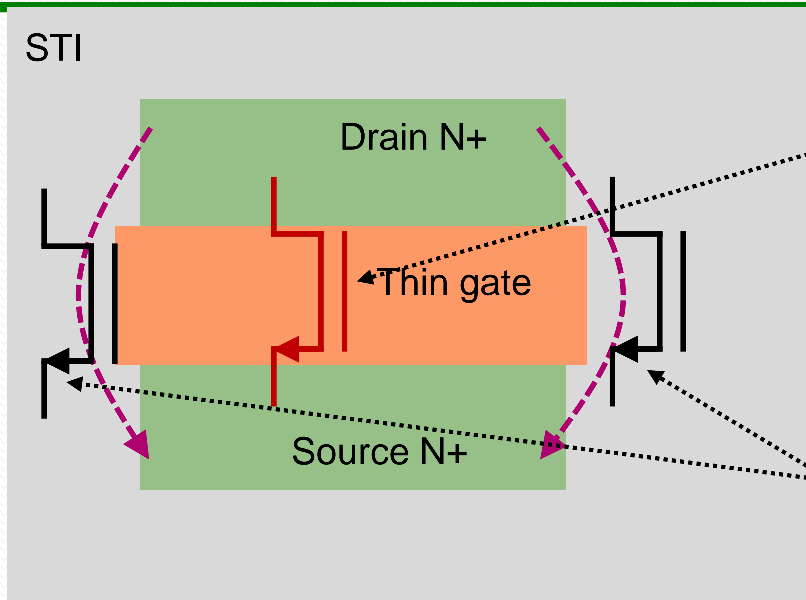
RD53A prototype

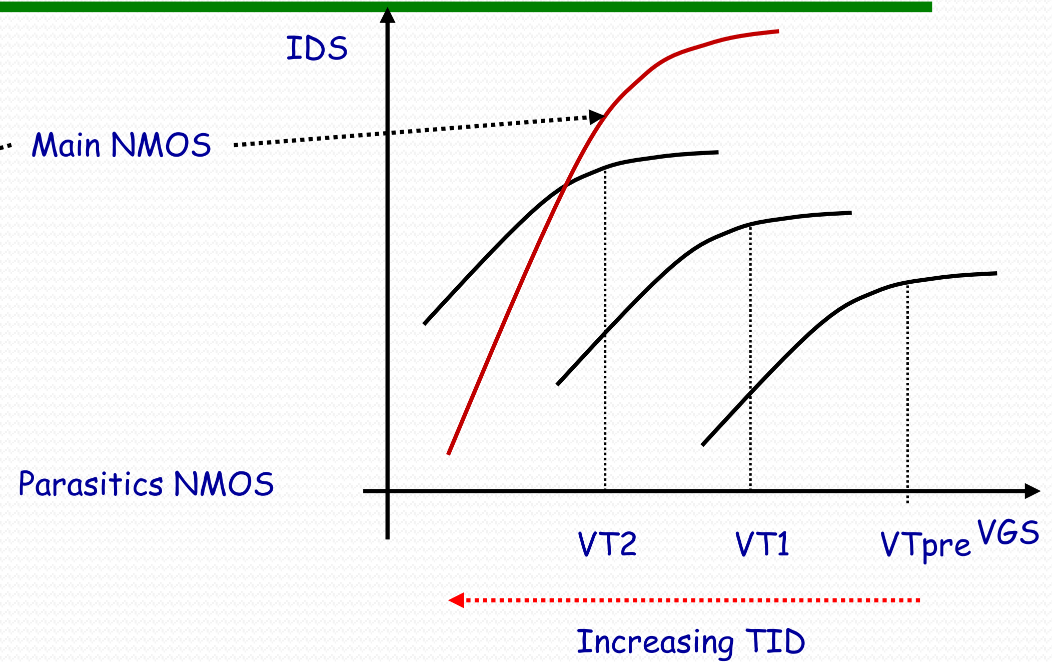
- 20 mm × 11.8 mm
- 400 × 192 pixels de 50 µm × 50 µm
- Demonstrator chip and not the production chip
- Achieve all the specifications ?
- 65 nm process in term of irradiation
- Test of Different design variants
- Bump bonded to the sensor
- Test of the serial powering



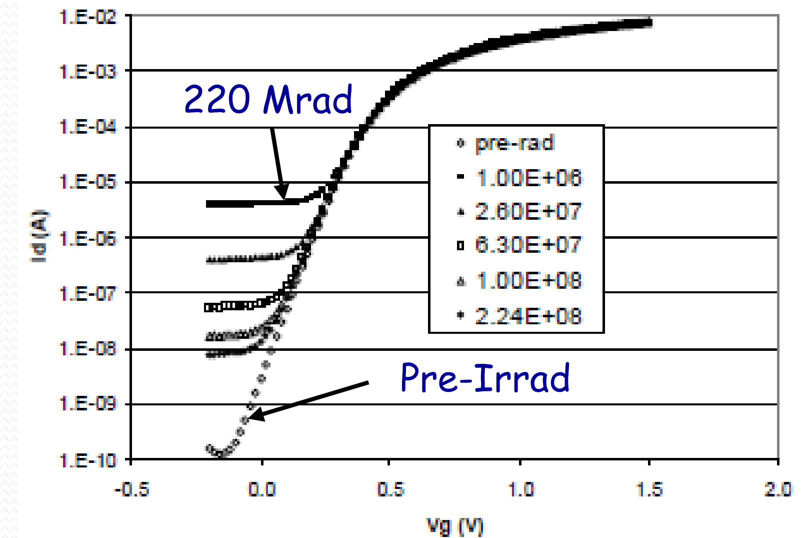
- To be submitted May 2017

Radiation Induced Leakage Current



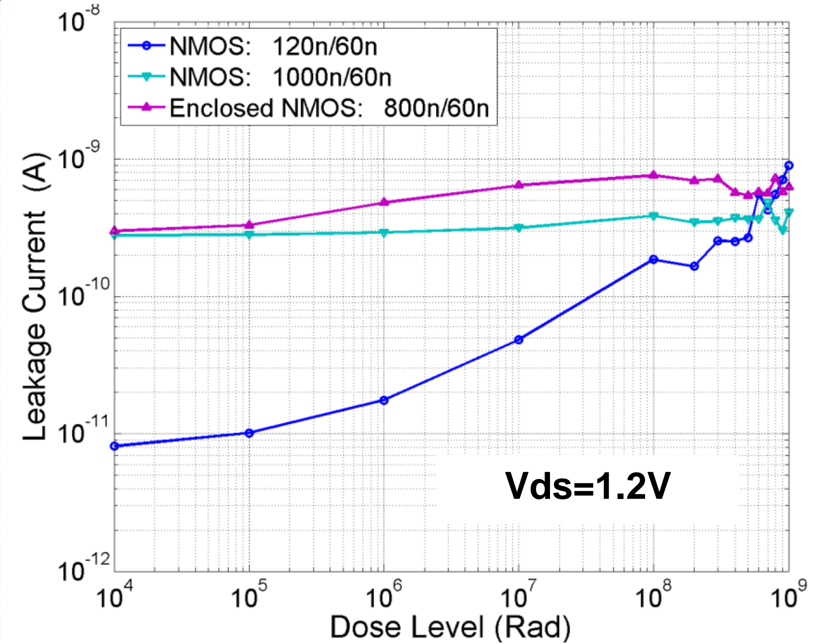


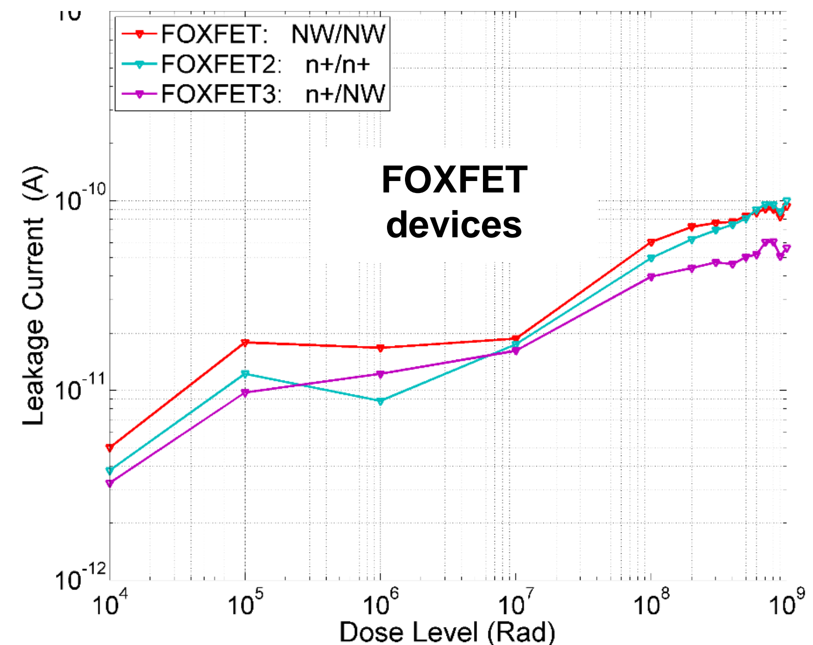
- ❑ Concerns only NMOS transistors
- ❑ Trapping in the isolation oxide (Shallow Trench Isolation – STI)
- ❑ Increase in off-state leakage and Inter devices leakage
  - Radiation-induced positive charges opens inversion channel / parasitic transistor
  - Higher effect for narrow transistors
  - Parasitic transistor is a strong competitor to main channel
- ❑ Effects on IC design : increase power, overheating and failure



Leakage Measurements for TSMC 65 nm

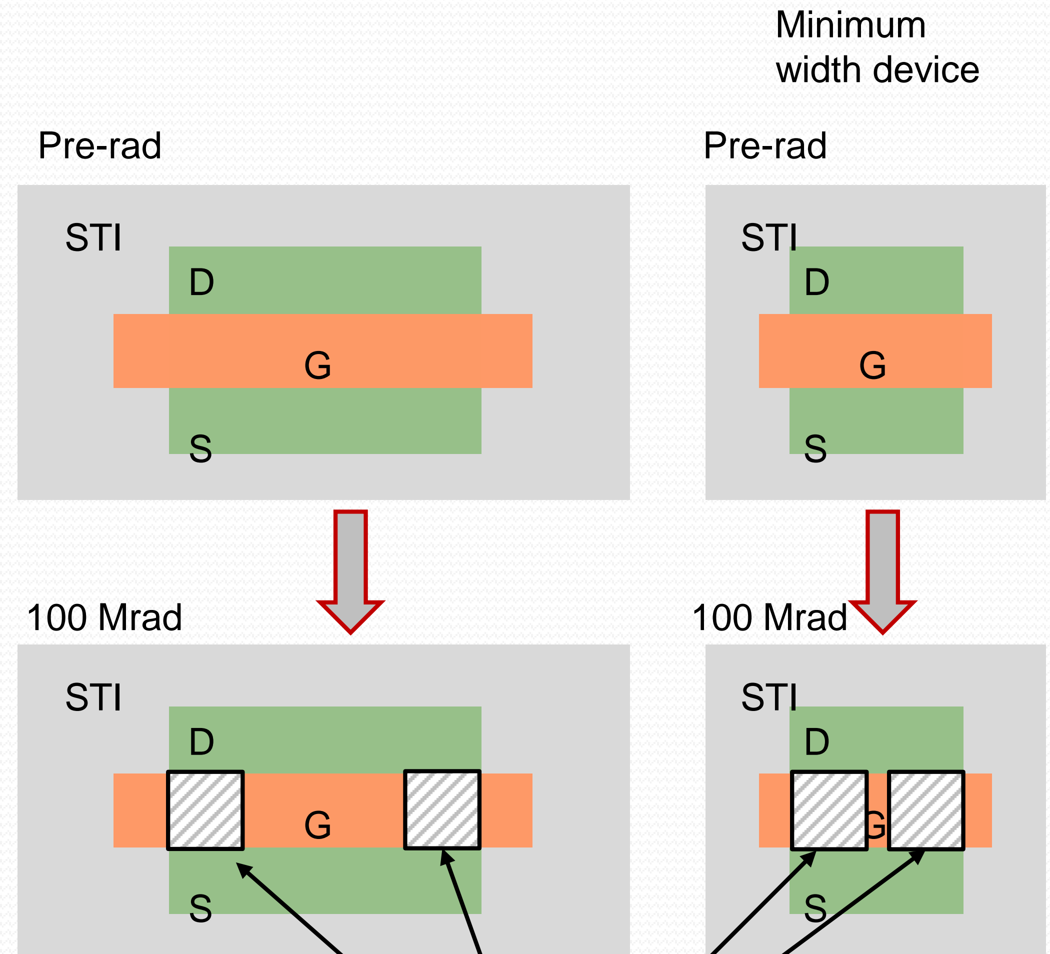
- Device with 120nm/60nm (the narrower one) shows the highest increase in leakage :
  - Parasitic device more influent
  - ~ 2 orders of magnitude for the level of 1000 Mrad
  - Same order of magnitude for the leakage variation with the process
  - The leakage value is below 1 nA for 1 Grad
  - Peak of 200 nA at 1-6 Mrad for IBM 130nm
- Different FOXFET structures have been tested (NW/NW, n+/n+ and n+/NW)
  - The current increase is low
  - The increase of the Inter-device leakage is also limited
- For this 65nm process, the increase of the leakage current is very limited
- The enclosed layout is not needed





Radiation Induced Narrow Channel Effect

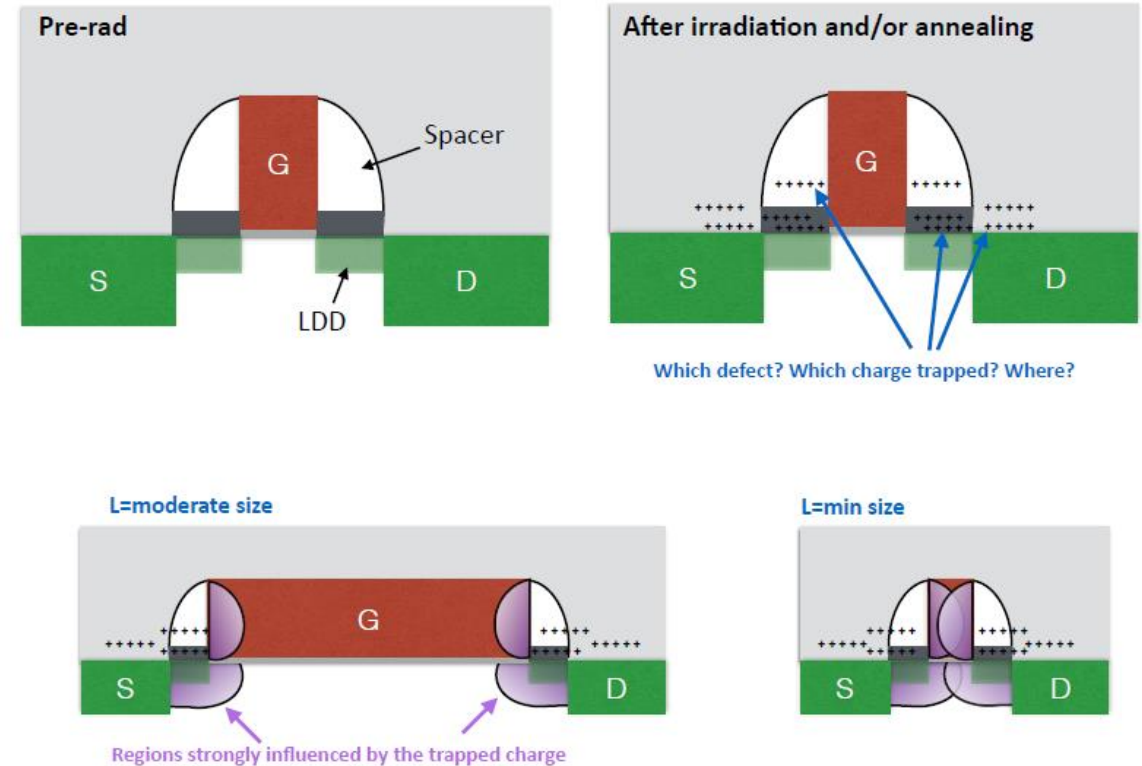
- RINCE is caused by the charge trapped in the STI
- This charge affects the electric field in the channel and modify the transistor characteristics
- More relevant for narrow transistors



Radiation Induced Narrow Channel Effect:
F. Faccio and G.Cervelli, IEEE Trans. Nucl. Science, Vol.52, N.6 (2005) pp.2413-2420

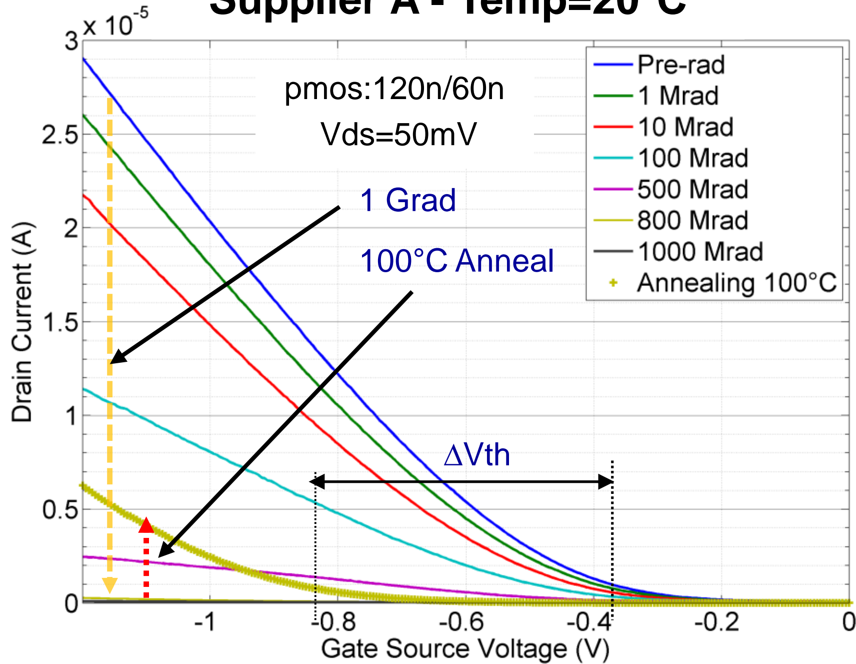
Radiation Induced Short Channel Effect

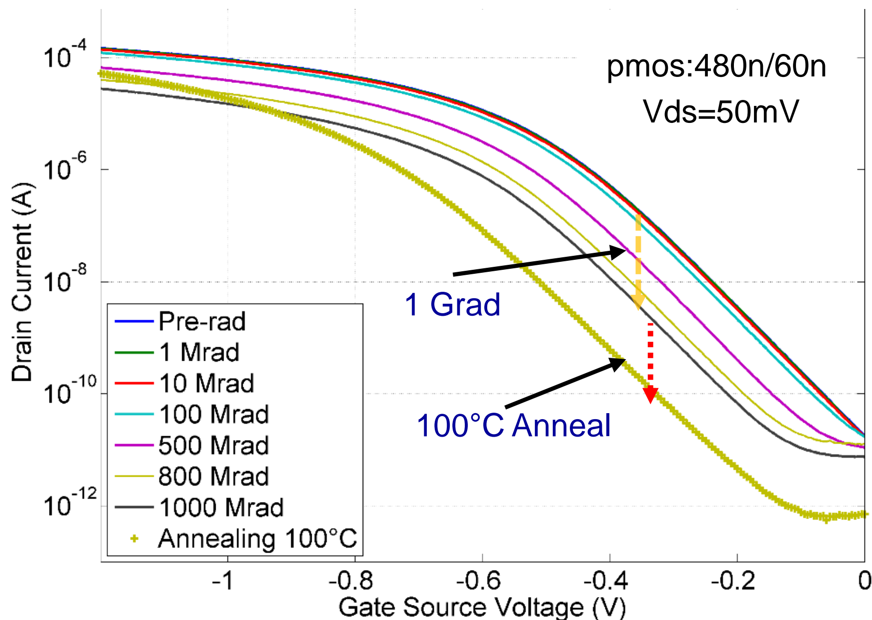
Radiation Induced Short Channel Effect:
F. Faccio et al., IEEE Trans. Nucl. Science, Vol.62 , N.6 (2015)



- RISCE is not related to the STI
- May be attributed to the charge induced in the spacer's oxide because of irradiation effects.
- This charge affects the electric field and then the surface potential in the LDD (Lightly Doped Drain)
- More damage for short channel device

Ids(Vgs) variation for small pmos device





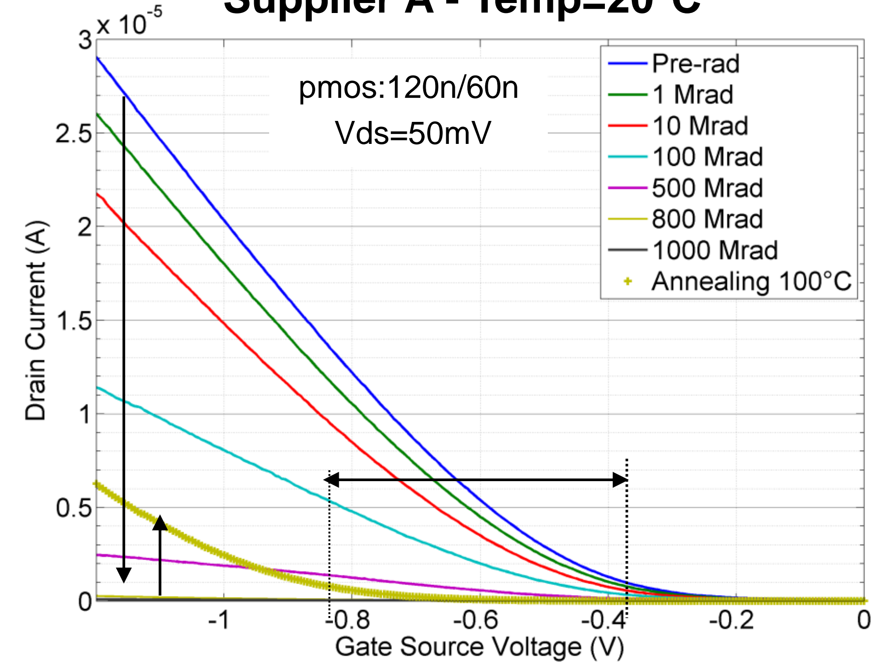
- Id(Vg) for the narrower device (120nm/60nm)
- At the high level of dose, The device becomes completely “OFF”
- The transconductance factor G_M (mobility) is more affected than the threshold voltage
- With high temperature annealing G_M recovers well but Vth increases
- The Vth shift is ΔVth ~ 0.45 V for the small size devices

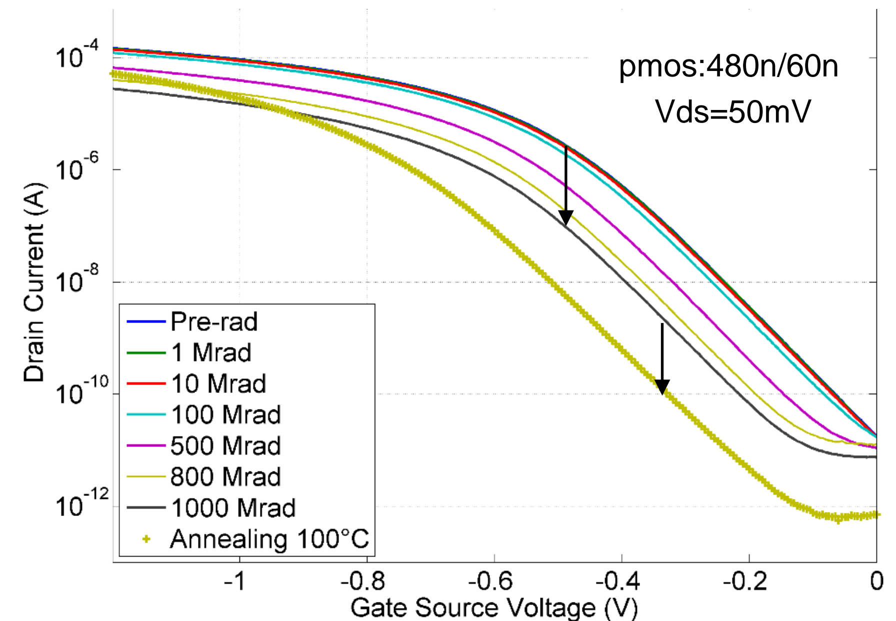
PMOS devices irradiation

- Id(Vg) for the minimum size device (120nm/60nm)
- At the high level of dose, The device becomes completely "OFF"
- The GM factor (mobility) is more affected than the threshold voltage
- No increase for the leakage current
- With high temperature annealing GM recovers well but Vth increases
- The Vth shift is ~ 0.45 V for the narrower device

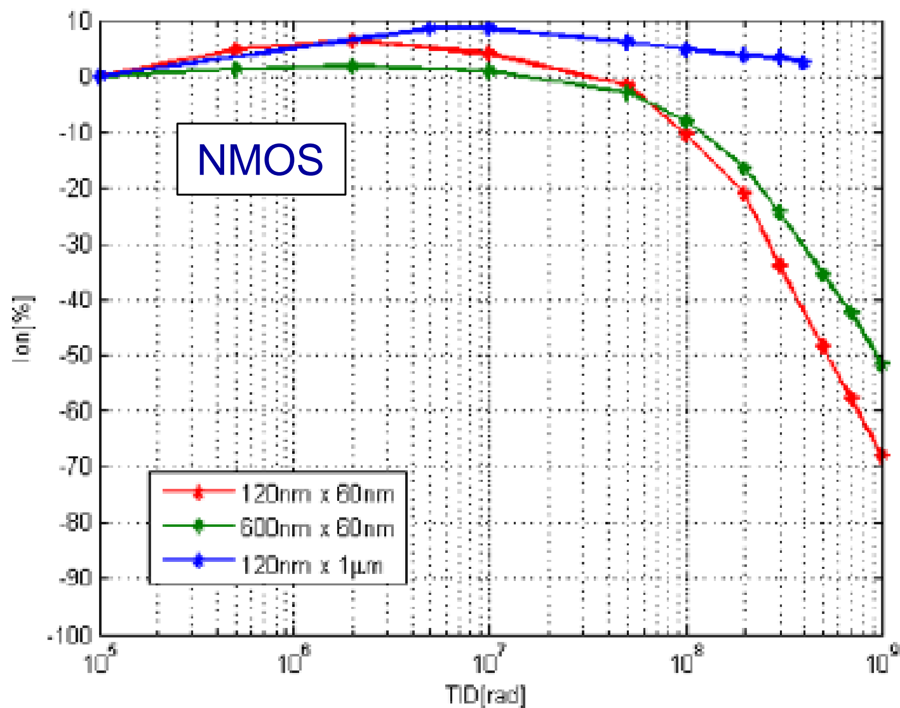
/60

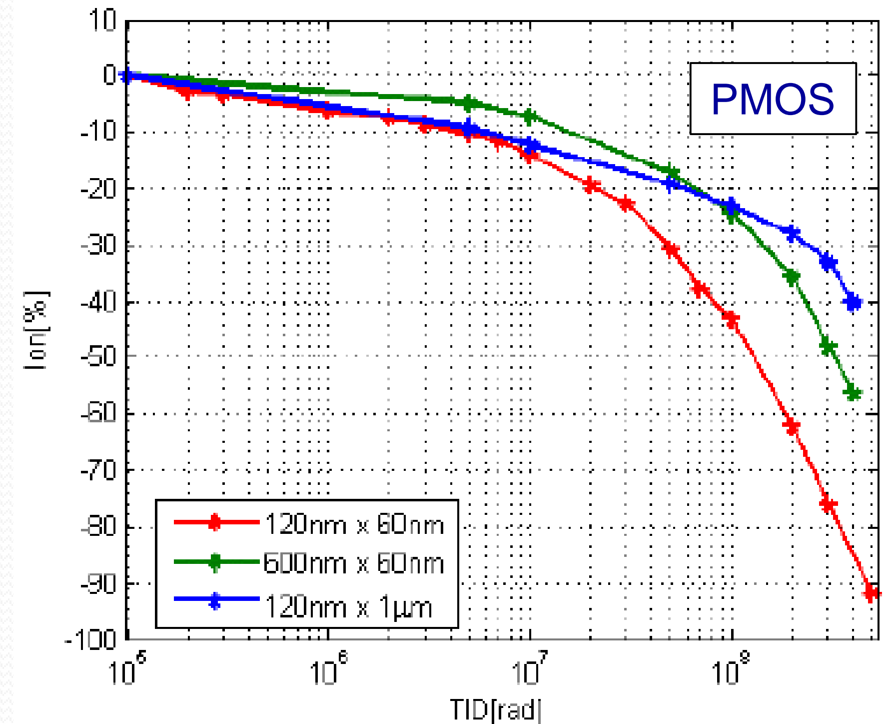
Supplier A - Temp=20°C





Short and Narrow transistors

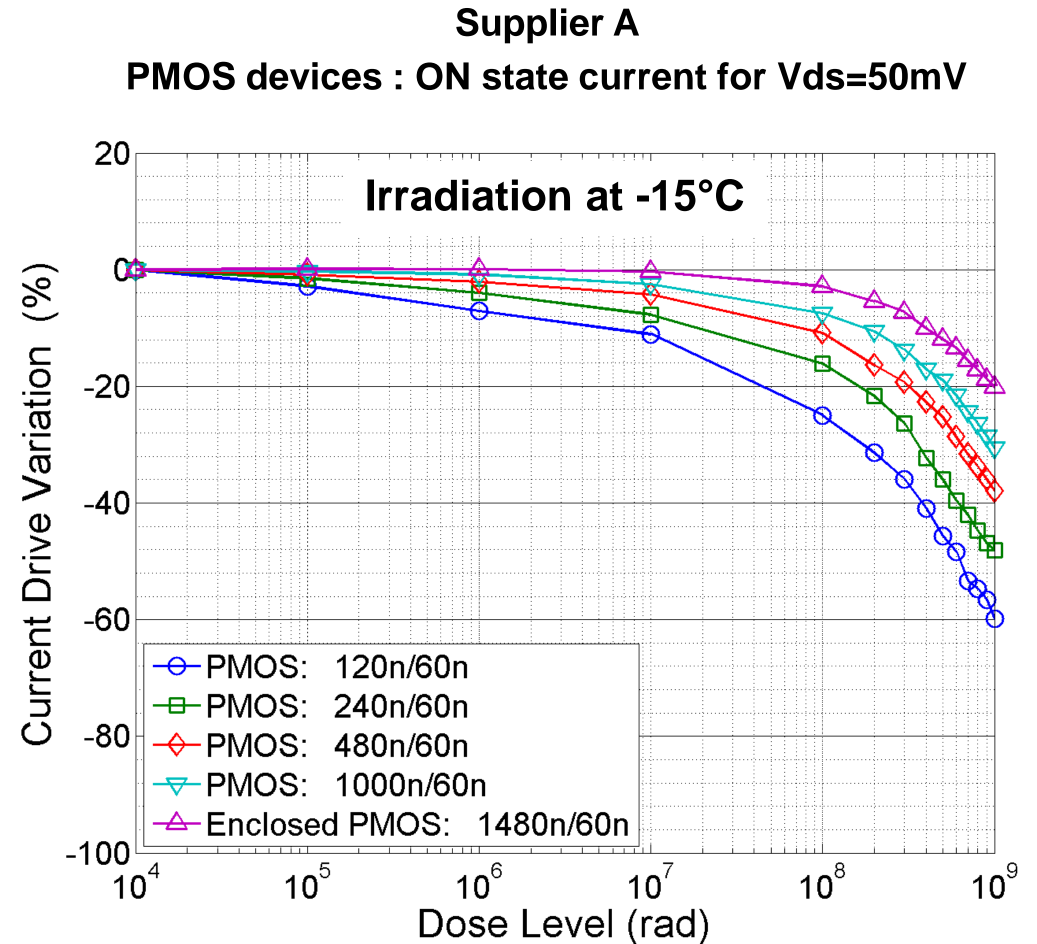




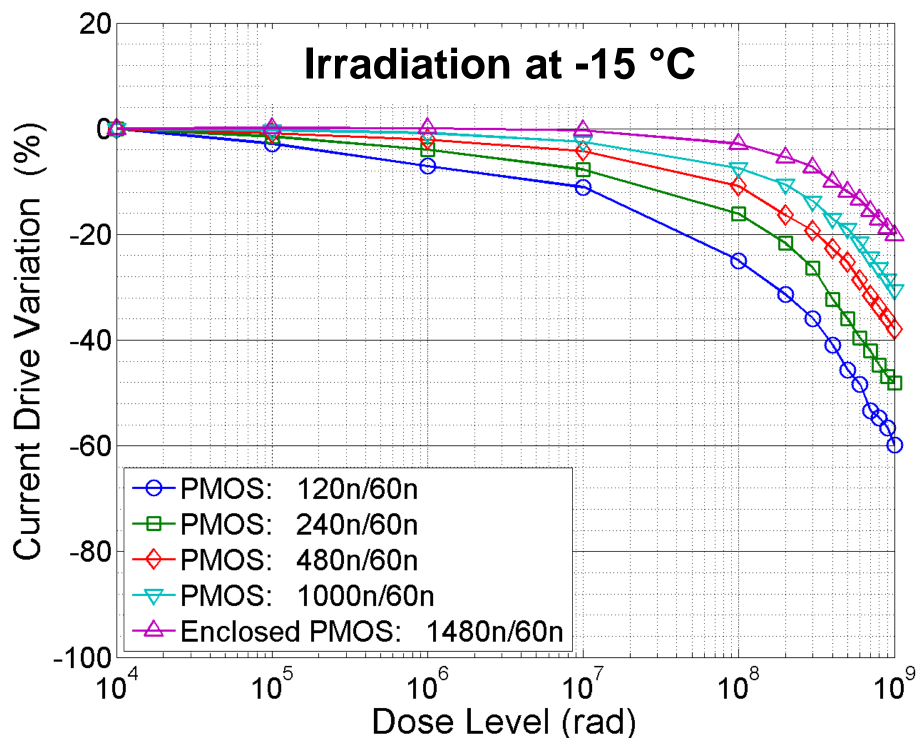
- Short and Narrow transistors are affected by RISCE and RINCE. Strong degradation of "Digital" devices
  - RISCE is dominant for the NMOS devices
- Strongly depends on temperature during irradiation and bias conditions of the devices
  - Less damage for the NMOS and PMOS device when Irradiation is done at low temperature (-20 °C)
  - More damage for the worst case bias : VGS=VDS=1.2 V (diode connected)
- An issue for standard digital cells DRAD: Various digital libraries , various test cells…
- Need to define libraries to be used for RDR53A

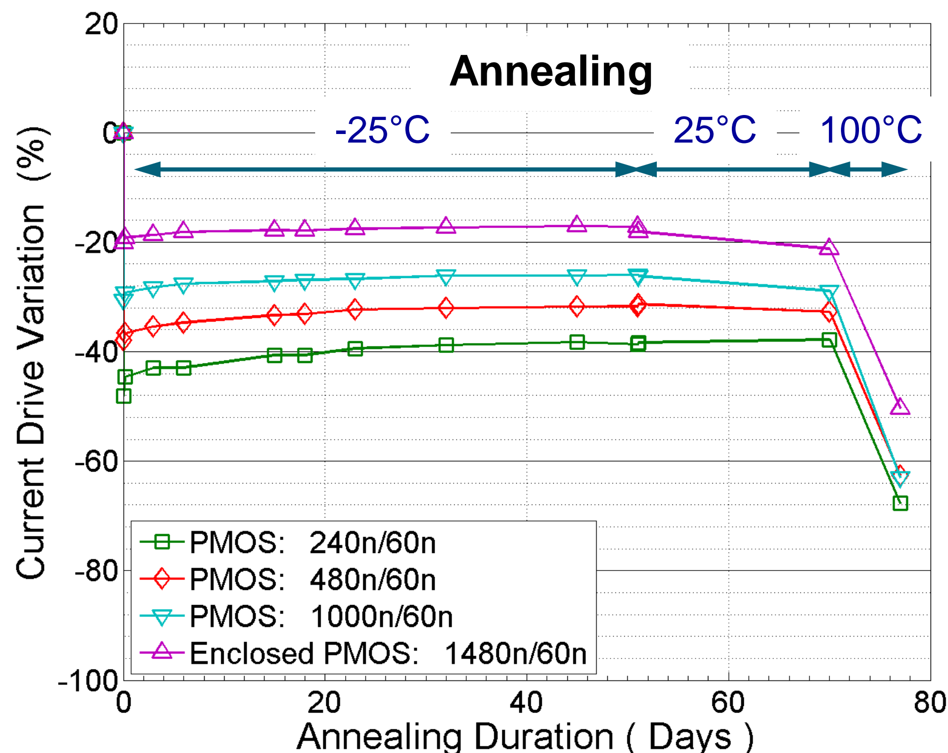
Annealing Effect

- Less damage for the PMOS device when Irradiation is done at low temperature
  - Parameters shift does not compromise the digital design functionality
- This TID testing and qualification is performed at a High Dose Rate (HDR) of 9 Mrad/hour
- Several orders of magnitude higher than the Low Dose Rate (LDR) expected for the actual HL-LHC environment
- In general, the qualification for LDR consists in performing HDR testing followed by the high temperature annealing under bias



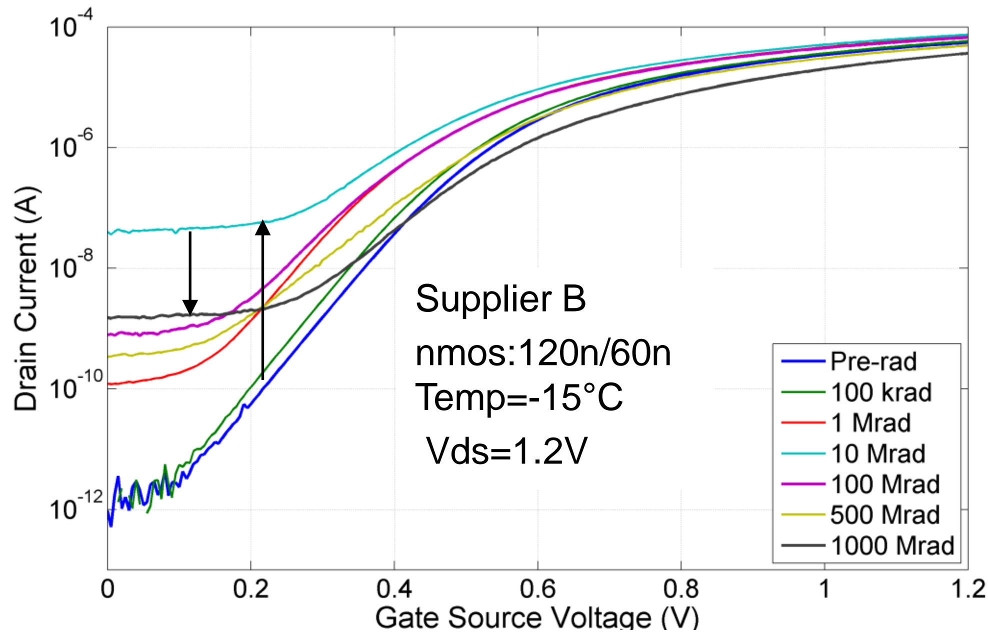
Annealing Effect

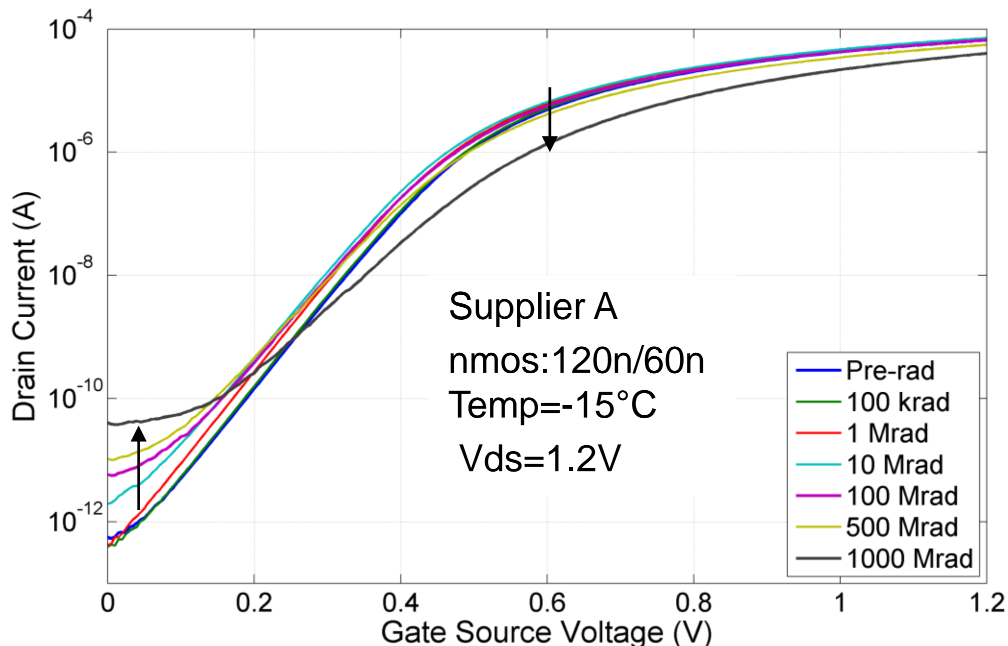




- This TID testing and qualification is performed at a High Dose Rate (HDR) of 9 Mrad/hour
- In general, the qualification for LDR consists in performing HDR testing followed by the high temperature annealing under bias
- High temperature annealing (100 °C for 7 days) degrades strongly the DC parameters
- This degradation comes from the increase of the threshold voltage
  - ΔVth = 0.28 V with respect the pre-irradiation value for the 240nm/60nm device

Comparison of processes A / B at -15°C

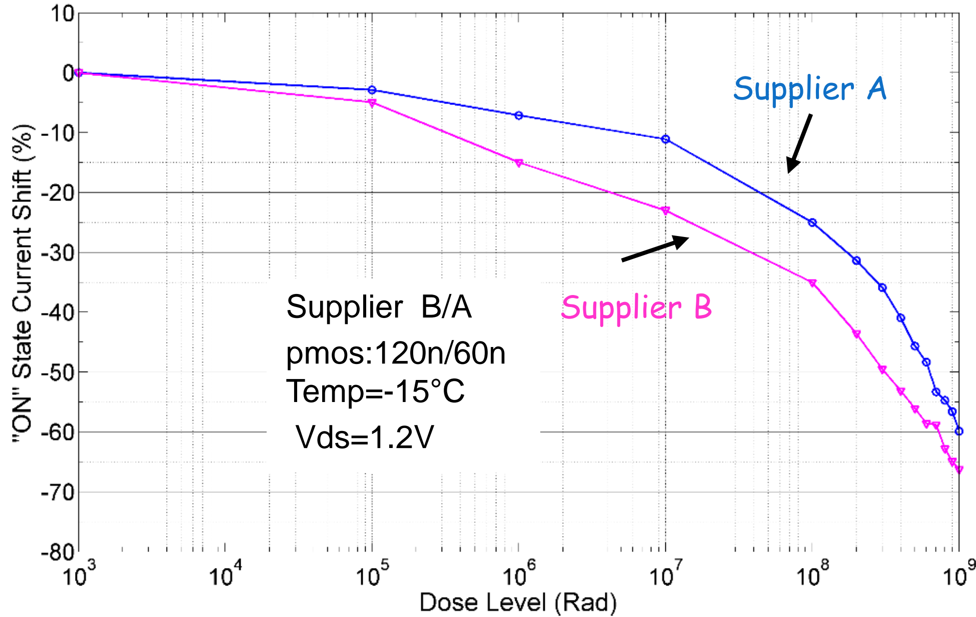


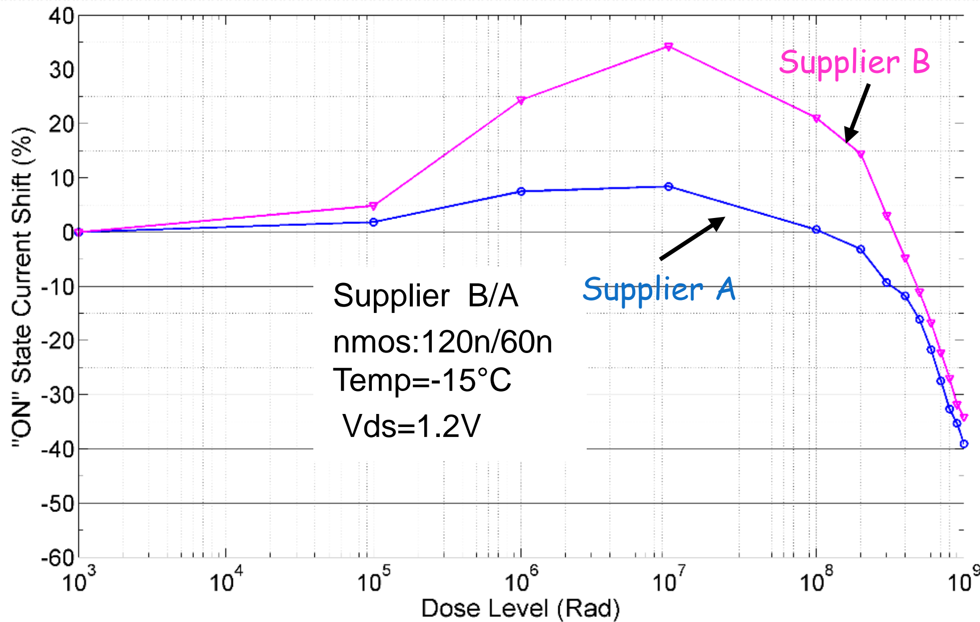


- The test chip (process B) provided by MOSIS through Berkeley
- Compared devices : L=60 nm and W : 120nm, 240nm, 480nm and 1um
- The process B devices show a higher increase for the leakage current
  - The maximum value (~10 Mrad) is 200 nA
  - 10^5 times the pre-rad value
  - Parasitic transistor leaks much more than for the process A

Comparison of processes A / B at -15°C

ON state current for Vds=1.2V





- A similar behavior is observed for another 65nm process (supplier B)
- Pmos : Loss of transconductance in both cases
- Nmos : Larger rebound region between 100krad-100Mrad for the supplier B
- The degradation depends more on the device width for B than for A in this region
  - Confirms that the parasitic STI device is more influent for the process B
- The degradation at the high level of dose is not related only to the 65nm process from the supplier A (CERN contract)

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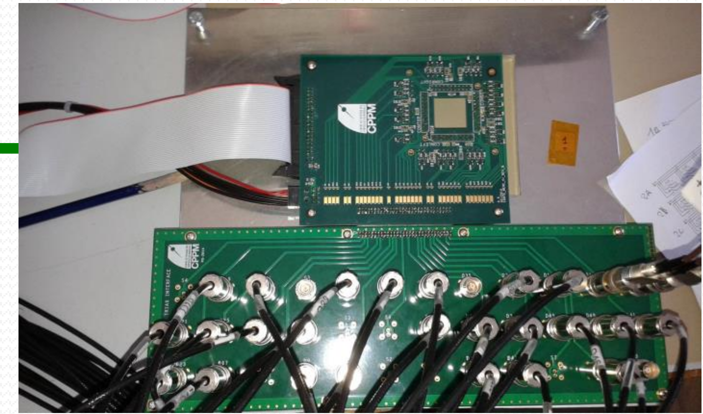
Test set up



- 65 nm Devices Irradiation Test Set-up
- Different set up were designed (Denis Fougeron presentation)
  - Stability of the set up
  - External ESD to overcome the Pb of the static charge

-> First “reliable” characterization for 1 Grad was done by CPPM

- Do we need to progress in this work ?
- Which facility to use ?
- Denis in contact with JL Autran (IM2NP)

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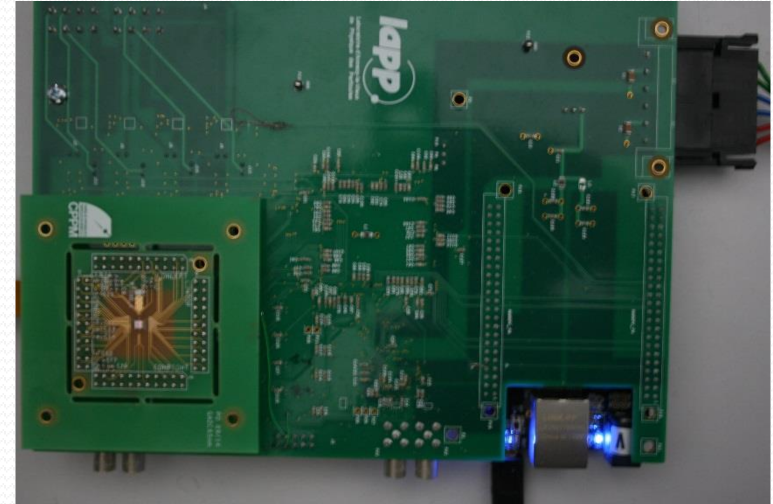
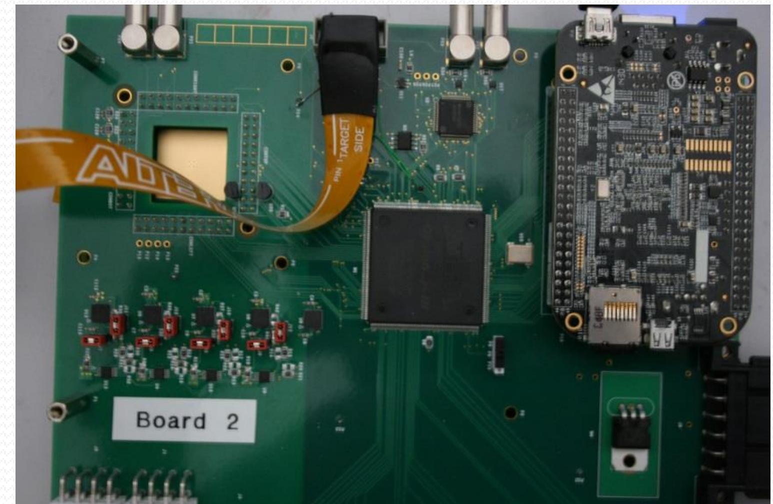
Test Set-up

- The test board based on a nano PC boarb
  - Easy Ethernet interface
  - High level programming framework
  - Up to 50 m link
  - An FPGA deals with the low level interface (clock, IO. . .)
  - 16 bit DAC, 14 bit ADC implemented
- The GADC reference voltage and the GADC input voltage are generated with 16 bit DAC controlled by the nano PC board
- Collaboration with LAPP (Renaud Gaglione)
- Preparation of the RD53A test firmware based on this test set-up





Xray Test Set up

- Xray CERN Facility: 10 keV
- A total dose of 1000 Mrad is reached in ~1 week following a Dose rate of 9 Mrad/hour (2.5krad/s)
- Measurement of devices characteristics for (100 krad, 1Mrad, 10 Mrad, 100 Mrad, 200 Mrad …. 1000 Mrad) and takes 3-4 hours
- Evaluate the irradiation tolerance of digital devices (120nm/60nm to 480nm/60nm)
- Study the dependence of the irradiation hardbess on the device width
- Set device size suitable for a radiation tolerant digital library
- During irradiation and during annealing phase, pmos and nmos devices are set in :
  - Nmos : VG=VD=1.2V and VS=VB=0V
  - Pmos : VG=VD=0 V and VS=VB=1.2V

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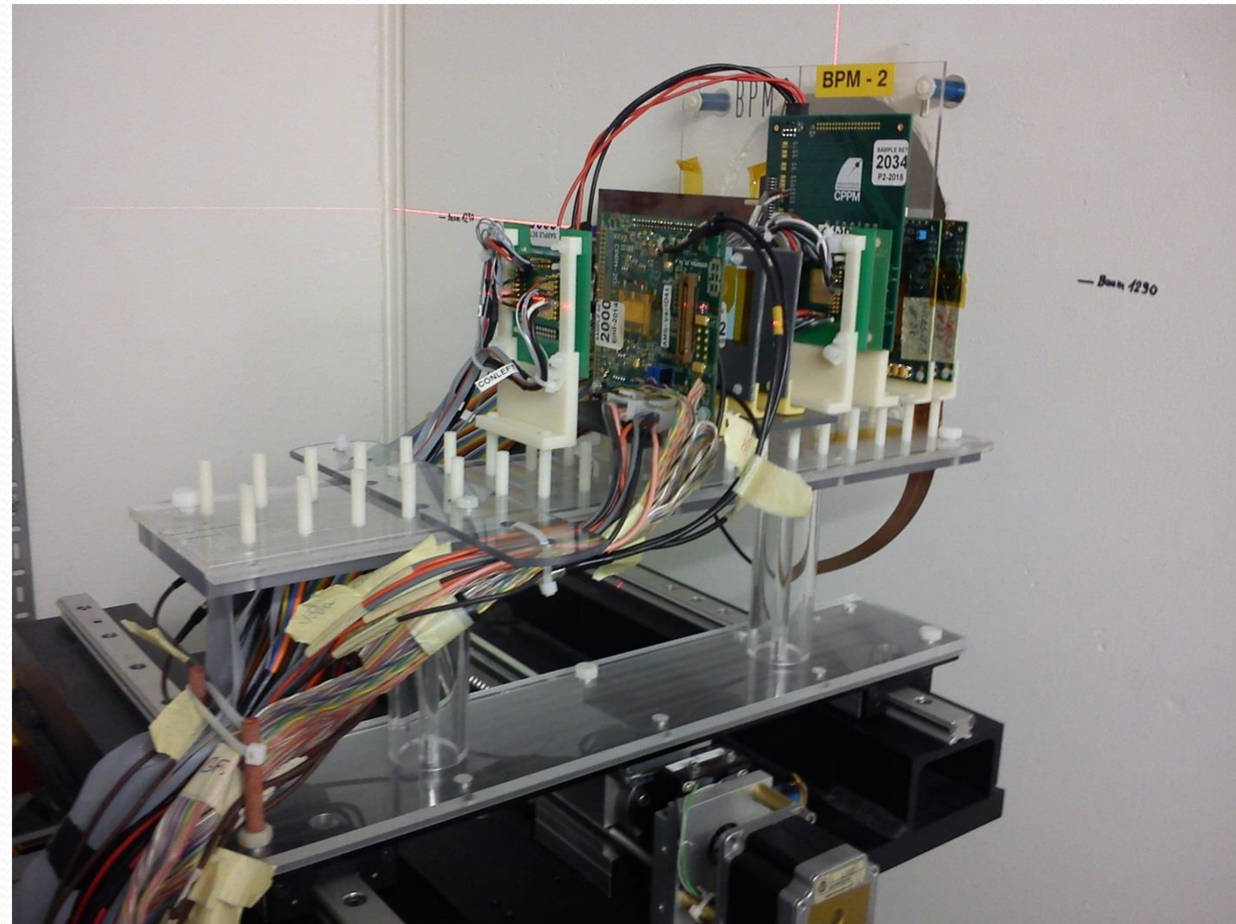
Next irradiation tests

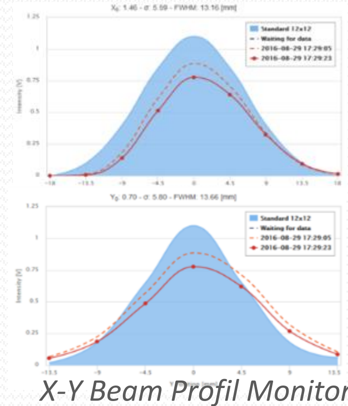
- The 24GeV primary proton beam is extracted from the PS ring



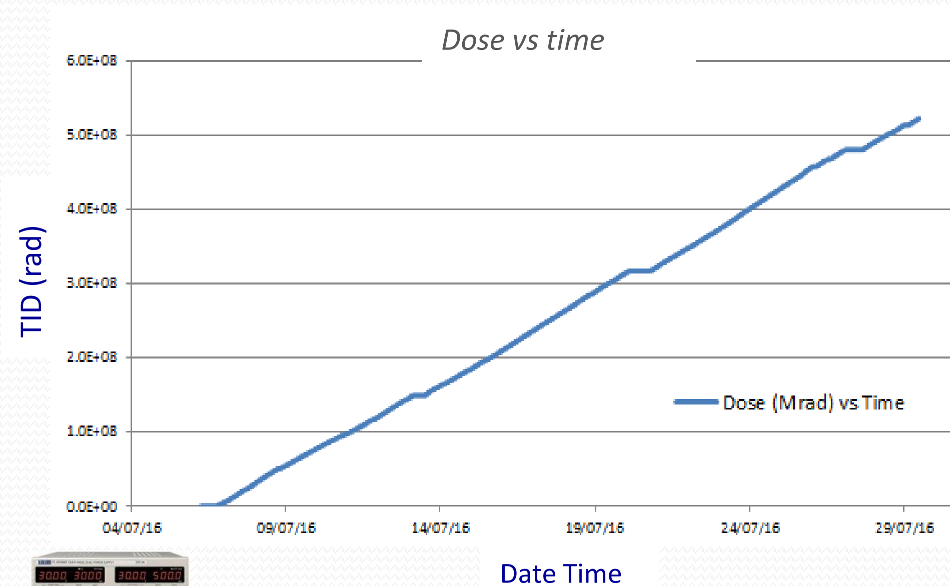
- PS Irradiation tests (SEU and TID) scheduled on June 2016
- SEU from the Digital radiation test chip ??

SEU setup

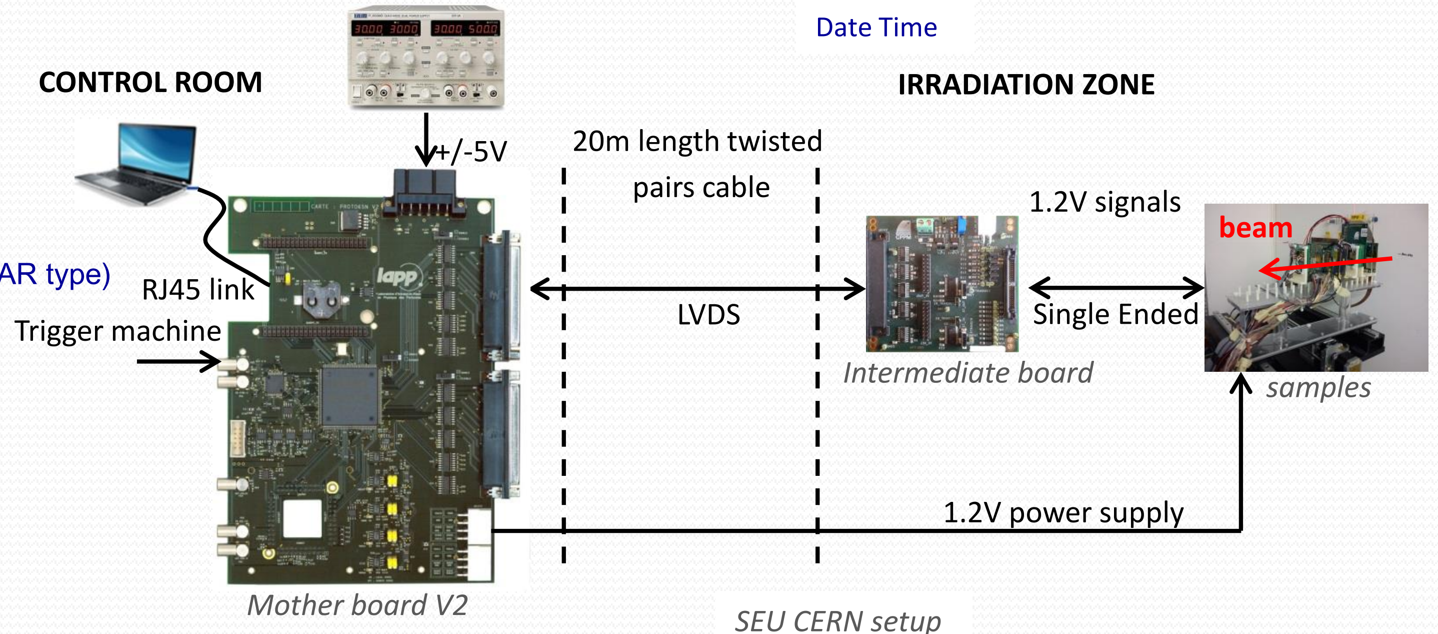
- 24 GeV protons beam line at CERN
  - 12.10[10] protons/cm²/spill
  - beam size1cm²
  - mean dose rate
    - 950krad/h
  - TID: 500Mrad
  - exposure time 3 weeks



X-Y Beam Profil Monitor

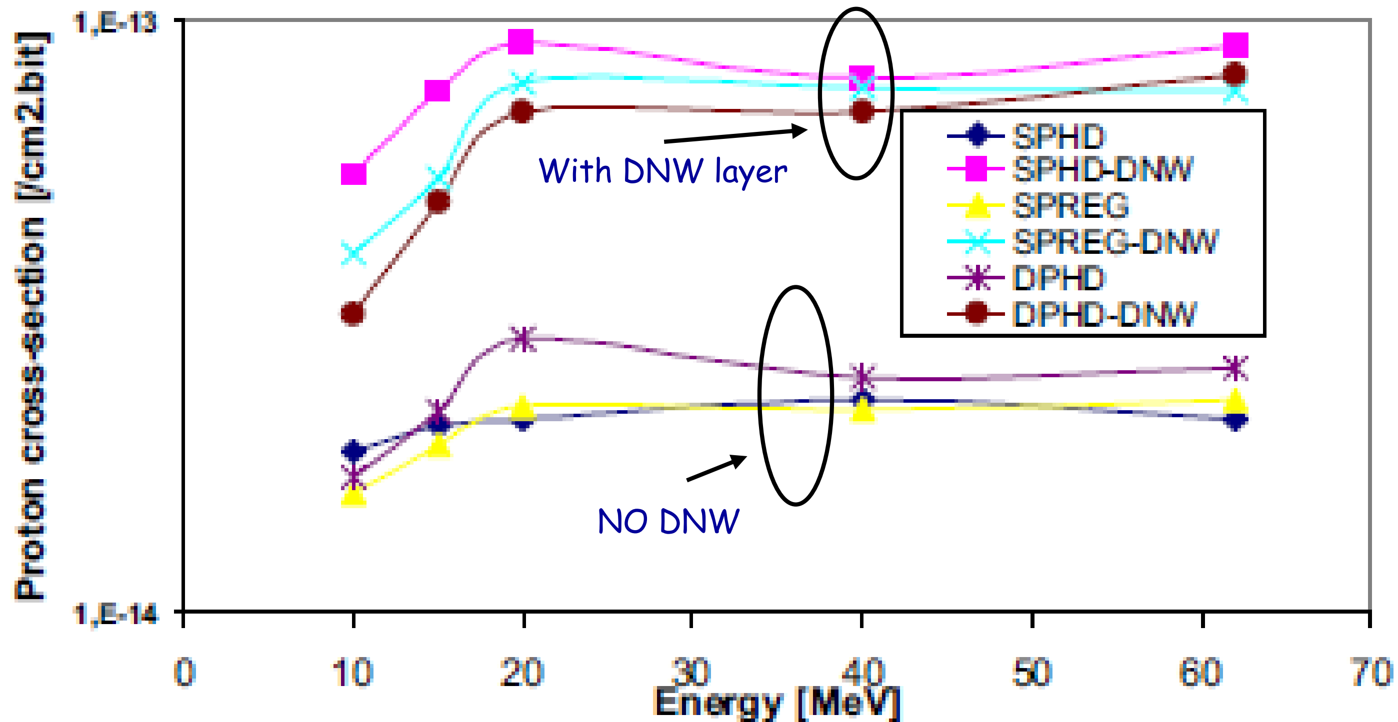


- Mother board V2
  - with a LAPP collaboration
  - nanoPC BeagleBone card + FPGA
  - Flexible programing
  - 30 logic signals available (*)
  - Analog channels
    - ADC (4 16 bits conversion channels SAR type)
    - 4 DAC (16 bits) (*)
  - Monitoring (°C, current supply)
  - Lab tests + irradiation tests
  - (*): evolution on going



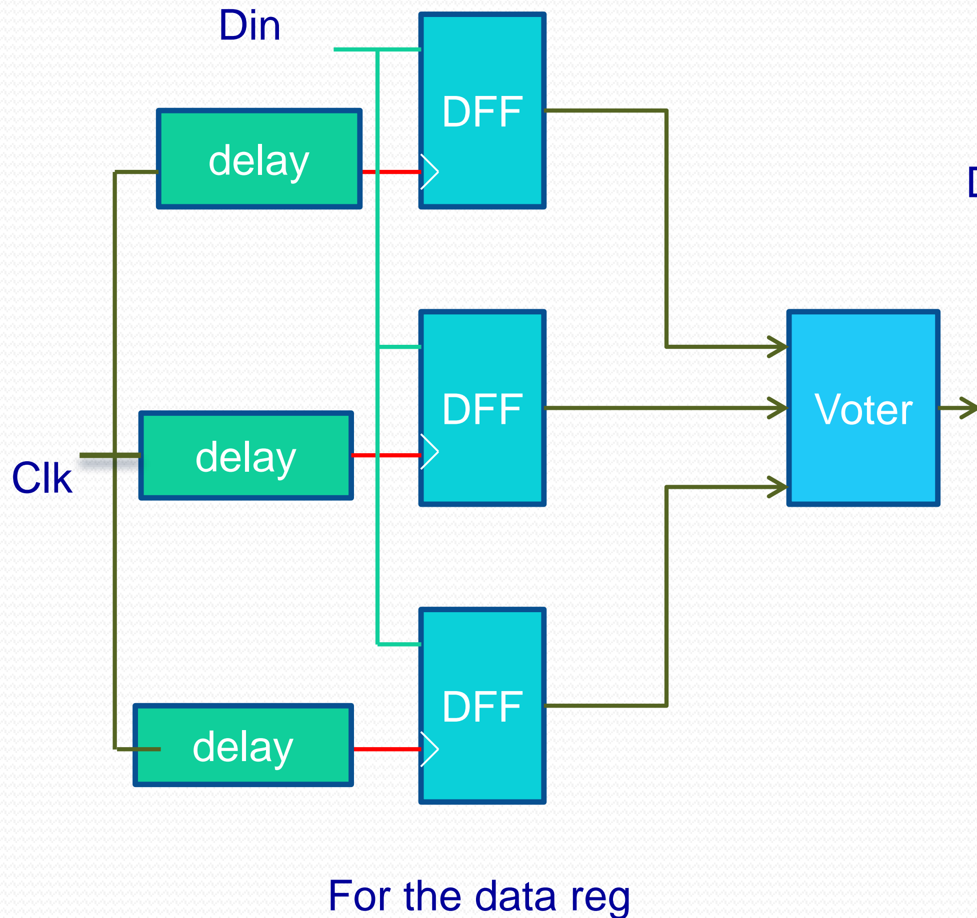
SEU CERN setup

DNW effect on SEU

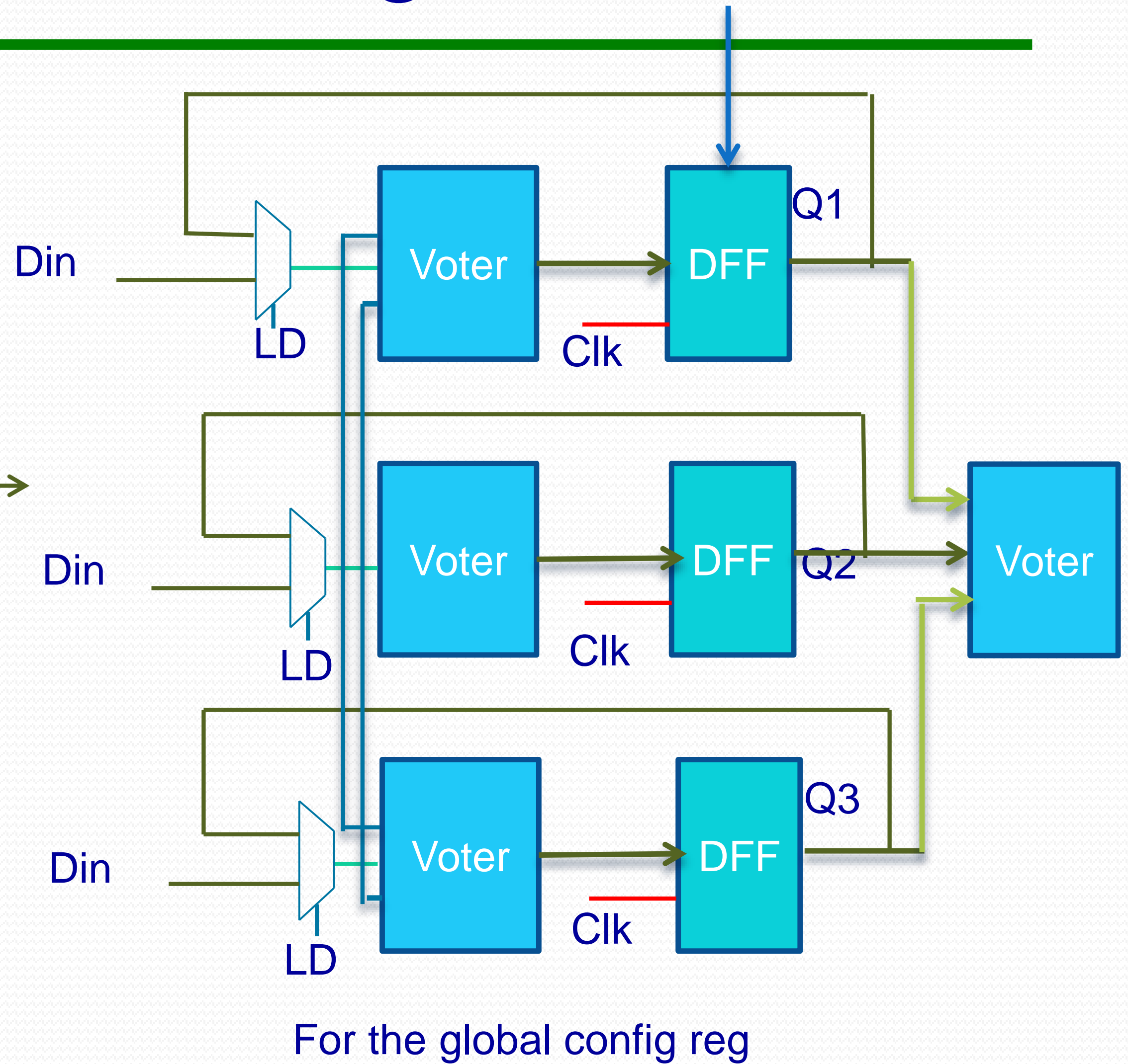


- SRAM structure with 65 nm ST process
- No DNW : cross section ~2 E-14 cm² (Similar with our measurements)
- DNW : increase of the proton cross-sections by a factor 5

SEU strategy for the digitalRD53A



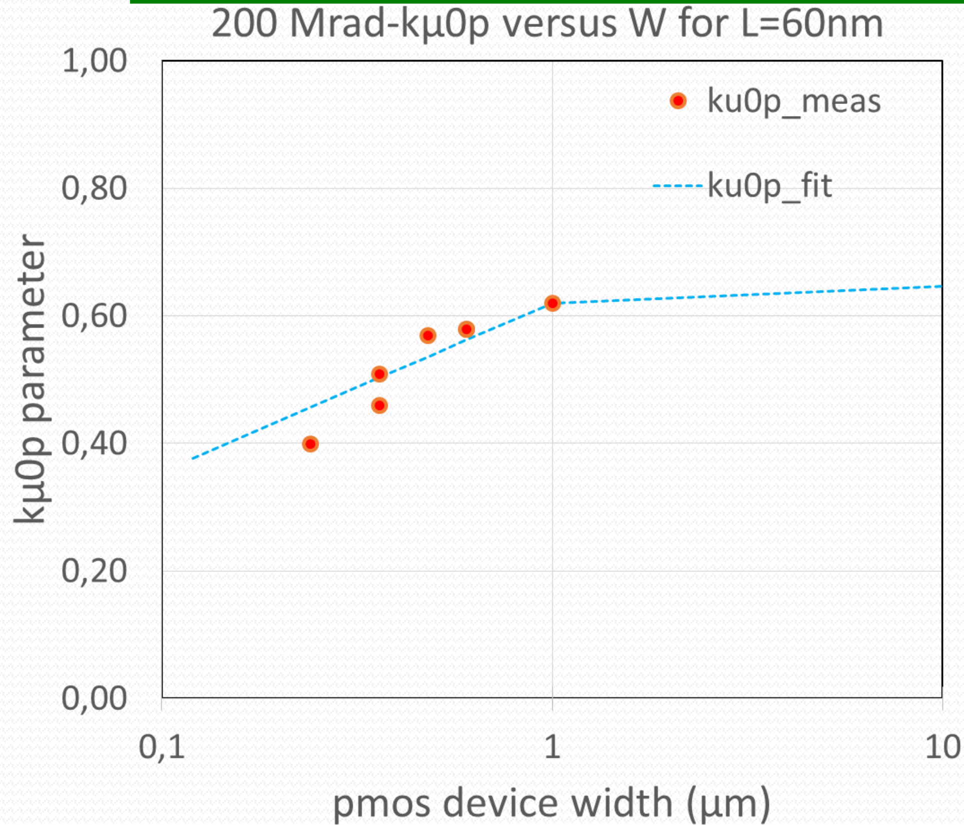
For the data reg

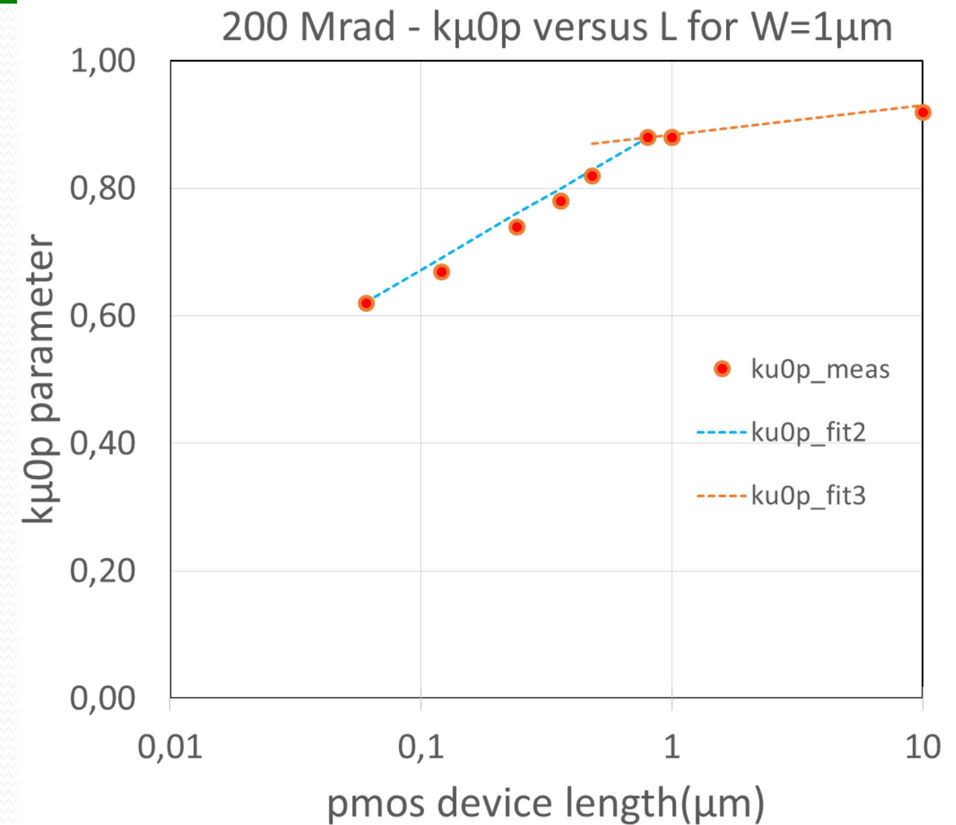


For the global config reg

- Minimum distance of 10 µm between redundant storage nodes
- Synthesis tools used for the design

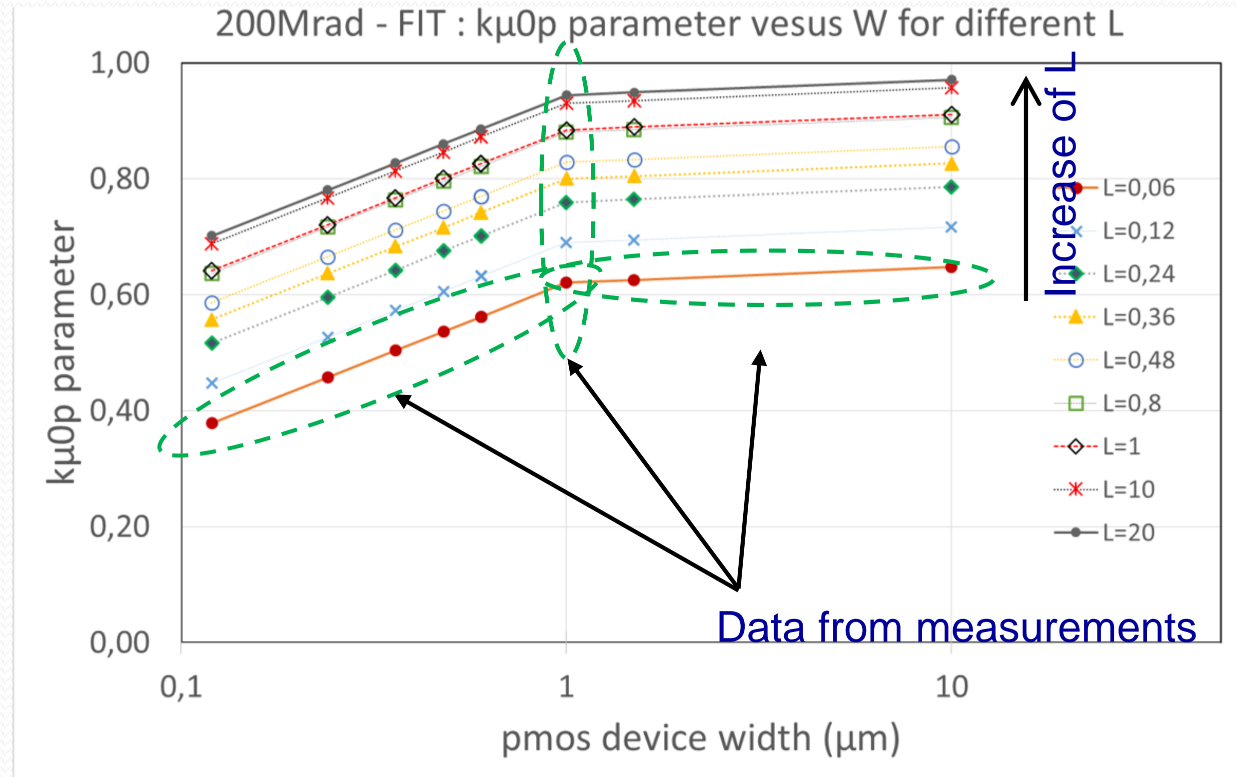
Pmos fitting parameters





- The current drive loss depends strongly on the device width W and on length L
- A large part of data used in the fit (200 Mrad and 500 Mrad) were provided by Stefano Michelis (CERN)
- For pmos devices only the transconductance degradation is considered (Annealing is not included)
- The mobility factor kµ0p is defined as the ratio µ0_rad/µ0_prerad
- kµ0p depends on W and on the L

pmos fitting parameters



- The current drive loss depends strongly on the device width W and on length L
- The mobility factor kµ0p is defined as the ratio µ0_rad/µ0_prerad
- kµ0p depends on W and on the L
- For PMOS devices the transconductance degradation is considered as the main effect (Annealing is not included)
- kµ0p relation to W and L is implemented inside the TSMC spectre model file

Digital Library Information

- Timing
  - Combinational
    - Delay
    - Transition time
  - Sequential
    - Delay & Transition time
    - Hold & Setup
    - Recovery and Removal
- Power
  - Leakage : Static power
  - Internal Power

Different standard cells implemented for each library

STANDARD CELL NAME	DESCRIPTION
INVD1	Inverter with driving strength = 1
INVD4	Inverter with driving strength = 4
ND2D1	2-input NAND gate with driving strength = 1
ND4D1	4-input NAND gate with driving strength = 1
NOR2D1	2-input NOR gate with driving strength = 1
NOR4D1	4-input NOR gate with driving strength = 1
XOR2D1	2-input XOR gate with driving strength = 1
CKBD1	Clock buffer with driving strength = 1
CKBD4	Clock buffer with driving strength = 4
CKBD16	Clock buffer with driving strength = 16
DFCNQD1	Flip-Flop with async clear with driving strength = 1
LHCNQD1	Latch with async clear with driving strength = 1

- Library characterization
  - Cadence Liberate based on the spectre model for 200 Mrad and 500 Mrad

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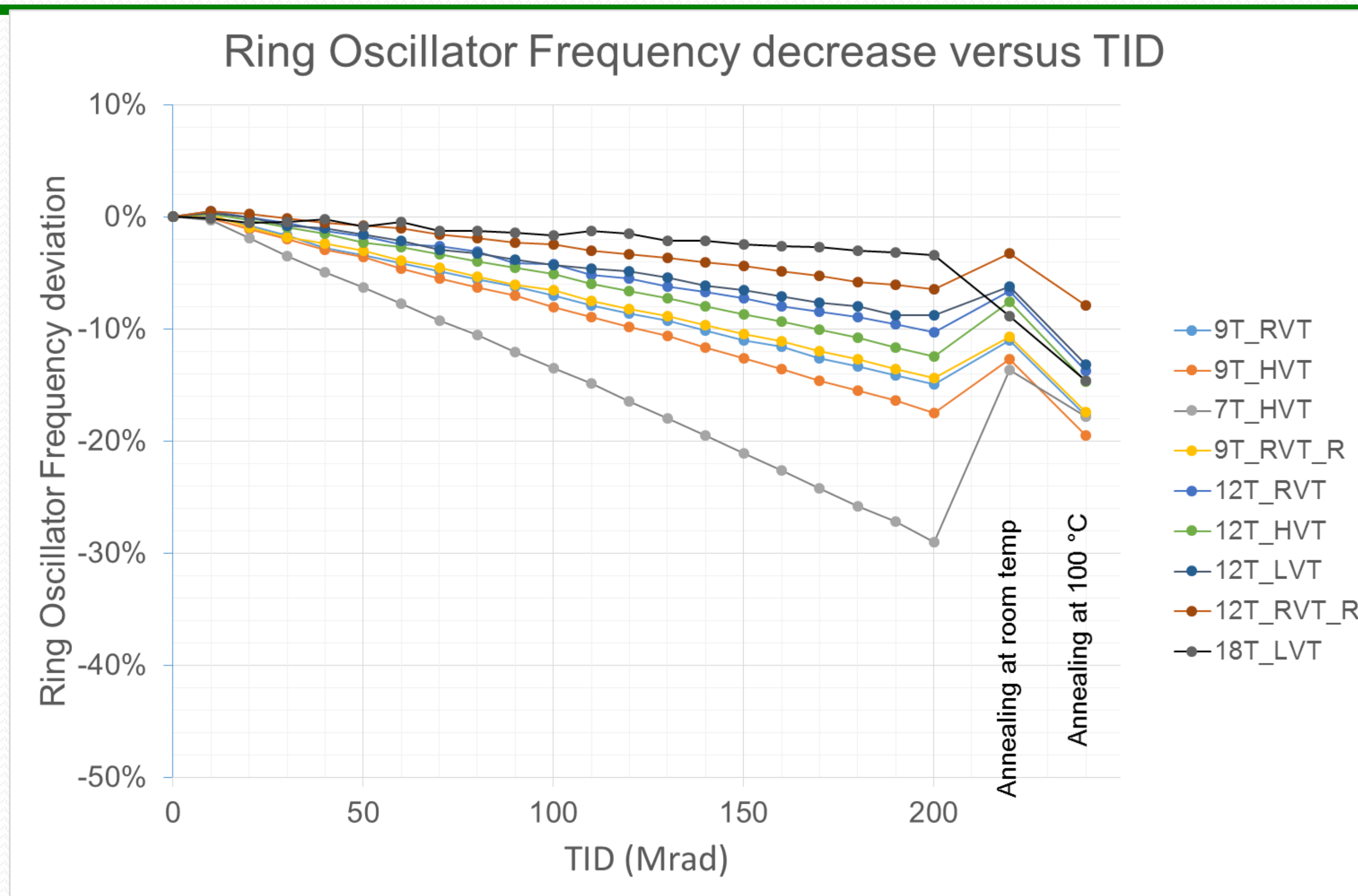
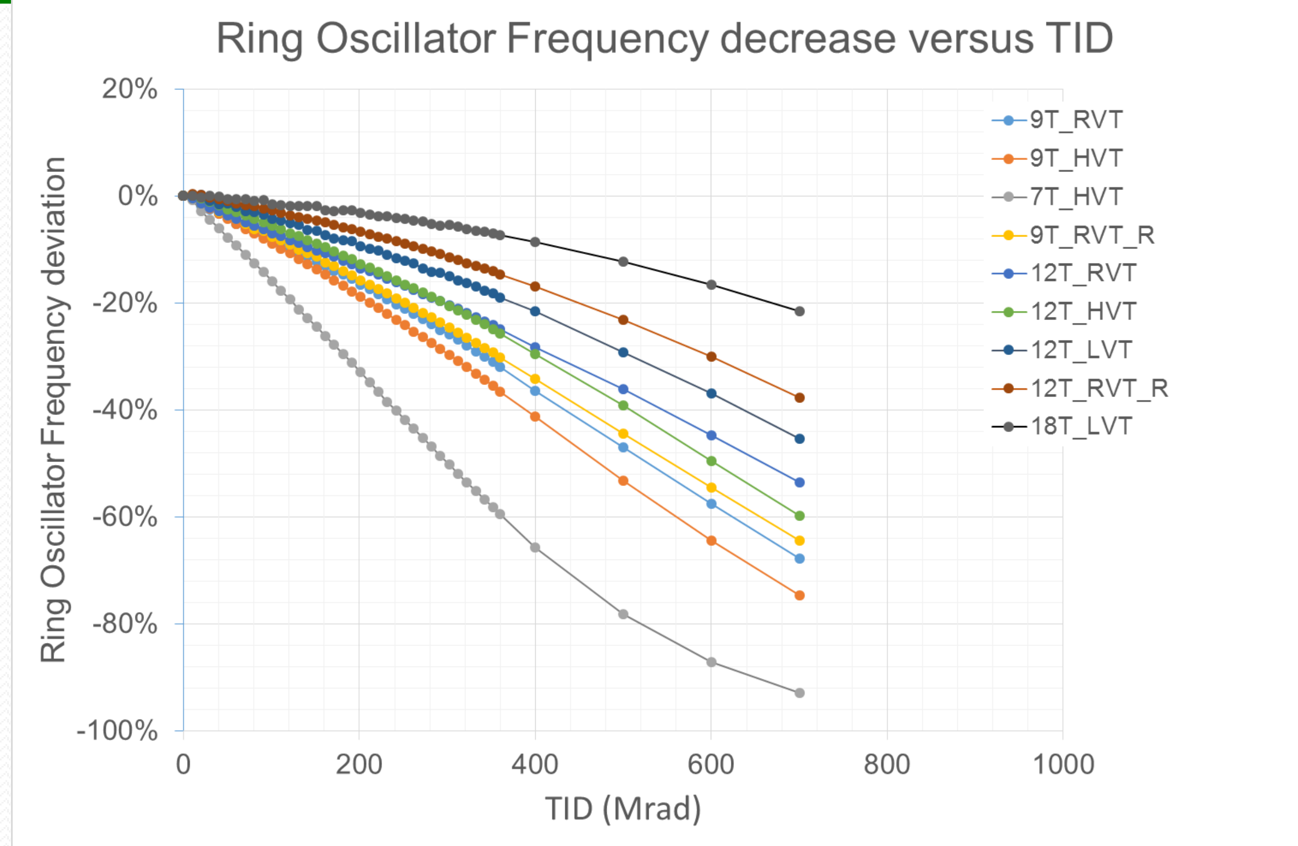
Results for 200 Mrad



- Different behaviour after room temperature annealing for 18T_LVT library (ELT transistors)
- 7T_HVT more sensitive but recovers better (in %) respect the rest of the libraries.
- For the rest of the libraries, the relationship of the behavior between libraries is the "expected": libraries with smaller size behave worse than big ones, libraries with higher Vt behave worse than libraries with lower Vt.

Results for 500 Mrad



Irradiation at 500 Mrad at room temperature

No annealing

Post-irradiation tests