WP4.3 activities at OMEGA and DESY/UNIH

on behalf of C. de La Taille

AIDA2020 annual meeting, Paris, 5 -7 April 2017

Organization for Micro-Electronics desiGn and Applications

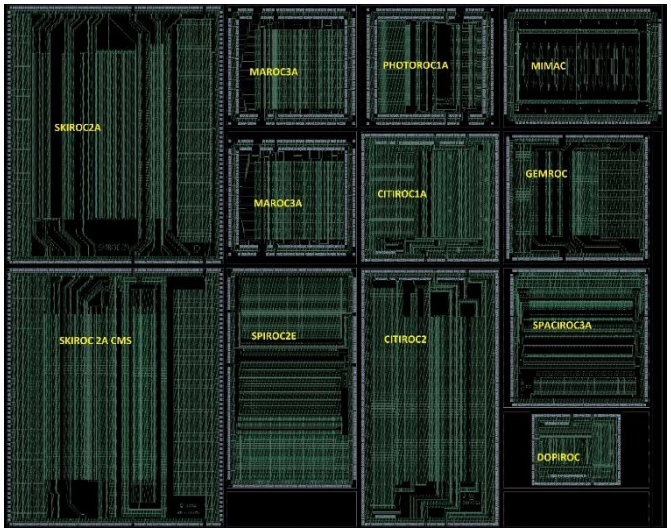
WP4.3 : Technology choice

(CNRS-IPNL, CNRS-OMEGA, DESY, AGH-UST)

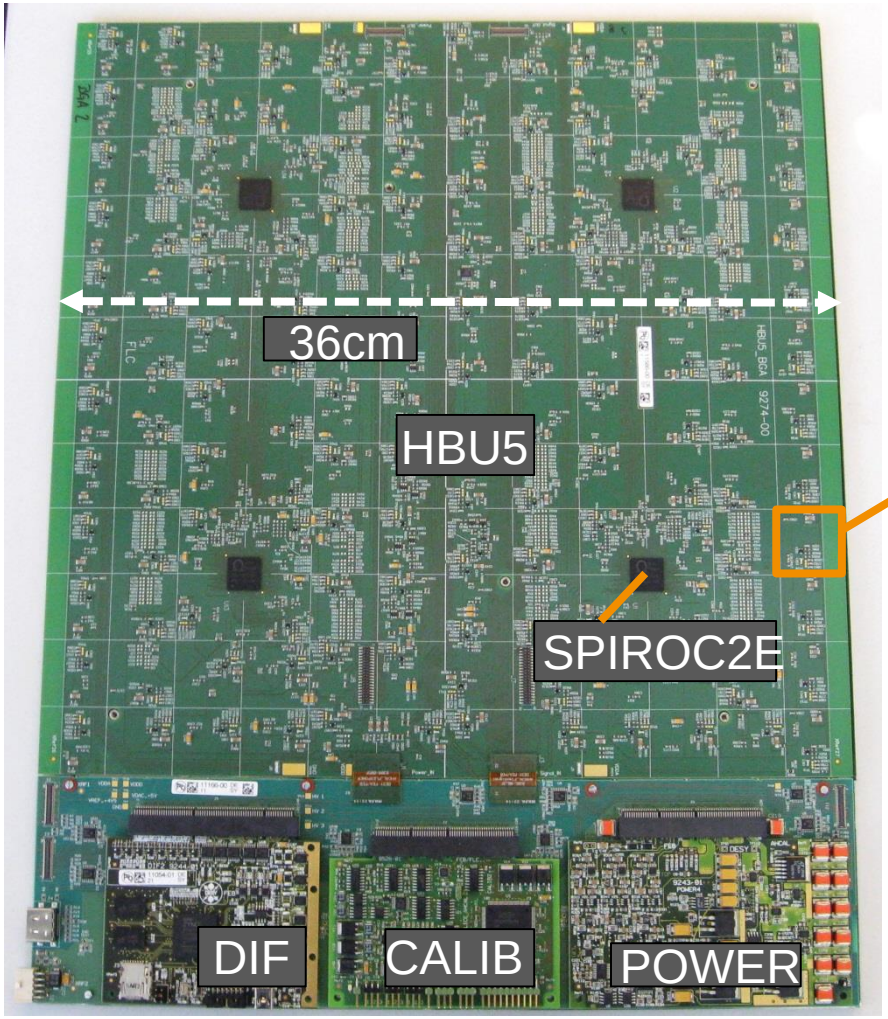
- Select best SiGe 130/180 nm process for high speed/high dynamic range ASIC design to upgrade current SiGe 350 nm AMS process MS22 M14
  - **Proposal to choose TSMC 130 nm**
    - **Qualified by CERN for high radiation environment**
    - **Wider community**
- Deliver SPIROC3 SiPM readout for calorimeter readout of WP14
- Deliver RPC high timing readout chip for WP13 (Petiroc3)
- D4.2 M36 resp CNRS (OMEGA)
- Share expertise within HEP community
- Studies for LHC run 2, ILC…

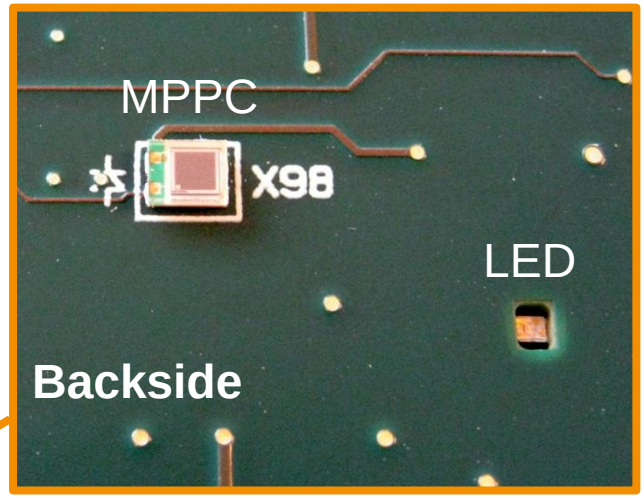
AIDA2020 AT OMEGA in 2016

- Fabrication and test of 800 SPIROC2E and SKIROC2_CMS in SiGe 0,35
  - Will equip large scale prototypes of WP14
- Move to TSMC130nm for HL-LHC and AIDA2020
- 4 chips submitted in MPW 130n (may&dec 16)
  - LAUROC : Liquid Argon Upgrade Read Out Chip (ATLAS)
  - HGCAL TV1 : Test Vehicle 1 for CMS HGCAL
  - ALTIROC : Atlas Lgad Timing ROC for ATLAS HGTD
  - HGCAL TV2 : test vehicle 2 for CMS HGCAL



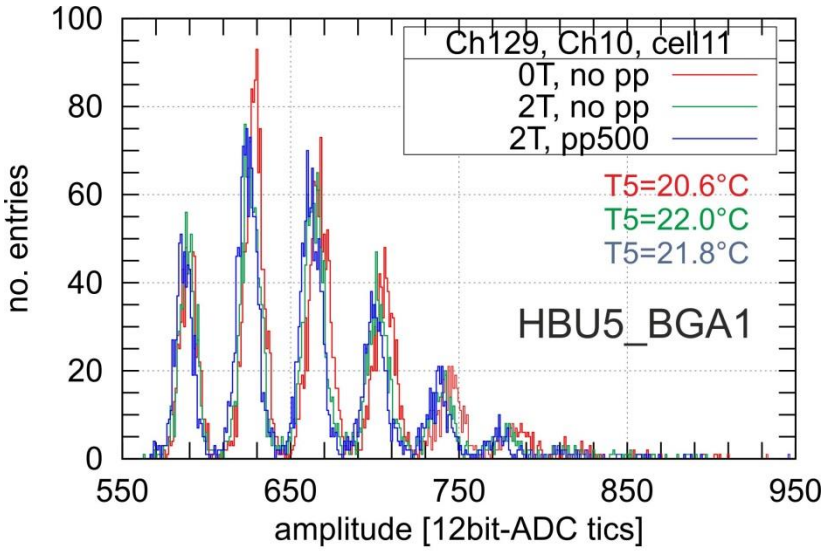
AHCAL Frontend Detector Module (HBU5)



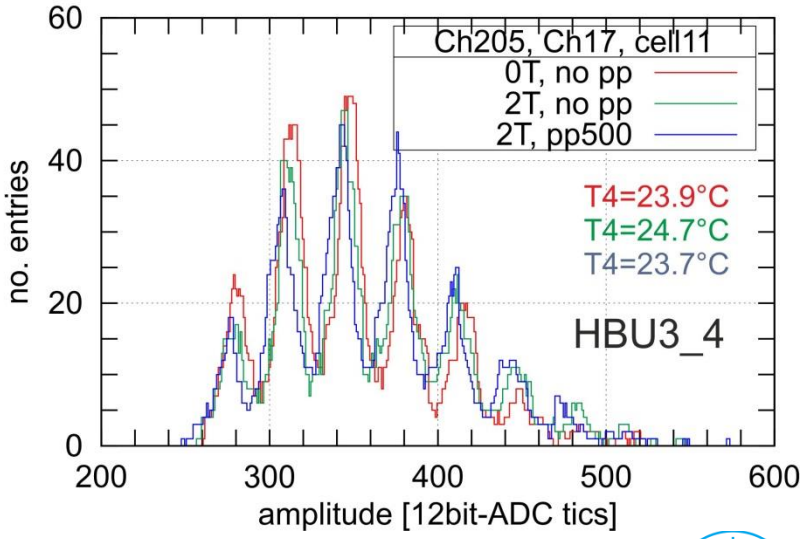


- 144 detector channels
- 36x36cm², 0.75mm thick
- MPPCs: 2600px, gain>500,000
- Individually wrapped tiles (not shown) on backside
- Four analogue/digital readout ASICs: SPIROC2E (BGA)

Magnetic Test of Front-End and DAQ Modules



- Three test runs with LED system:
  - SPS with magnet off
  - SPS with 2T magnetic field
  - SPS with 2T field and power-pulsing (100µs switch-on time)
- HBU5 with SMD MPPCs and HBU3 with THT MPPCs show no influence by magnetic field.



Uni Heidelberg contributions to WP4

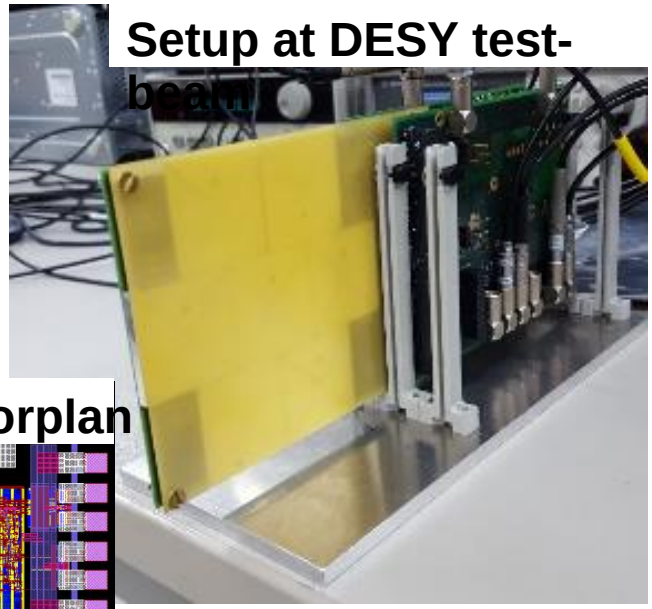
KLauS: low power SiPM Charge Readout ASIC

UMC 180nm technology

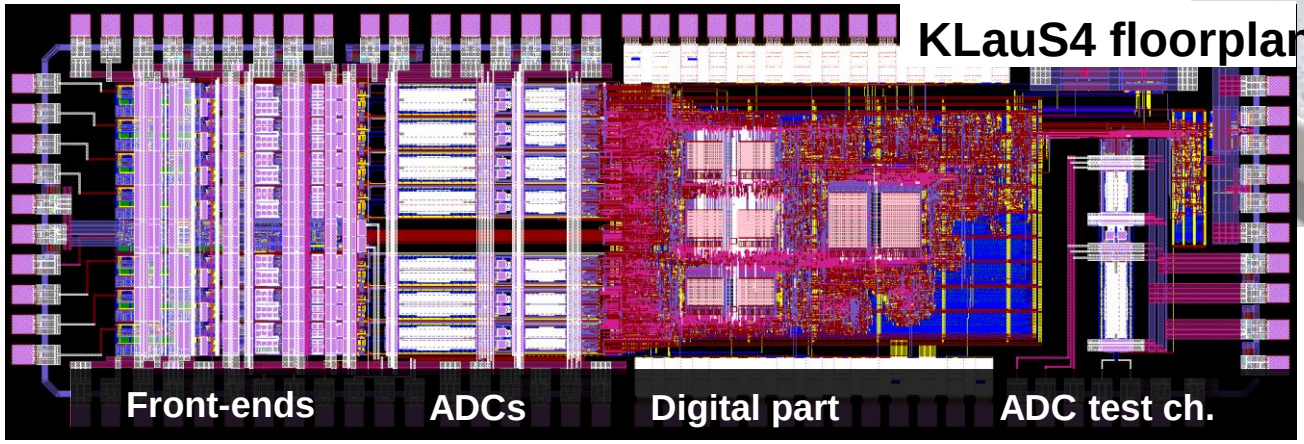
KLauS4: Seven channel prototype under test since Q3/2016

- all analog features implemented
- 10b/12b ADC per channel
- 1 TDC-only channel (external time reference)
- Features for test-beam usage
- 1 separate ADC test channel

Setup at DESY test-beam



KLauS4 floorplan



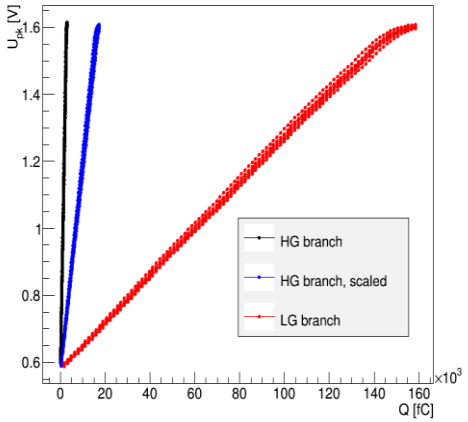
KLauS4 characterization

- Characterization in lab:
  Dynamic range, comparator thresholds,
  SPS using different SiPM, ...
- Beam test using 3 layers (15 equipped channels) at DESY
  Gain experience in operation:
  System calibration
  Testbeam features, power-gating, multiple channel operation
- Currently undergoing detailed characterization

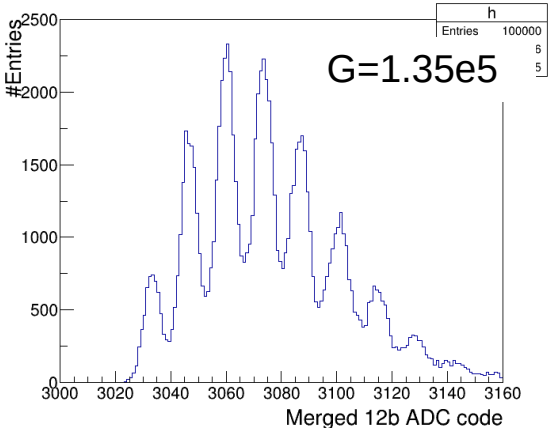
Only minor issues found, will be corrected in next version:

Full 36 channel ASIC, Submission in summer 2017

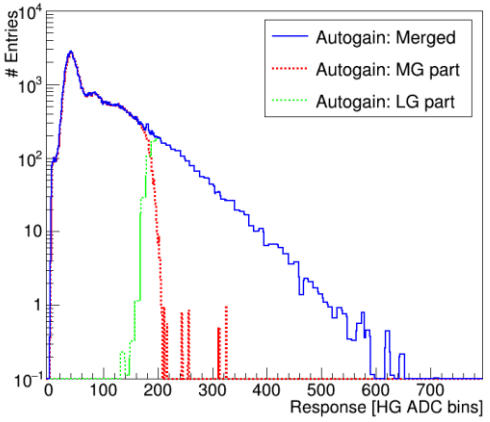
Charge measurement linearity



Single pixel spectrum: 10um pixel MPPC



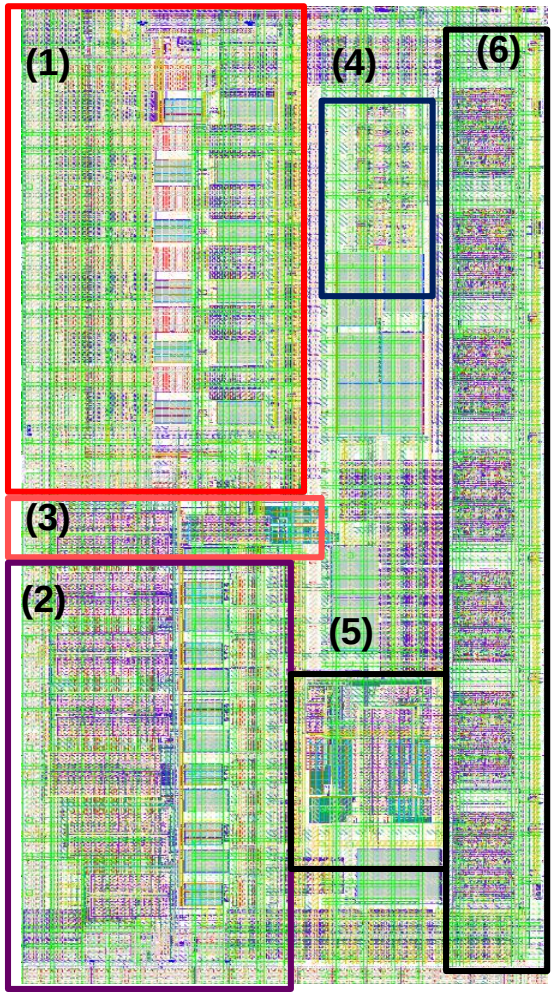
Test-beam: MIP spectrum autogain intercalibration



HGCAL Test vehicle TV1

- TSMC130 nm, area: 2x4 mm², useful 0.5x1
- Power supply: 1,2 – 1,5 V
- Submitted in may 2016
- Received in august 2016

- Floorplan
  - (1) positive input preamps x6
  - (2) negative input preamps x6
  - (3) baseline channel (CERN) x1
  - (4) discriminators x4
  - (5) CRRC shapers: HG and LG
  - (6) digital part



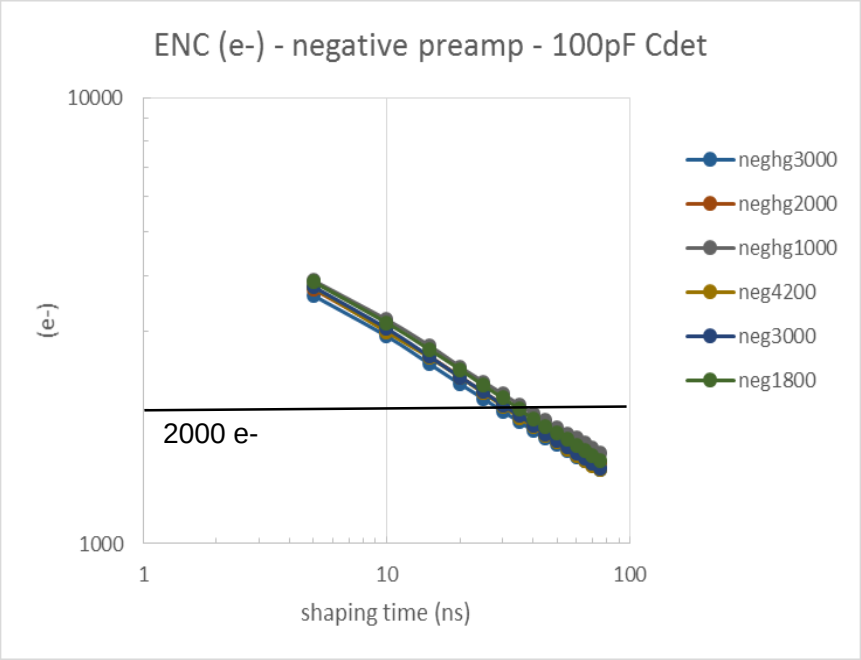
- Dedicated PAD available to characterize the shapers or the discriminators
- All bias can be externally tuned

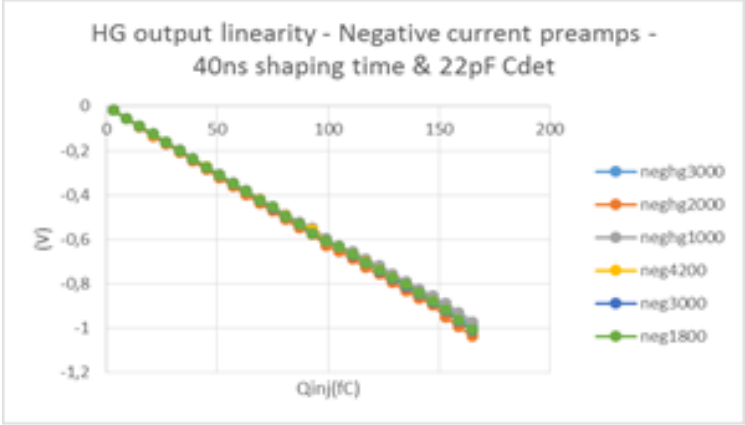
- Many measurements performed on the different configurations.

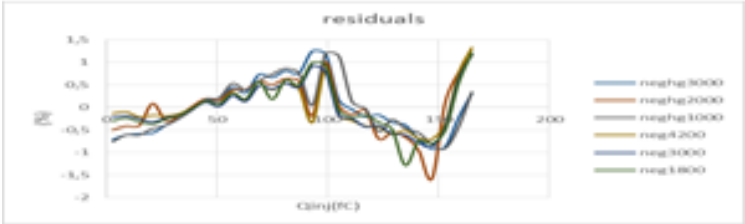
TV1 measurements

- Noise measurements in charge and current sensitive configuration
- Fit of ENC vs Cd gives e_n~0.5 nV/√Hz (OK) and C_{PA}~40 pF (too high)

30 ns pt	nghg3000	neghg2000	neghg1000	neg4200	neg3000	neg1800
e_n (nV/√Hz)	0,462	0,485	0,521	0,469	0,472	0,496
Parasitic Cap (pF)	42	41	38	44	44	42



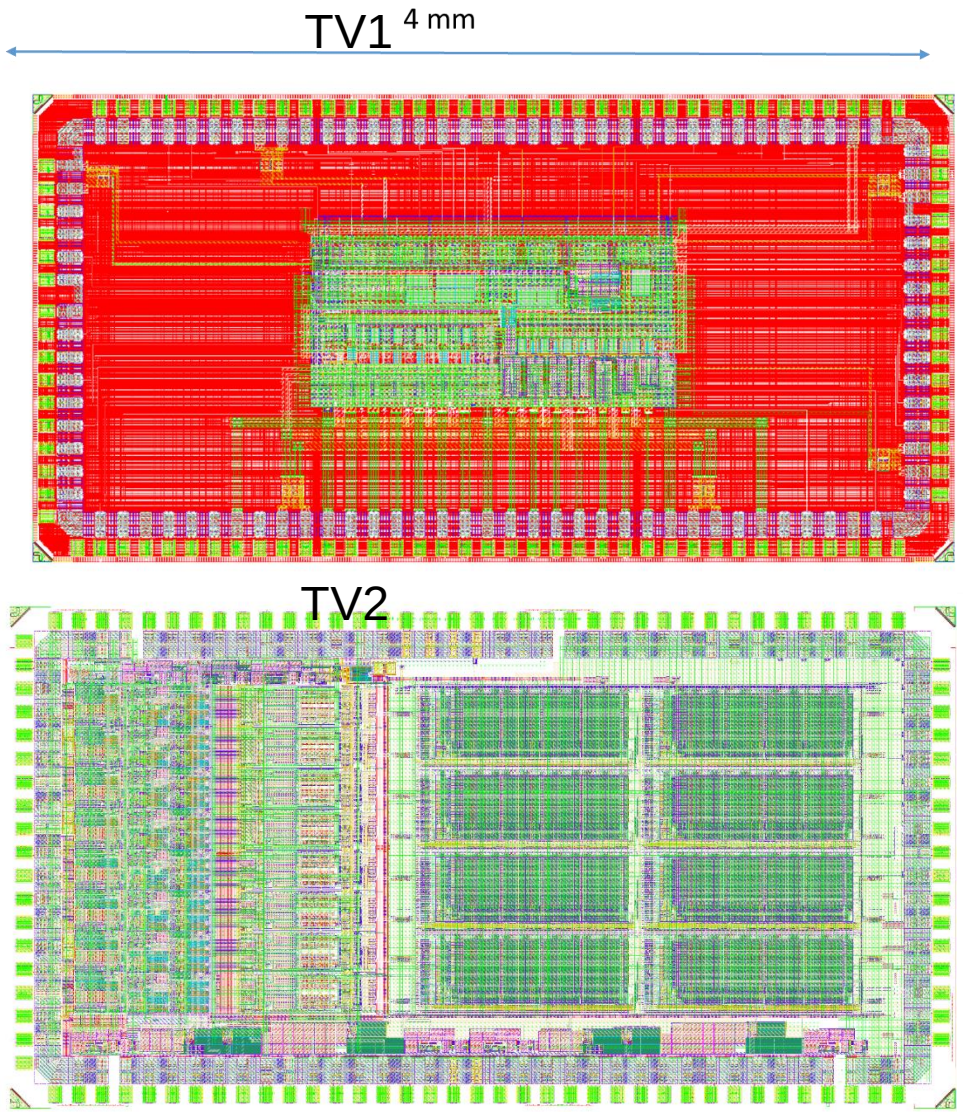




HGCAL Test Vehicle TV2

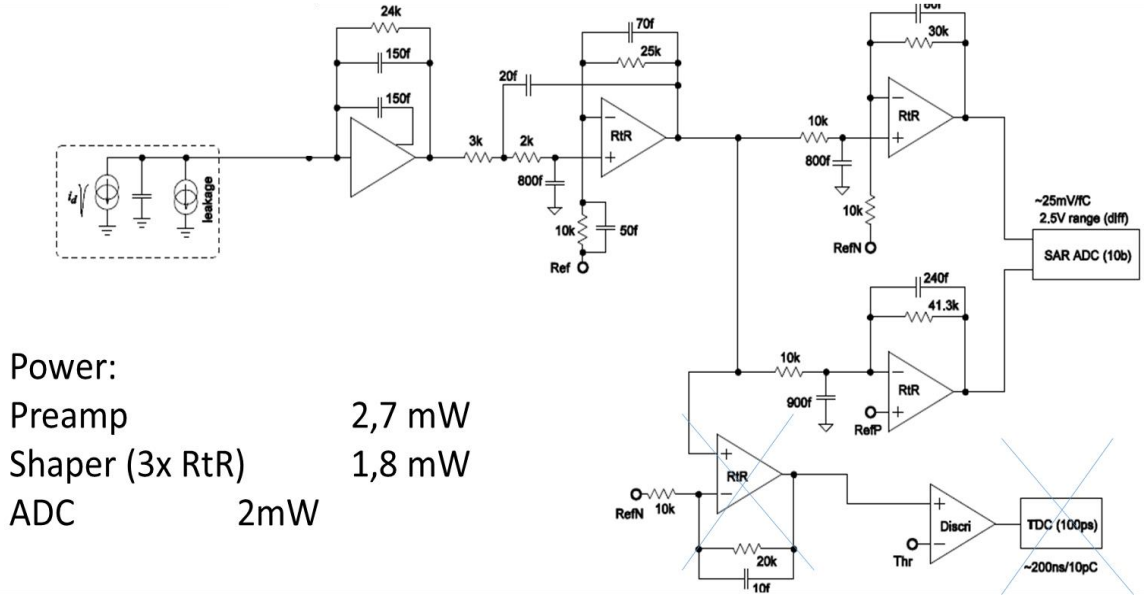
- TV2 groups 8*analog channels + ADC + 32x512 RAM (CERN)
- TV2 was sumbitted in December 2016 (HGCAL milestone) and received at the end of March 2017

- Testability :
  - External signal can be sent to ADC
  - For asynchronous ADC, local delay can be externally tuned
  - Data output are available directly or after memorization (@ 40MHz)
  - Test pulse injection (as in TP)
  - Analog probes: shapers, ADC
  - Digital probe: ToT



detail of HGCAL TV2

- Negative input preamp
  - High OL gain (90dB)
  - Variable Cf: 0,1fF – 1,5pF
  - Two selectable Rf: 24K & 1M
  - Cf_comp for high gain setting
- Shaping based on RtR amp
  - Tunable bias
  - Tunable miller comp
  - Global 10b DAC and 5b DAC in order to tune the Reference voltages
- 11b 40 MHz SAR ADC based on Krakow design
- ToT: No TDC but discri output on a PAD
- ToA: not implemented (high speed TDC still not available)



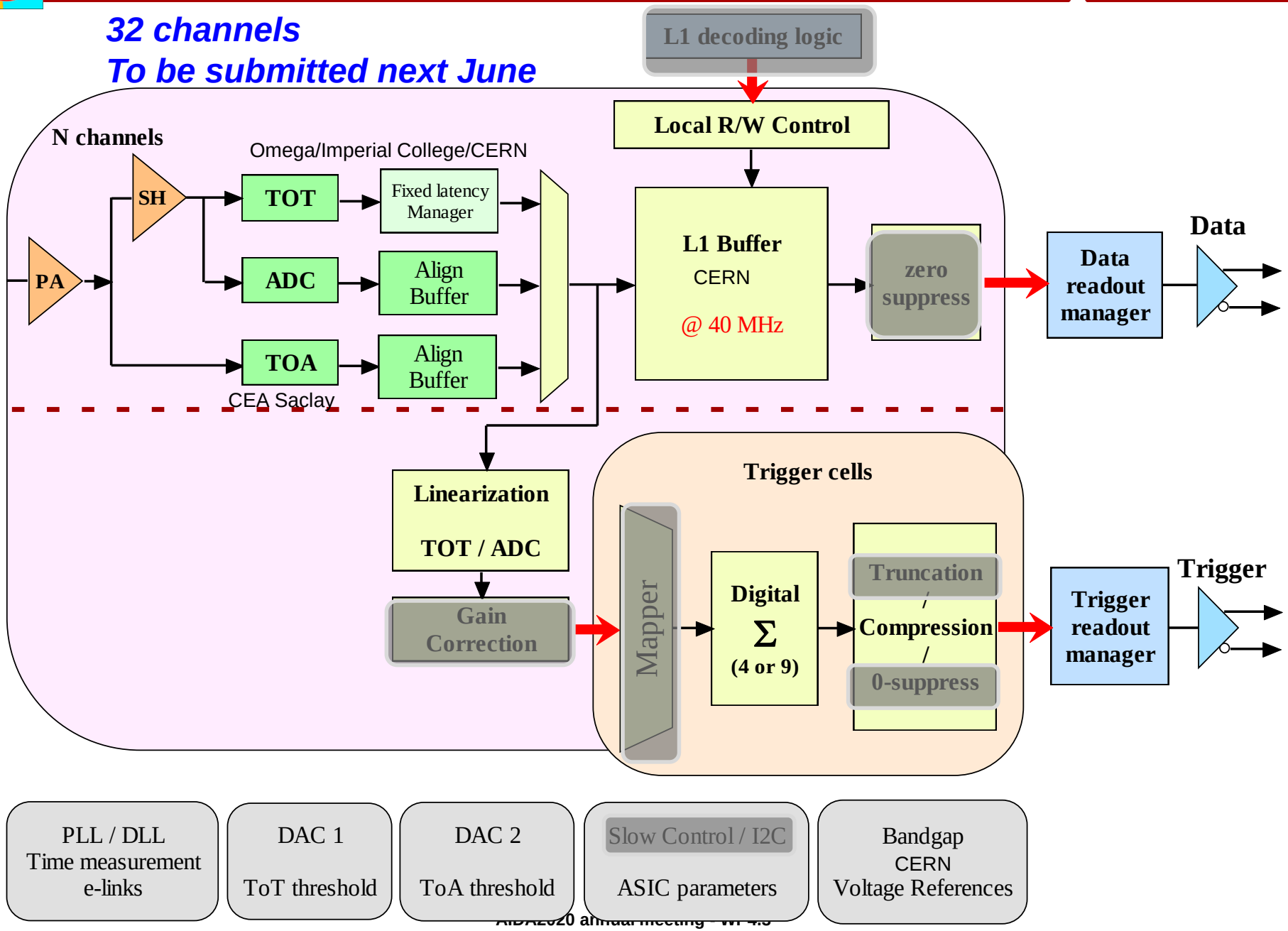
Power:

Preamp	2,7 mW
Shaper (3x RtR)	1,8 mW
ADC	2mW

Different versions:

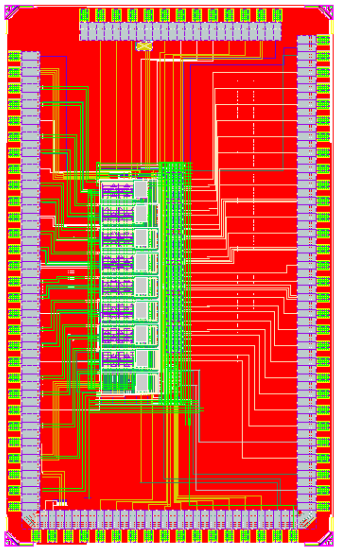
- Preamp: baseline, low parasitics cap (custom layout)
- 11b ADC: asynchronous and synchronous ADC, with and without bootstrap

HGROCv1 block diagram

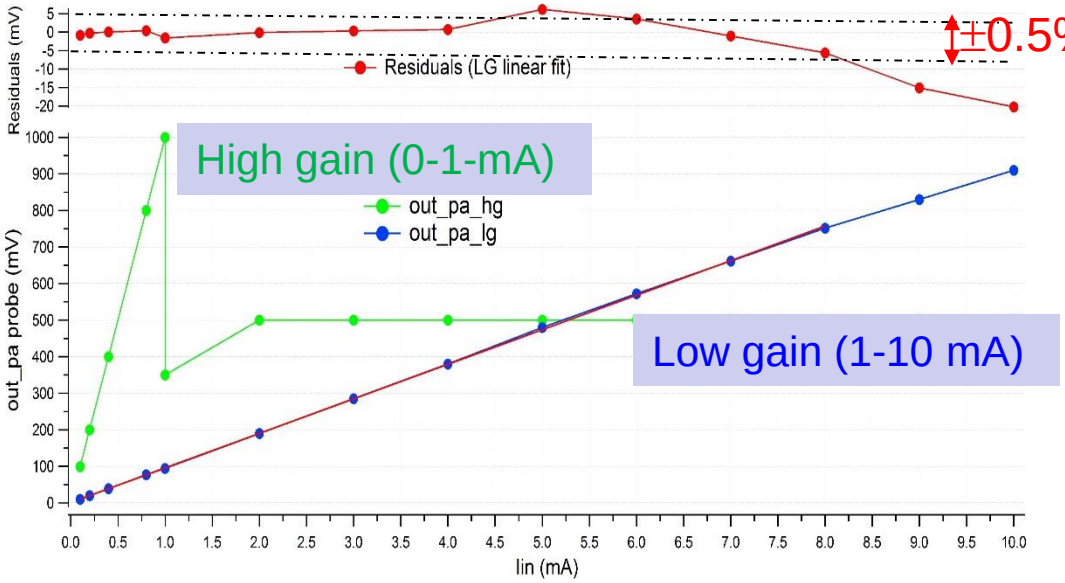


LAUROC

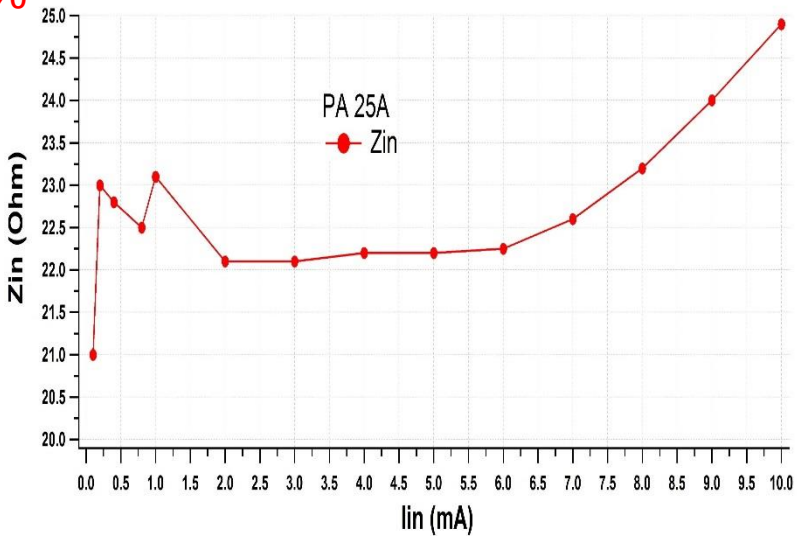
- LAUROC (TSMC 130nm) is a new innovative line-terminating preamp featuring “electronically cooled” resistance for the ATLAS liquid argon calorimeter upgrade
- Submitted in May 2016, received in August 2016
- Good testbench performance on input impedance and linearity
- But excessive noise compared to simulations



Linearity : High and low gain



Zin vs Input current

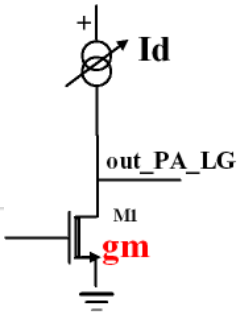


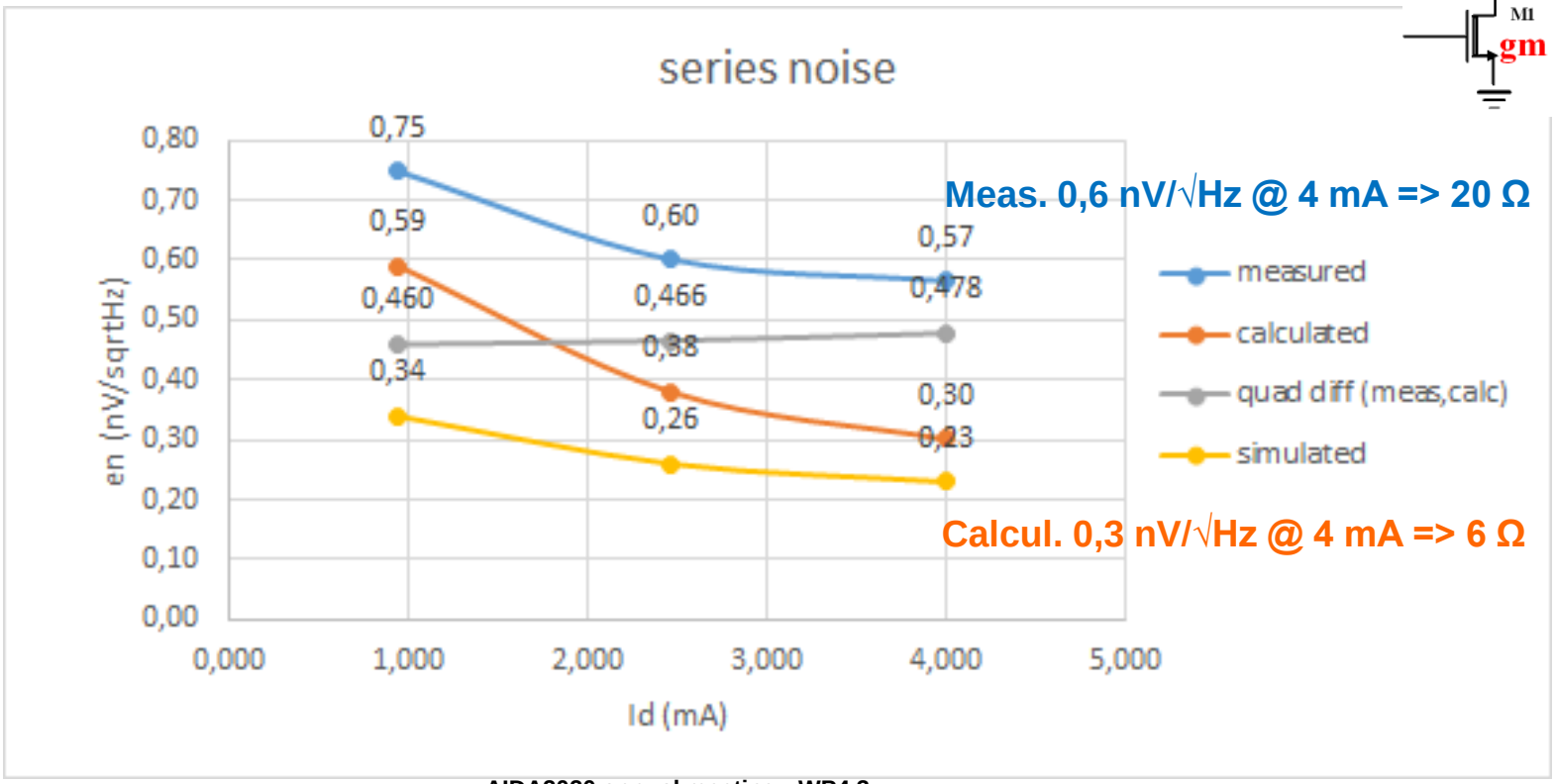
- Excessive noise => Measurement of input transistor alone
- Noise spectral density e_n vs I_d current: Measured, calculated and simulated e_n inversion)
- **Simulation** gives a smaller e_n than the calculated one
  - Id= 4 mA: Sim= 0.23 nV/√Hz (= 3.3 Ω) Calculated en= 0,3 nV/√Hz (5,6 Ω) => 30% difference
- **Quadratic difference** of measured and calculated e_n is flat

=> Proves that there is an additionnal noise R equal to 14 Ω

Calculation

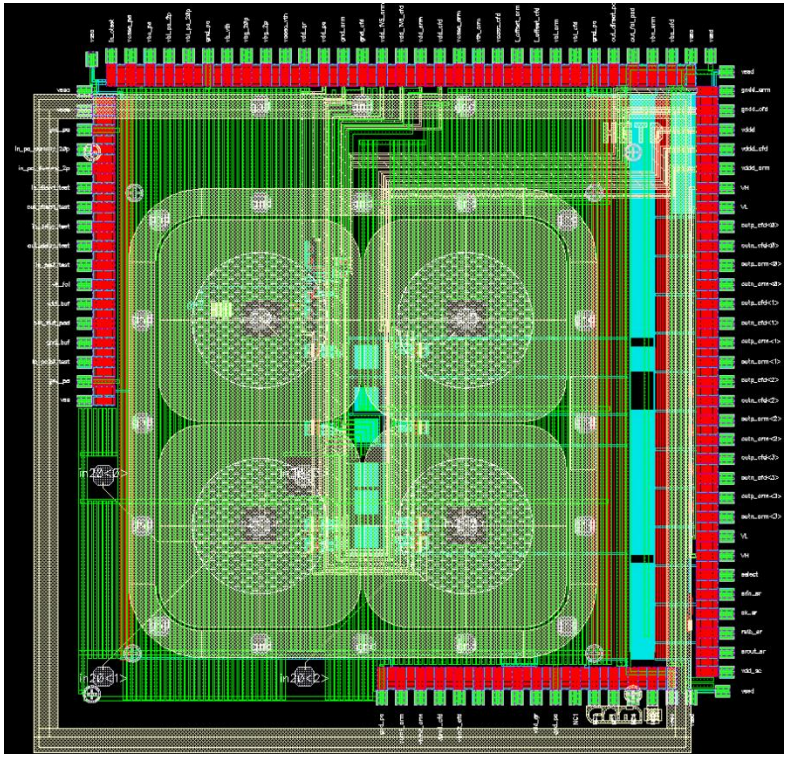
$$e_n = \sqrt{\frac{2kT}{g_m}}$$



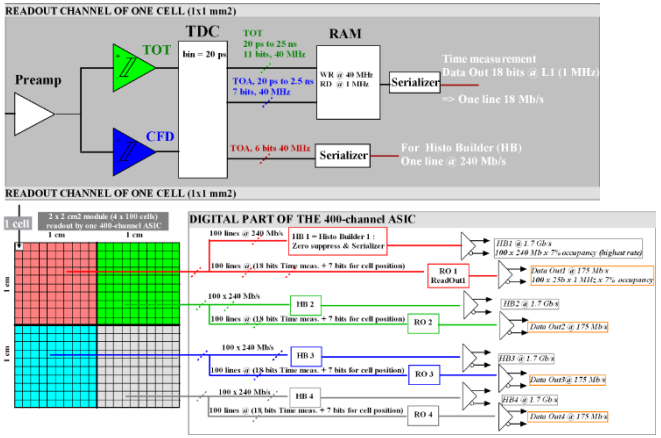


ALTIROC

- ALTIROC = ATLAS LGAD Timing ROC
  - Submission of a chip (TSMC130 nm) in December 2016 (MPW CERN/IMEC), received at the end of March 2017
  - 20 ps timing measurement with LGAD sensors for ATLAS HGTD
  - Test chip bondable to sensors of 1x1 mm² and 2x2 mm²
  - High speed preamp (1 GHz) + TOT + constant fraction discriminator (20 ps)

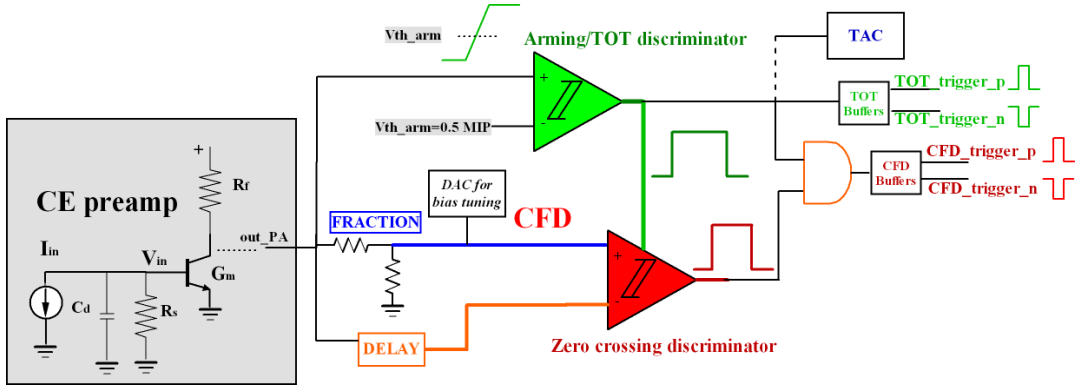


- Will evolve to 400 ch chip
  - With internal TDC (Collaboration with SLAC)
  - Bump bonded to sensor
  - Detector still to be approved

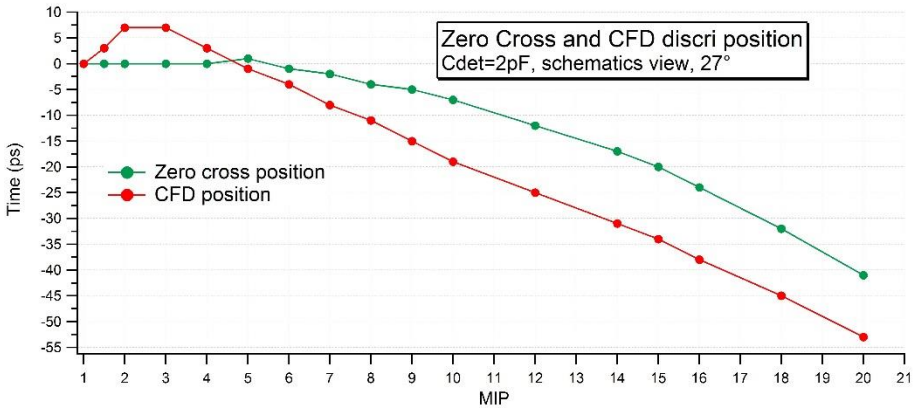


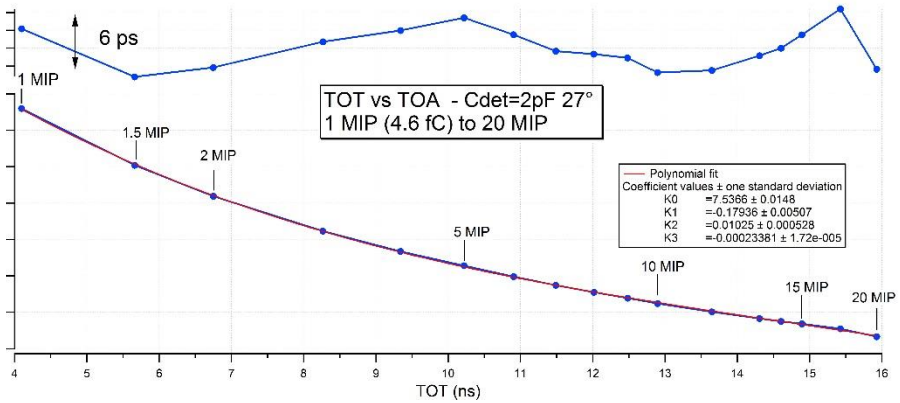
HGTD front-end

- ALTIROC0: 8 analog channels, 4 channels for 2 pF (1x1 mm2 sensors) and 4 channels for 10 pF (2 x 2 mm2 sensors)
  - Preamp followed by a TOT and a CFD
  - All trigger outputs available on PADs



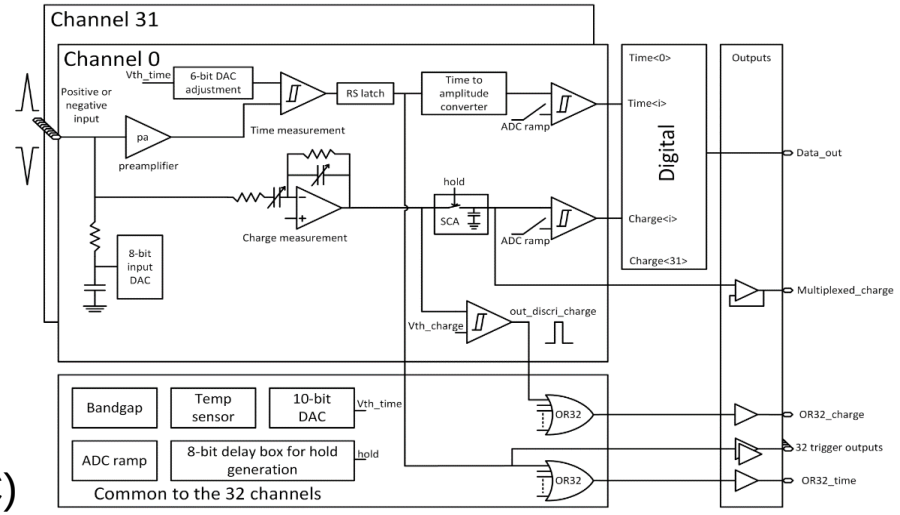
- Simulation results:
  - Jitter for 2 pF sensors (1x1 mm2): 22 ps @LGAD gain=10, 11 ps @ LGAD Gain = 20
  - Time walk (1 to 10MIP)
    - With TOT + correction: 6ps
    - With CFD: 30 ps effect (best integrated CFD nowadays = 1ns)





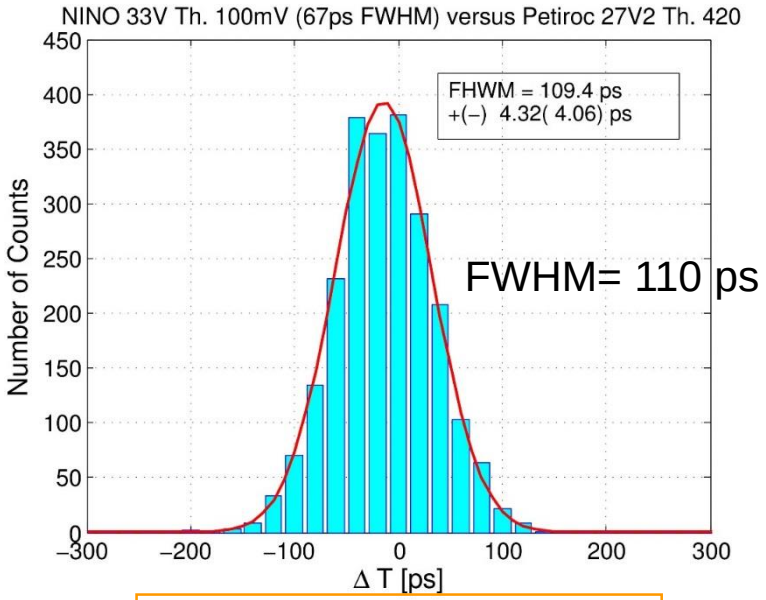
PETIROC2 to PETIROC3 (High Timing RPC WP13)

- PETIROC2A features high speed time and charge measurement (AMS 0,35µm SiGe)
  - 32 channels braodband amplifiers+discriminators
  - G = 25 BW = 0.9 GHz GBW = 20 GHz
  - Minimum Threshold <1 mV
  - Low power : 6 mW/ch
  - 10 ps jitter in analog operation (external TDC)
  - 50 – 90 ps with internal TDC (synchronous/asynchronous)



weeroc

- Submission of PETIROC3 in TSMC 130 nm in 2017
  - High speed preamp + discriminator
  - TDC from IPNL Lyon
  - Milestone for AIDA 2020 project WP13



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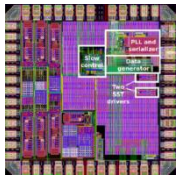
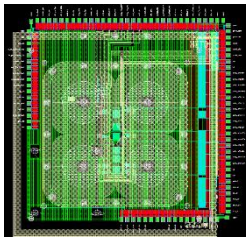
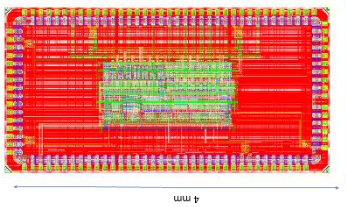
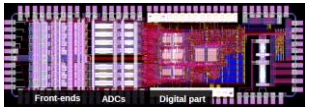
Conclusion

- 4 chips (TSMC 130nm) produced in 2016
- 32 channel ASIC HGROC (CMS HGCAL) to be submitted in june 17
- TV2 and ALTIROC will provide the blocks for SPIROC3 and PETIROC3 (deliverables of WP4.3)
  - SPIROC3:
    - A mix of HGROC (FE/digitization) and SPIROC (R/O)
    - Smaller input DAC span (2.5 V max supply)
  - PETIROC3: FE similar to ALTIROC
- A lot of sinergy between the chips and also sharing of expertise between the HEP groups






4 mm
2 mm


Front-ends
ADCs
Digital part