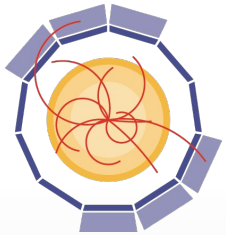
AGH University of Science and Technology



AIDA 2020

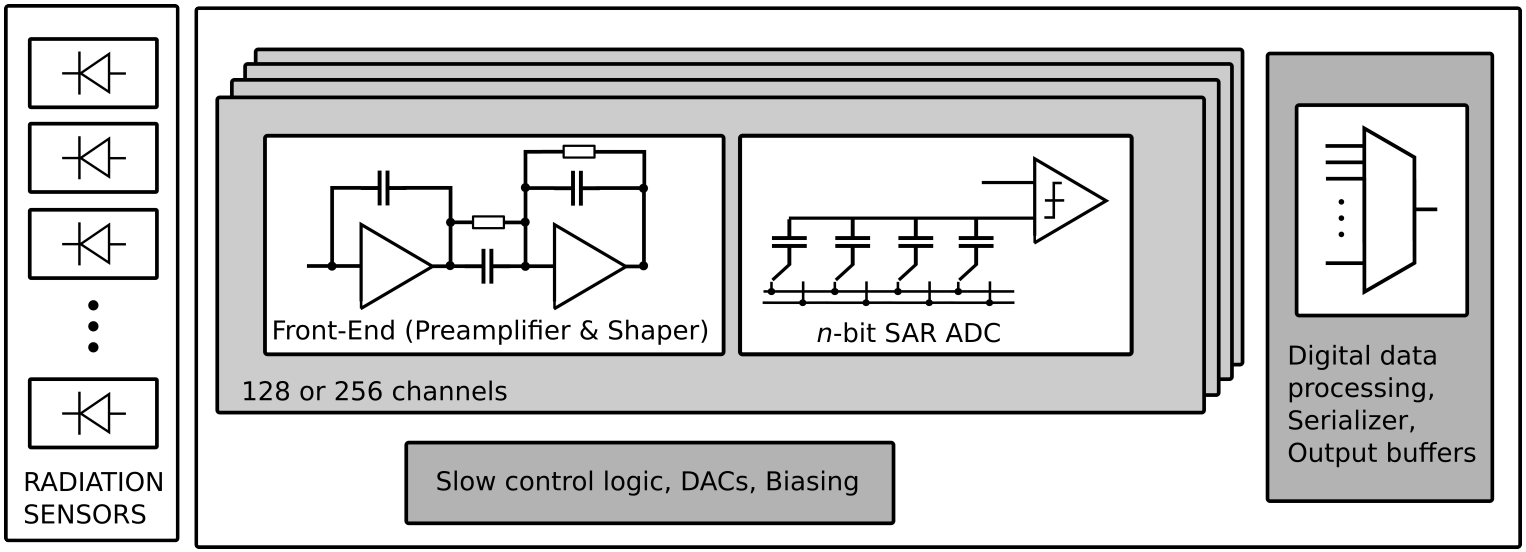
Developments for WP4 AIDA2020 at AGH Krakow

Marek Idzik on behalf of **AGH-UST**

Faculty of Physics and Applied Computer Science
AGH University of Science and Technology

AIDA-2020 2nd Annual Meeting, LPNHE Paris France 4-7 April 2017

Motivation
Advanced readout for particle detectors



For ILC/CLIC and LHCb applications we have been developing a fast ultra-low power multi-channel readout with front-end and ADC in each channel followed by fast serialization and data transmission. Such readout requires, apart from the front-end and ADC, various additional blocks like PLL, DLL, transmitter, receiver, bandgap, etc...

- Various blocks have been already developed in TSMC CMOS 130 nm
- Design is ongoing in TSMC CMOS 65 nm

Developments in TSMC 130 nm

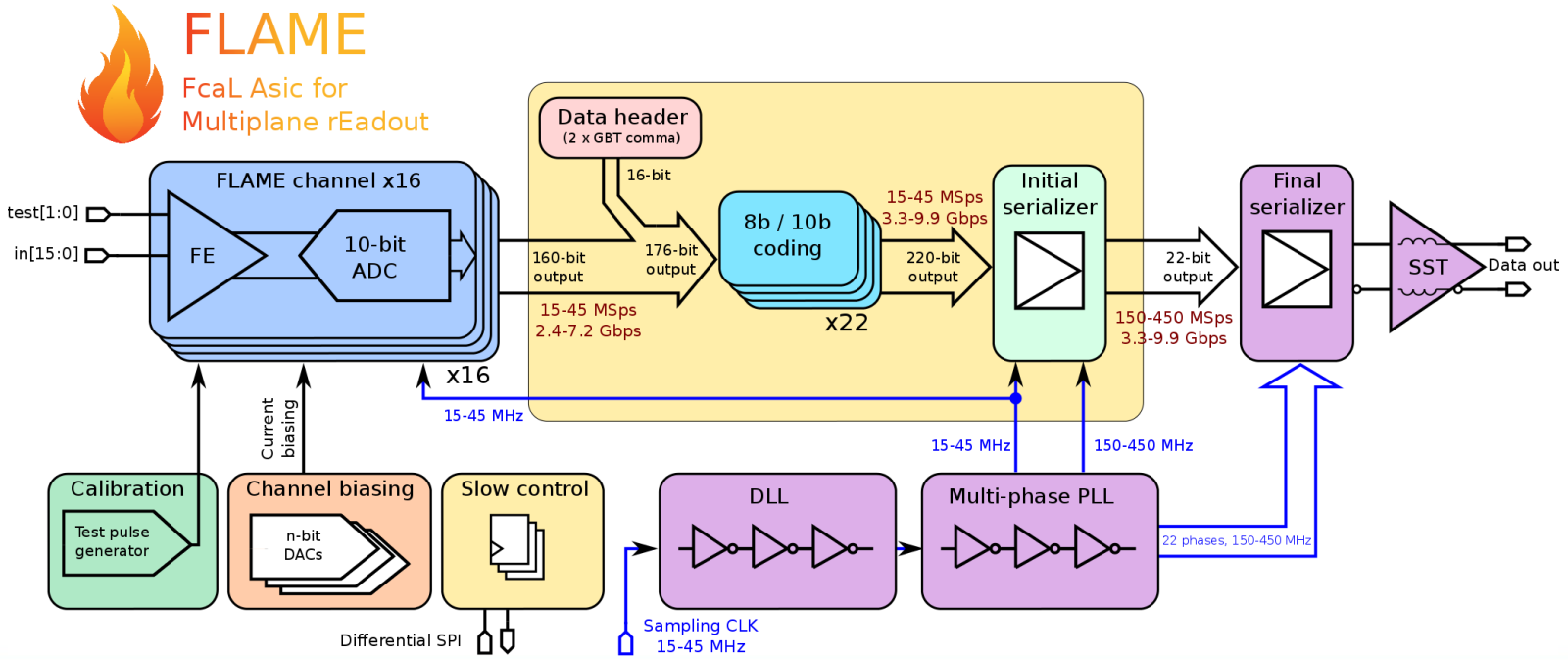
In last years we have developed for ILC/CLIC – FLAME ASIC and for LHCb – SALT ASIC many blocks:

- Ultra-low power SAR ADCs: 6-bit (up to 100MSps), 10-bit (up to 50MSps), 12-bit (not tested yet)
- PLLs (for clk generation), multi-phase PLL (for serialization), DLLs (for sampling time setting)
- SLVS I/O, SST driver
- Bandgap and temperature sensor
- DACs, opamps, etc...

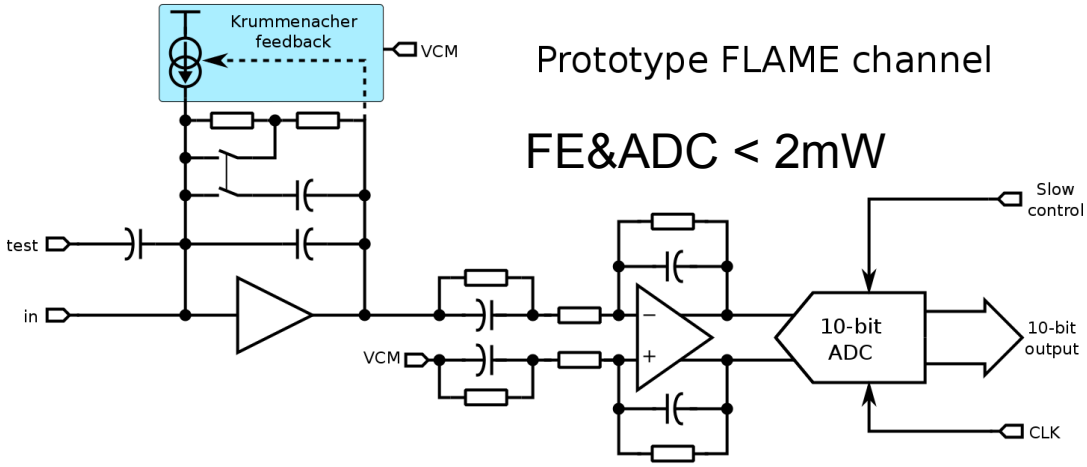
Here we show only two recent developments in synergy with our works for WP14

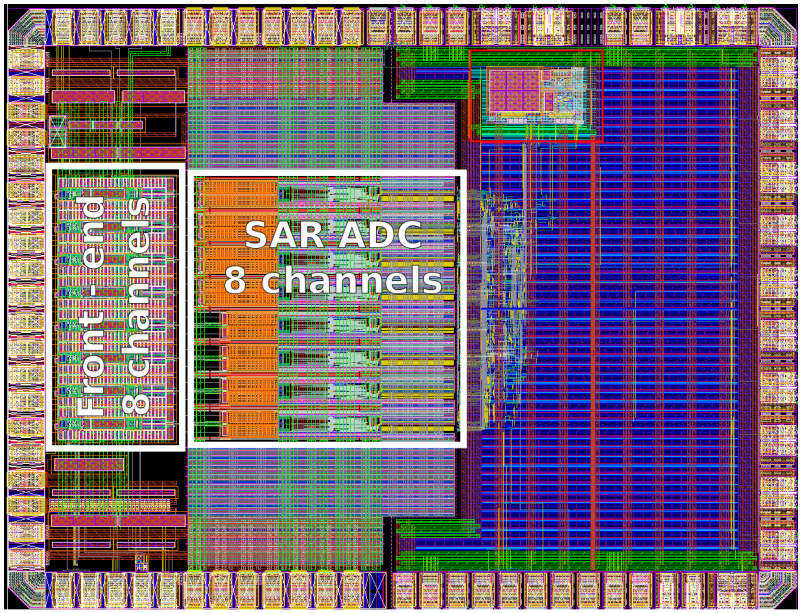
FLAME – dedicated readout ASIC for ILC in TSMC CMOS 130

- For **very compact** calorimeter we need an ultra-low power, SoC type (all functionalities on chip) readout ASIC
- FLAME: 16-channel ultra-low power readout ASIC in CMOS 130 nm, FE&ADC in ech channel, fast serialization and data transmission, all functionalities in single ASIC

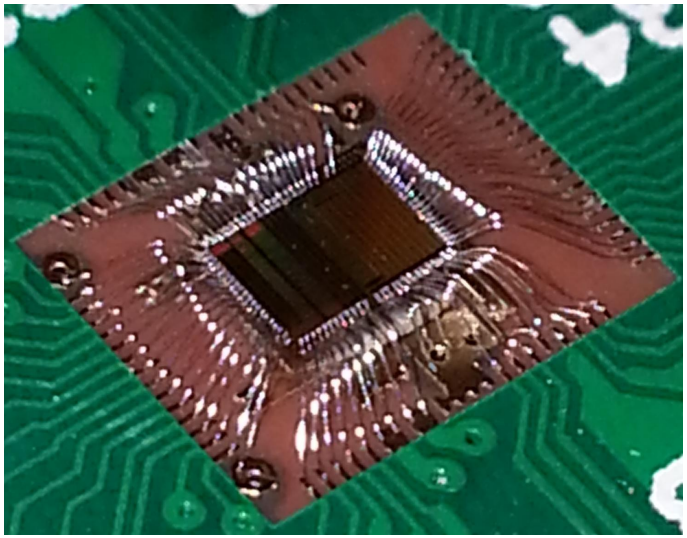


FLAME readout for ILC in CMOS 130 nm
8-channel FLAME ver.0 prototype





2600 µm x 2000 µm



8-channel FLAME v0 prototype:

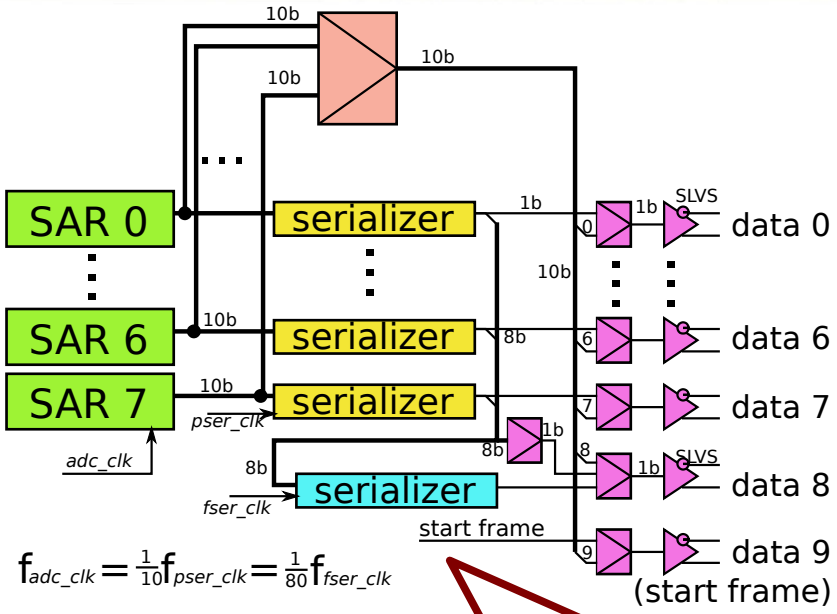
- 8 mix-mode channels (FE + ADC) with backend:
  - Front-end wit variable gain, CR-RC 50ns shaping
  - 10-bit SAR ADC sampling up to ~40MSps
  - 8 parallel data links (one per channel)

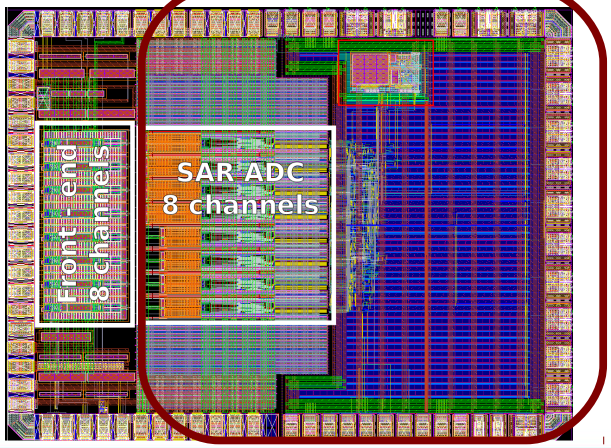
Fabricated in 2016

FLAME ver.0 Mixed-Mode and Digital part

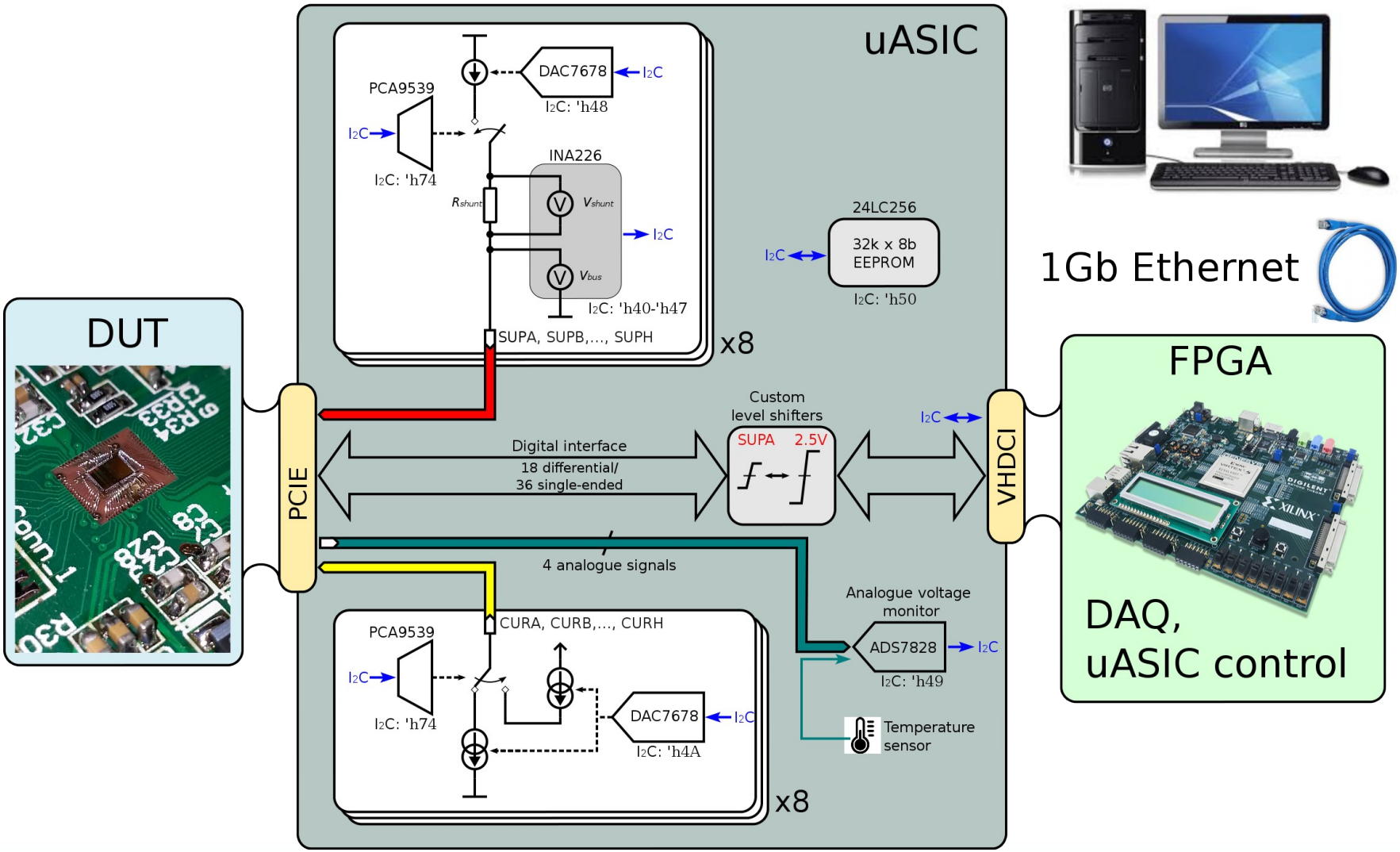
Specifications & main features:

- Technology TSMC CMOS 130 nm
- 8 channels of 10-bit SAR ADC
- Multimode multiplexer/serializer:
  - Single ADC mode: single channnel output
  - Parallel mode: one output per channel (10-bit serialization with faster clock)
  - Serial mode: one output per all channels (double serialization: 10-bit x 8 channels)
- Additional test modes, with counters/pseudo-random data instead of ADC output, to verify serialization/transmission
- PLL for data serialization
- High speed SLVS interface (>1GHz)
- Power pulsing





Testing complex chips
Test setup for FLAME



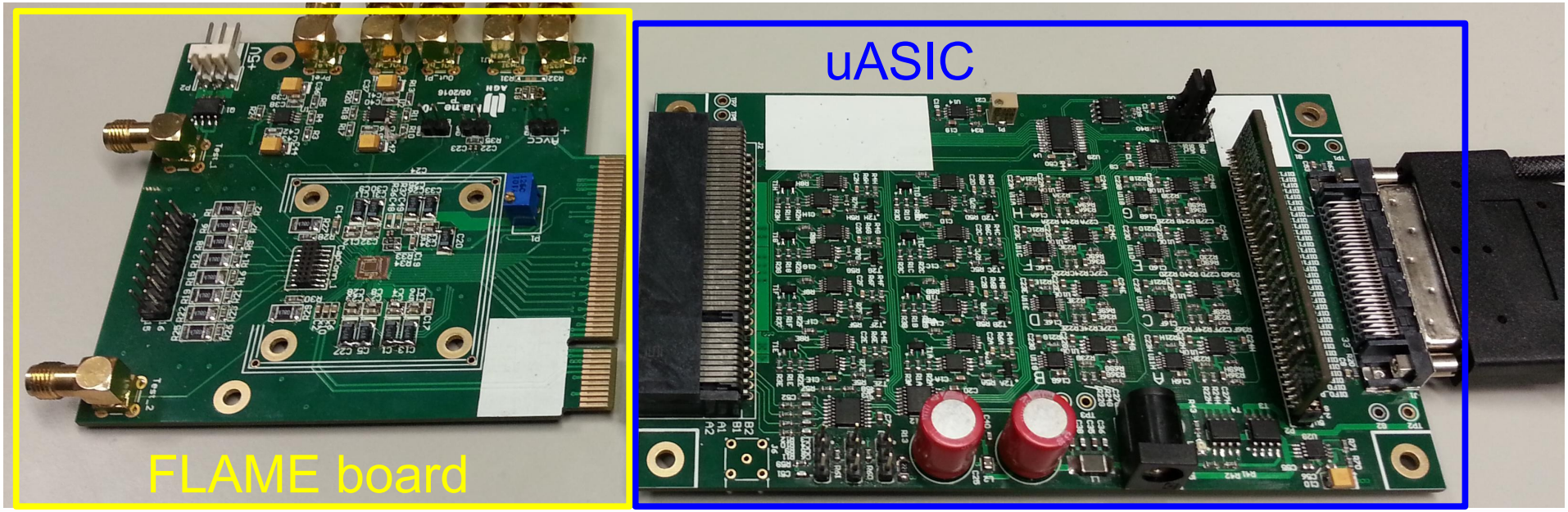
Testing complex chips
Test setup for FLAME...

uASIC board comprises:

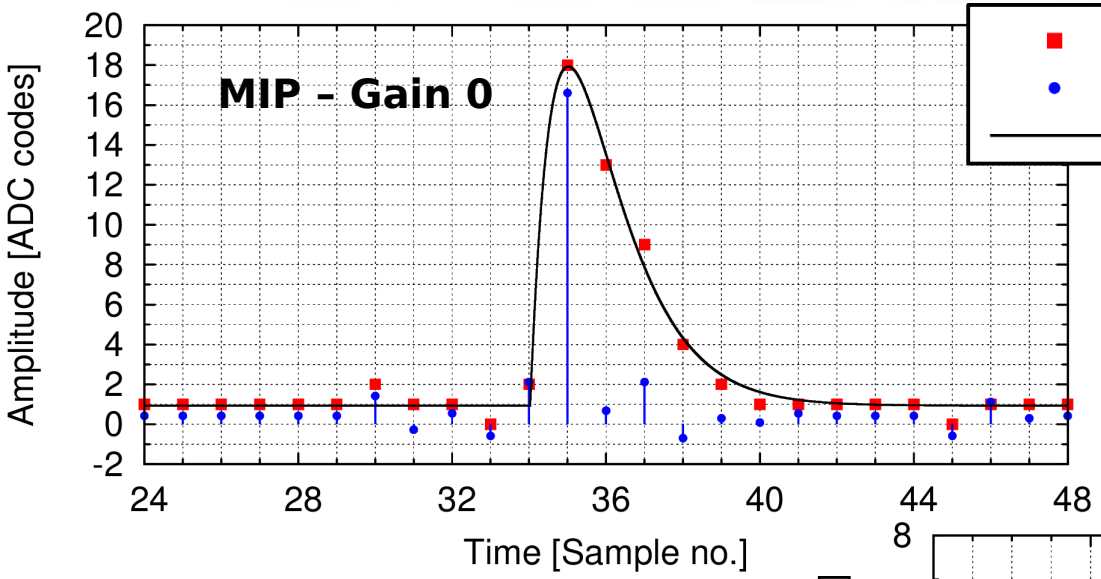
- 8 adjustable voltage sources with precise power consumption measurements
- 8 adjustable current sources
- 18 fast, differential data links between DAQ and ASIC
- Some additional features...

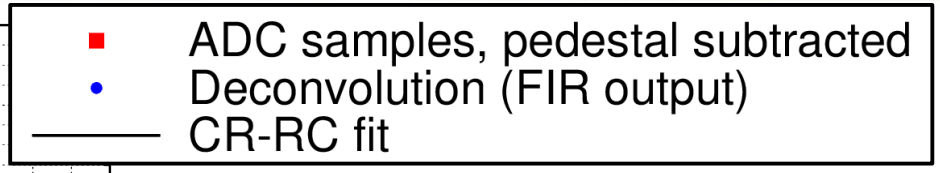
uASIC board advantages:

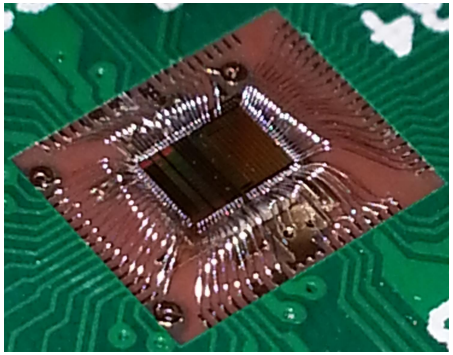
- DUT board can be very simple, cheap, easily assembled and replaced
- The same uASIC board can be used to test many different ASICs
- DAQ and slow control software and firmware can be unified

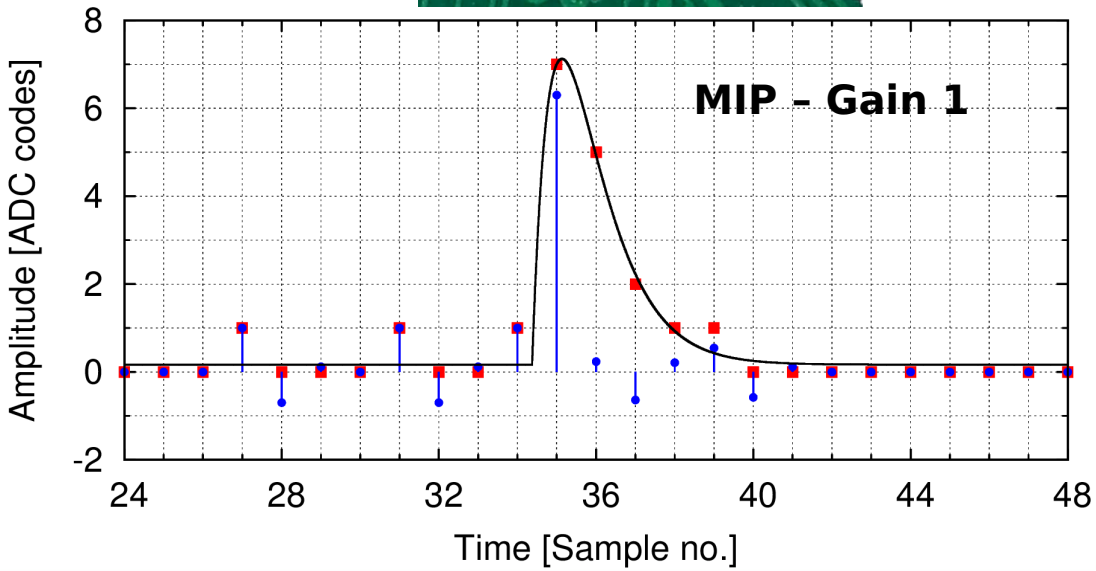


FLAME ver.0
First measurements





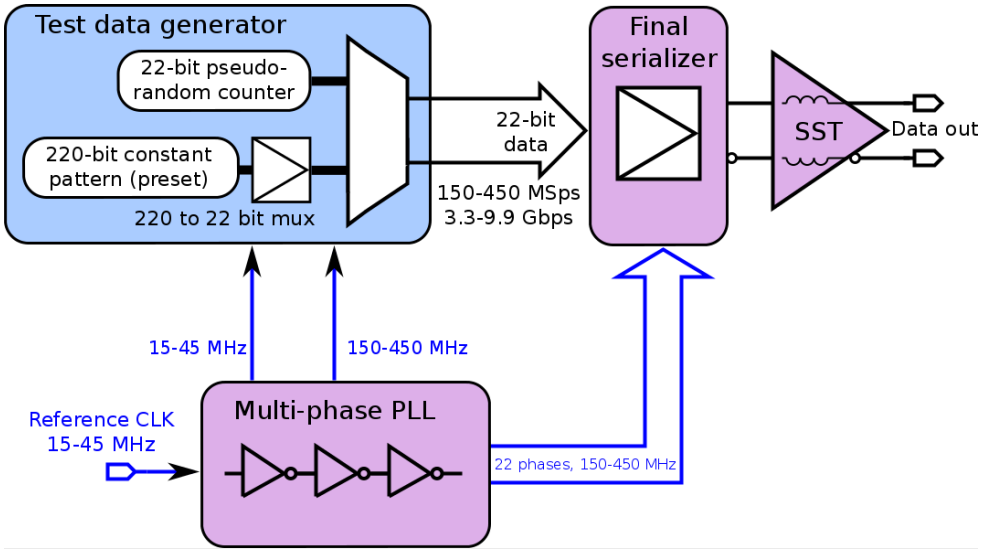


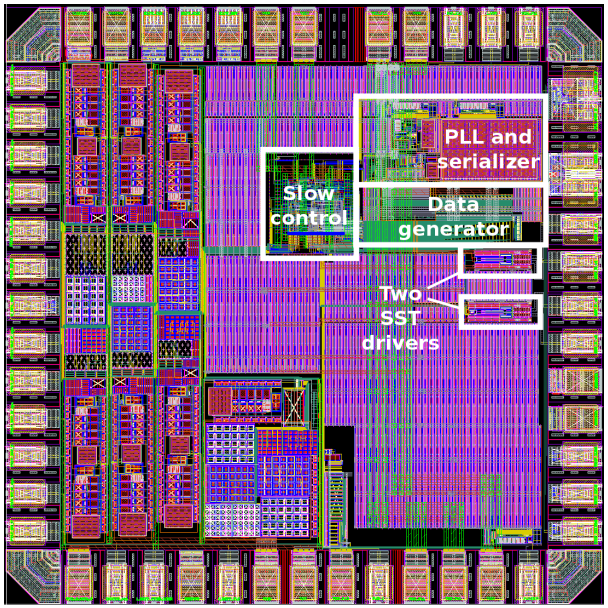


Exemplary FLAME v0 pulses

- MIP well visible with calibration and testbeam gains
- Low pedestal variations
- Tests in progress...

High Speed Serializer&Transmitter prototype in TSMC CMOS 130nm



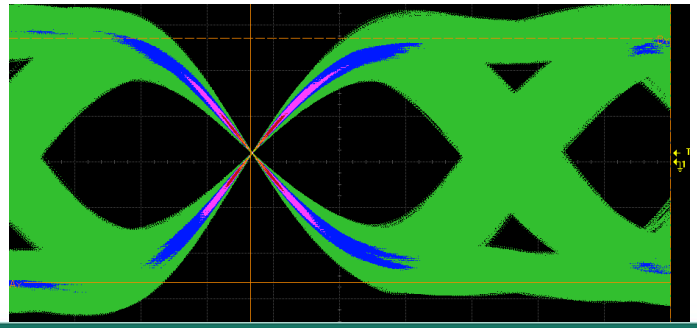


1250 µm x 1250 µm

FLAME serializer prototype:

- Ultra low power, low jitter multi-phase PLL
- 22b → 1b serializer with fast SST driver (3.3 – 9.9 Gbps)
- Test data generator

Eye diagram at 5Gbps



Test setup to measure quantitatively data transmission (BER) not yet ready, but we are close...

Developments in TSMC 65 nm

Because of production of SALT ASIC for LHCb Upgrade, significant delay was accumulated..., nevertheless:

- Design of ultra-low power SAR 10-bit and 12-bit ADCs s in advanced stage
- Design of PLL for data serialization has been started
- Design of monitoring ADC for LpGBT (10-or 12-bit SAR + Single-to-Diff conv. + Reference generation) in progress
- We plan the submission in ~2 months

Summary

- In TSMC CMOS 130 nm we have very good or promising results for data converters and transmission blocks, some of them still waiting for tests (man-power...)
- In TSMC CMOS 65 nm first submission with ADCs and simple serializer planned within ~2 months.

Thank you for attention