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SI LAB Silizium Labor Bonn

TSV developments at U Bonn

WP 4 Session

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U Bonn Group

AIDA 2020

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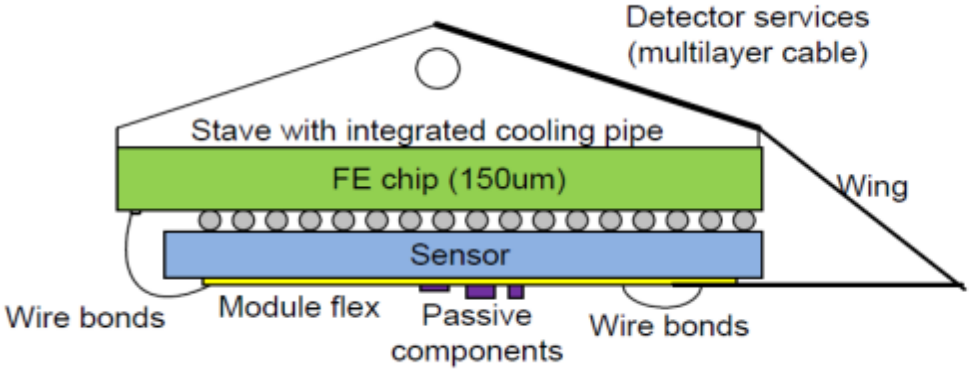
Bonn/CPPM TSV project

- The goal of the project is to develop modules for ATLAS pixel detector at the HL-LHC using a via last TSV process
  - Post-processing technology applicable on existing FE electronics
  - Dead area at the chip periphery can be reduced

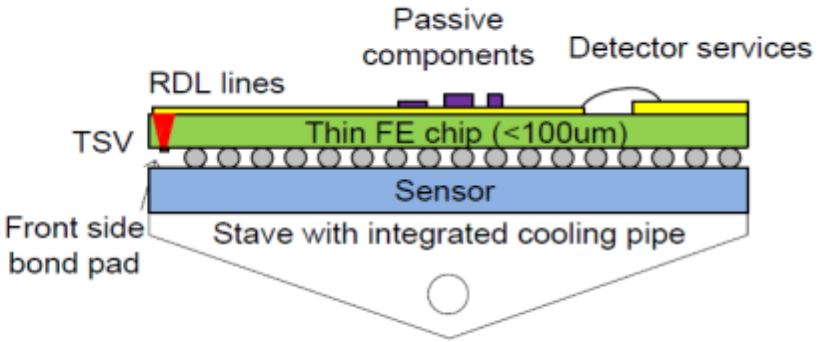
  → Compact, low mass hybrid pixel modules with minimal modification to the FE layout and using standard CMOS technology
  → no wire bonds needed if combined with new fley hybrid interconnection methods
  → Potential for 4 side abuttable modules using dedicated sensor layout

- Modules with TSV can be used for the outermost detector layers at the HL-LHC to provide full detector coverage over the large area

ATLAS IBL module



Example of TSV module

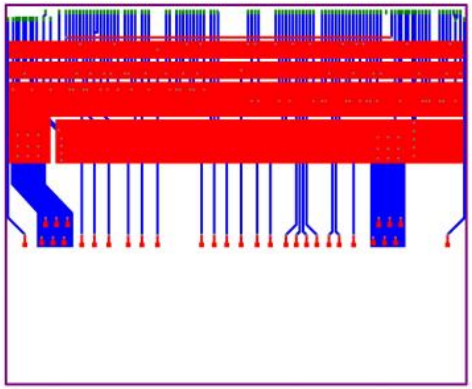


ATLAS FE-I4 TSV Run

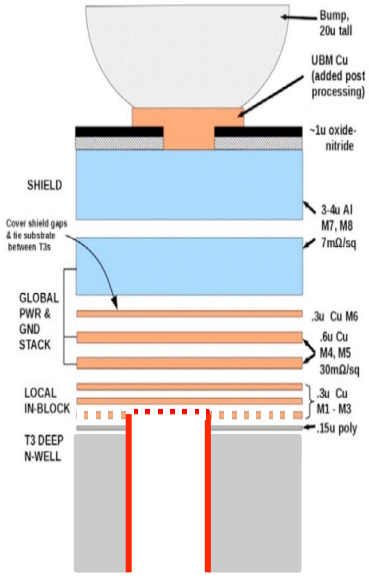
TSV modules using FE-I4 (ATLAS IBL chip): 160µm thick, 2 x 2 cm^2

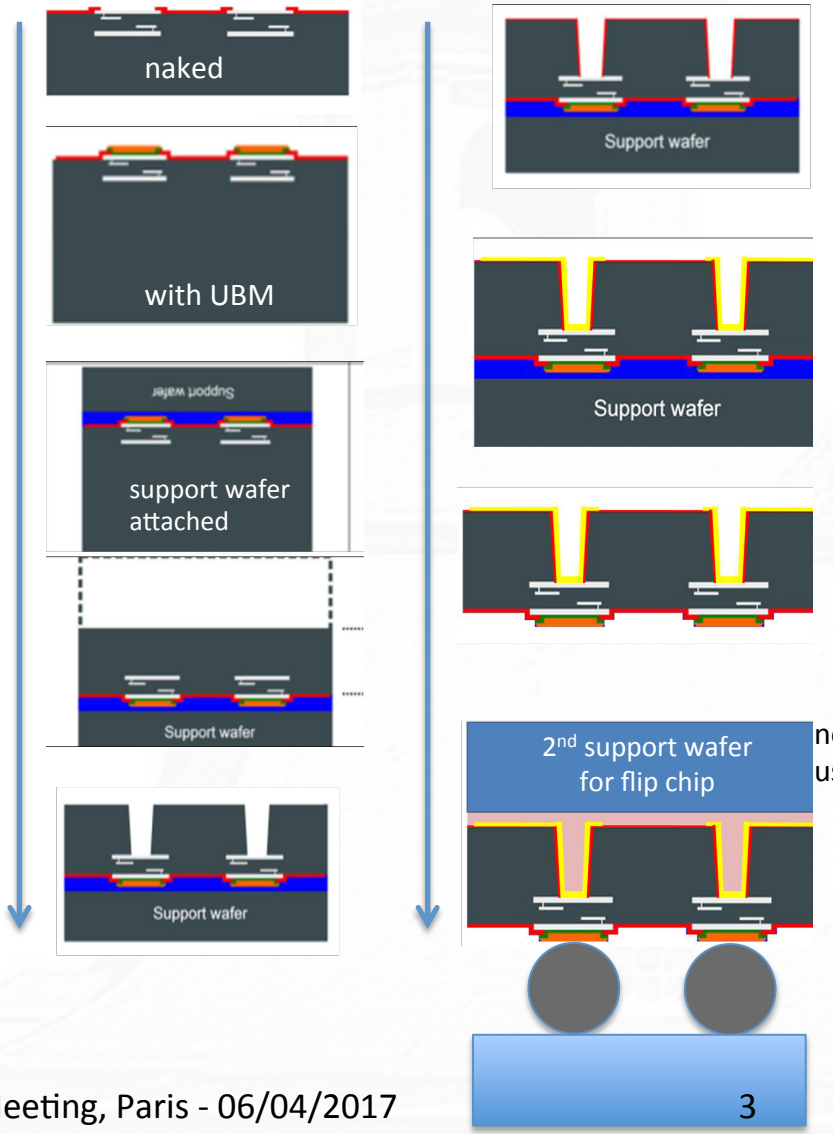
- use straight vias with aspect **ratio 3.5 : 1**

Goal: demonstration of **TSV/RDL processing together with solder bump bonding method** on 8" FE-I4 wafers thinned to 160µm (3 wafer pilot run)

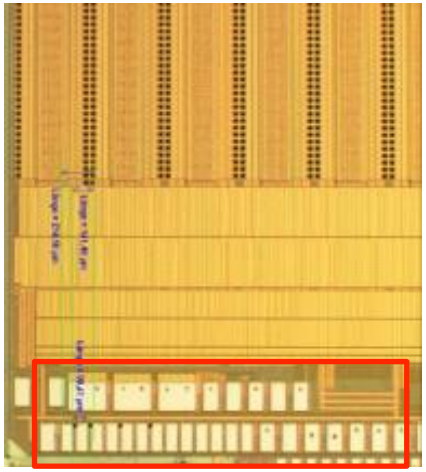


2-layer RDL

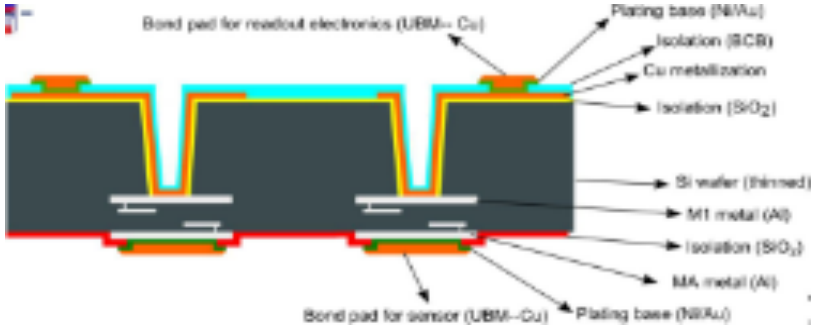




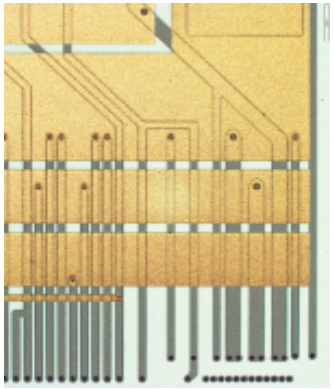
ATLAS FE-I4 TSV Run: Status

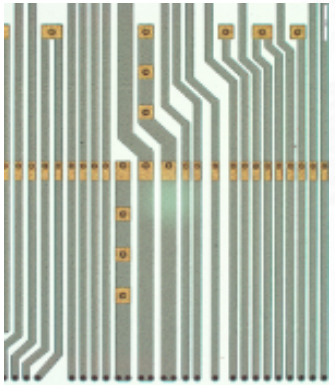


- Wire bond pad area for TSV contact
- Via from backside
- Liner filled TSV

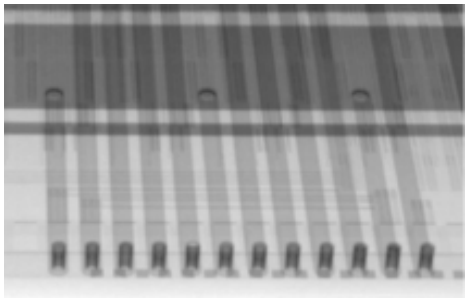


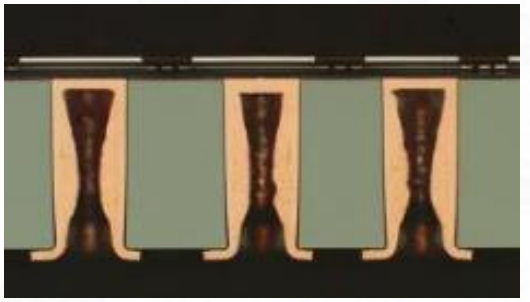
TSV schematical cross section





Two designs of Backside RDL and pad metallisation





ATLAS FE-I4B with Cu-filled TSV (x-ray and cross section)

- UBM on ATLAS FE-I4 wafer
- TSV formation on ATLAS FE-I4 wafer
- Functional test of ATLAS TSV chips
- Samples for module assembly available?

All pictures courtesy of Fraunhofer IZM, Berlin.

ATLAS FE-I4 TSV Run: Results

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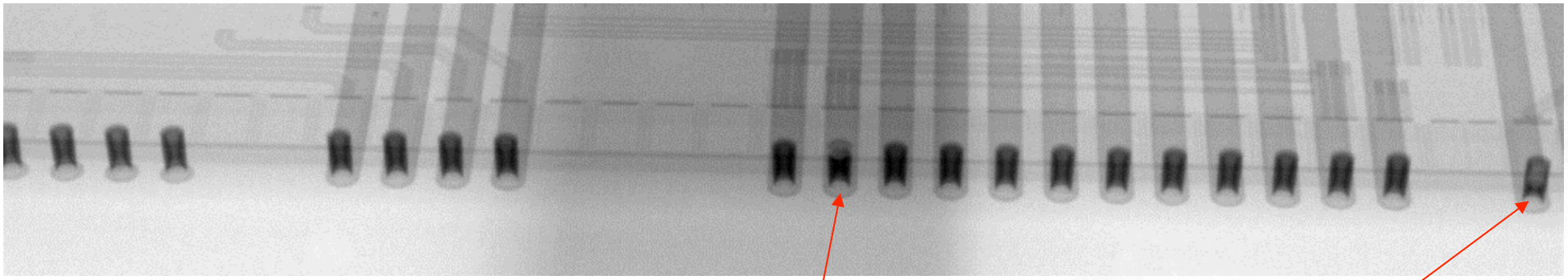
X-Ray Check of Via Filling:

- Easy non-destructive method to check the filling result
- High resolution x-ray necessary
- Wafer can be stored in sealed envelope
- Full wafer inspection time consuming and not 100% clear

ATLAS FE-I4 Chip: TSV x-ray check, RDL side down



TSV not completely filled, void at via bottom

TSV with poor side wall metallization but connected to M1

Picture courtesy of Fraunhofer IZM, Berlin.

ATLAS FE-I4 TSV Run: Results

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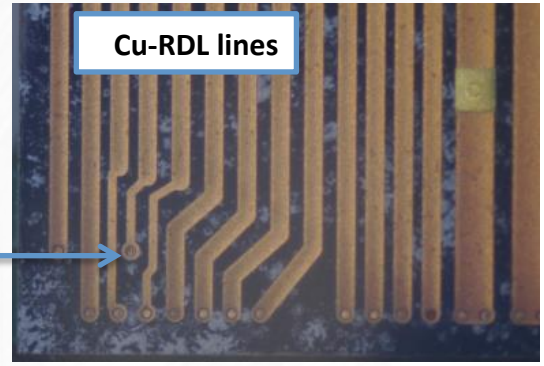
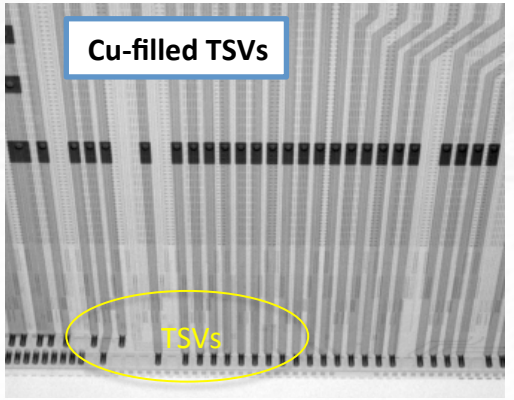
TSV modules using FE-I4 (ATLAS IBL chip): **160µm** thick, **2 x 2 cm²**

- use straight vias with aspect ratio **3.5 : 1**



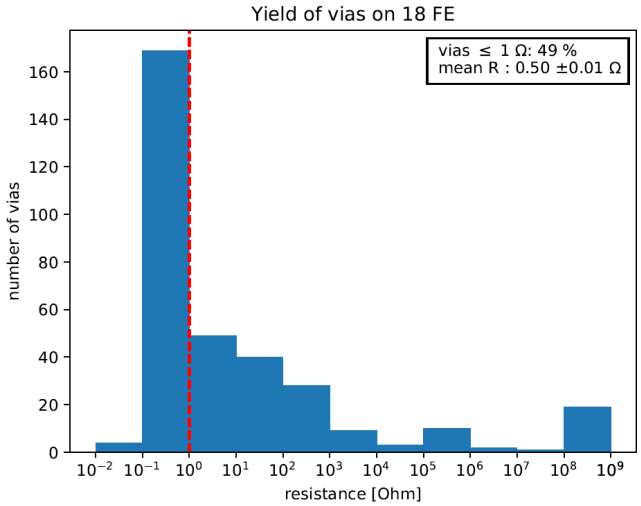
Visual inspection:

- good round RDL layer edges (Cu and NiAu) and clear cut vias
- X-ray image shows good metal coverage over full TSV depth



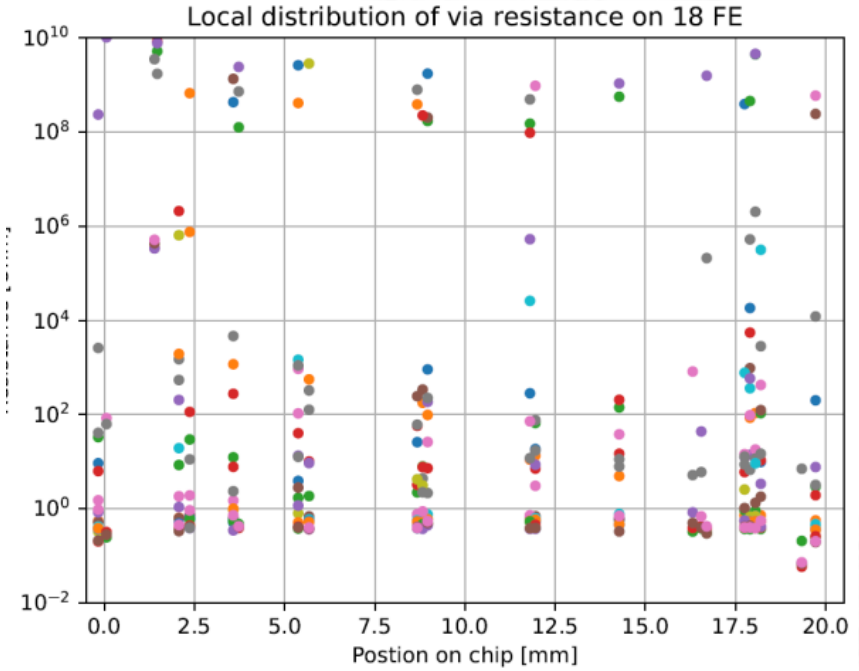
Electrical tests:

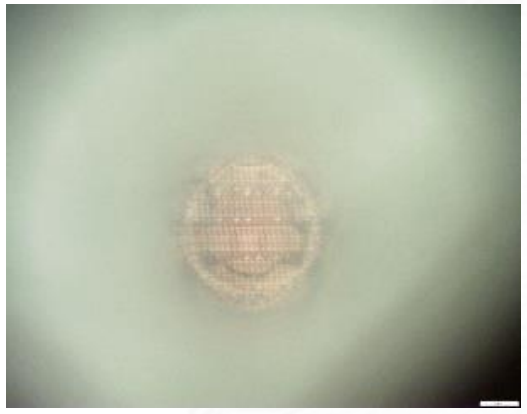
- yield needs improvement
- aspect ratio still challenging

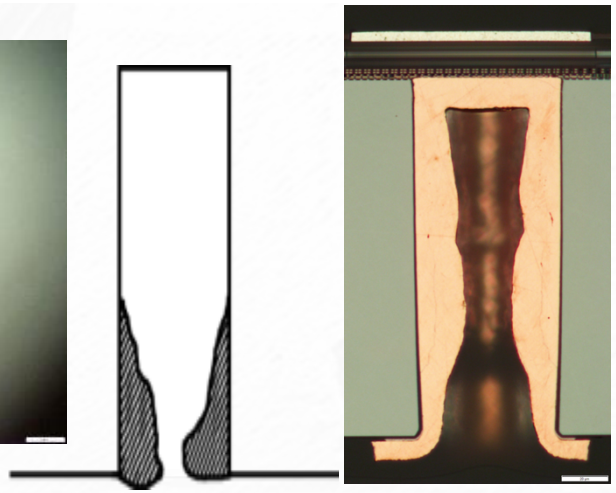


TSV Resistance measured on 18 FE chips

- Mean via resistance measured on FE-chips:
  - 18 modules tested
  - No correlation with TSV position on chip
  - All modules similar
- Mainly 2 effects caused the failures:
  - Insufficient copper plating due to rework
    - faulty sputtering of seed layer
    - no copper at via bottom
  - Incomplete Via etching
    - controlled optical
    - layer M1 is meshed
    - passivation layer beneath M1 needs to be etched through completely







PoC project: Advanced Through Silicon Vias for Pixel Detectors

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- **Goal:** establish high yield TSV + RDL process for pixel modules
- straight vias through (ultra?) thinned FE-I4 wafers and chips: note **2x2 cm^2 chip size**
- **80 – 120 µm** thickness (to be optimized),
- aspect ratio = 2 : 1
- one handle wafer step needed
- complete development including flip-chipping process for the final pixel module

Challenges of the project

- reliable TSV fabrication ... yield hoped/expected to be much better than for project 2
- thin (o(100 µm)) wafers are needed for the goal of "large yield"
  challenge is the handling of large and very thin wafers/chips
- surprises during flip-chipping can also be an issue

TSV Formation – Process Optimization

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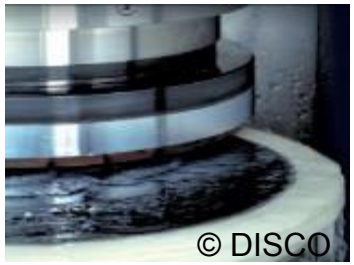
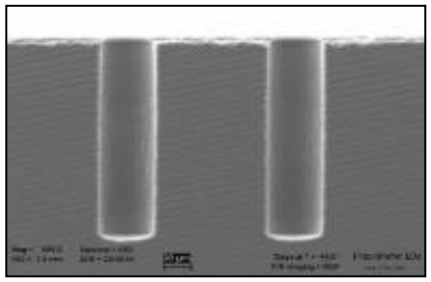
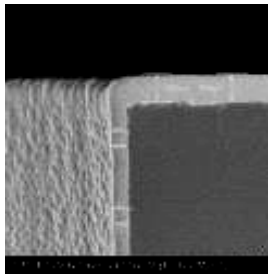
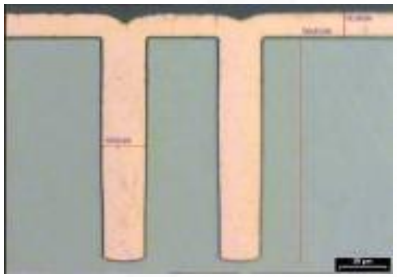
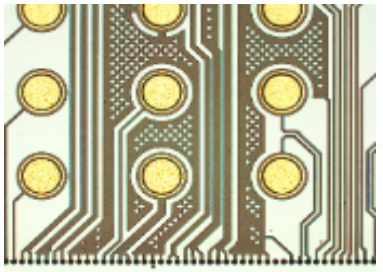
1. Wafer Thinning: Grinding, Wet Etching, DRIE
2. TSV Si-etching: DRIE BOSCH Process
3. TSV-Insulation: TEOS, PE-CVD, SA-CVD, Polymer
4. Adhesion-/Barrier-/Seed-Layer: Ti (TiW, TiN, Ta(N)) / Cu HI-PVD
5. Via filling: ECD Cu bottom up filling, liner filling
6. RDL / UBM pad metallization



All pictures courtesy of Fraunhofer IZM, Berlin.

TSV Project Implementation Plan

- WP1:
  - Process optimization for very thin (80-120 µm) readout wafers
- WP 2:
  - Design optimization of the TSV and RDL layers
- WP 3:
  - TSV run with optimized RDL design on FE-I4 wafer batch incl. electrical tests
- WP4:
  - Optimization of bumping and flip-chip using (ultra?) thin TSV chips to sensors
- WP 5:
  - Characterization of TSV chip sensor assemblies

ATLAS FE-I4 TSV Work Planning

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WP1 – Process Modifications/Optimization:

- Reduced wafer thickness: 160µm → 120…90µm:

  + better visibility of via bottom after TSV etch / oxide etch
  + improvement of TSV filling behaviour
  - higher risk of wafer breakage

- Fabrication of TSV Daisy Chain Testwafer with dedicated M1 setup layer:

  +/- setup of TSV etch process but without poly-Si layer
  - additional wafer fabrication (process steps)

- Test of backside carrier wafer process:

  + higher stability up to dicing process
  + stabilisation of FE-I4 chip during flip chip process
  - carrier release after flip chip assembly
  - more cleaning steps necessary

Conclusions

WP4 new interconnections techniques of hybrid pixel detectors:

- Continuation of our collaboration with IZM and CPPM for a via last TSV process on ATLAS Pixel FE wafer:
  - demonstrated with good results on FE-I2/3 assemblies
  - 1st Process with FE-I4 wafers → **some encouraging results although rework of TSV filling but overall yield is not satisfactory**
  - Next step: 2nd FE-I4 TSV run with optimized process parameters → **Goal is building full assemblies using complex RDL on chip backside.**
  - Funding received through PoC program of AIDA-2020
  - Long term plan: Move on with 65nm CMOS wafers from RD53
    - check feasibility → high capacity/inductivity of TSV could have impact on high speed links