University of Glasgow | Department of Physics & Astronomy

LAL Laboratoire de l'Accélérateur Linéaire

Max-Planck-Gesellschaft

cea leti

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CERN

TSV development with CEA Leti in the FEI4 chip

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Goal

- **WP4 (NA3) Micro-electronics and interconnections:**
  - *Task 4.4 Interconnections and TSVs.*
- Interconnection of 65 nm CMOS readout chips to silicon pixel sensors by using through-silicon vias (TSVs) across the substrate, full qualification and testing.
- Fine pitch bump bonding techniques will be qualified by this WP

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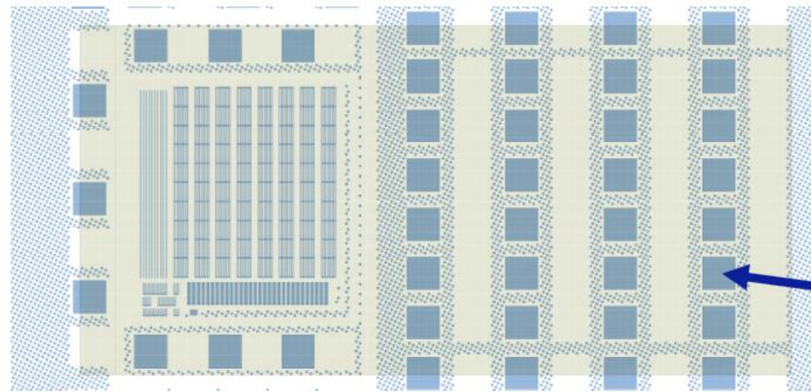
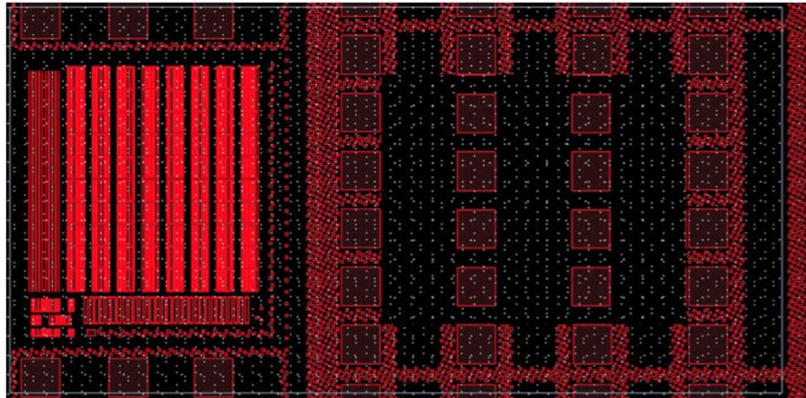
TSVs and RDLs with ATLAS FEI4 FE chips

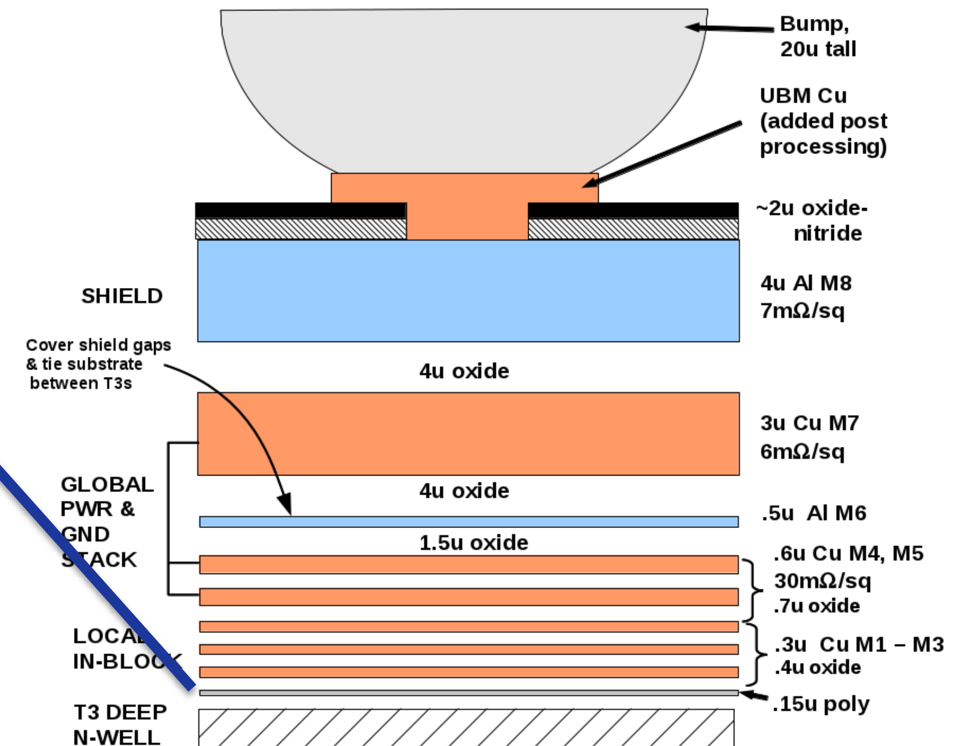
- Project started with CEA Leti on TSV-last process in FE-I4 chips
  - Connect chip M1 metal layer from front to back of chip via TSVs
- Front side processing with either UBM only or bumps
  - UBM only → solder on sensors
  - Bumps → UBM on sensor
- Back side processing RDL
  - Specific FE-i4 layout for laser soldering, same specs as Medipix
  - Pad layout to compensate thermal stressed during re-flow after flip-chip (demonstrated to work in previous project between Glasgow and LETI)

TSVs in FEI4

- Require access to M1 from the chip backside
- Re-spin of FEI4 wafers have reduced poly-Si to aid TSV etch
  - During MPI TSV project with EMFT understood that there was poly-Si under M1
  - Poly-Si causes issues with the TSV etch







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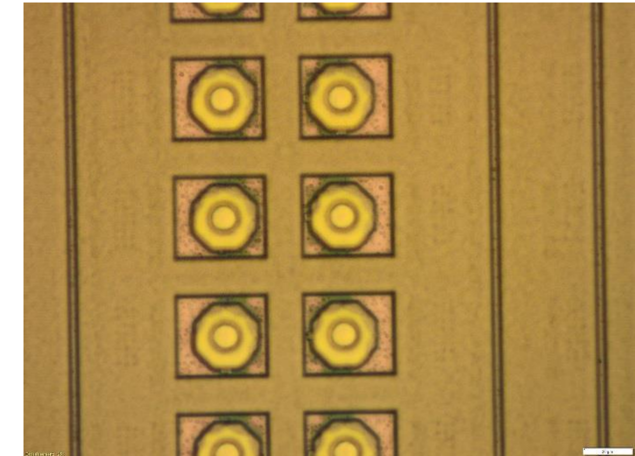
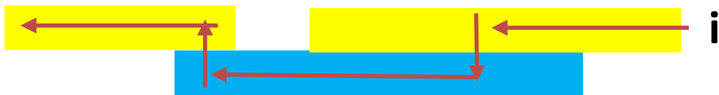
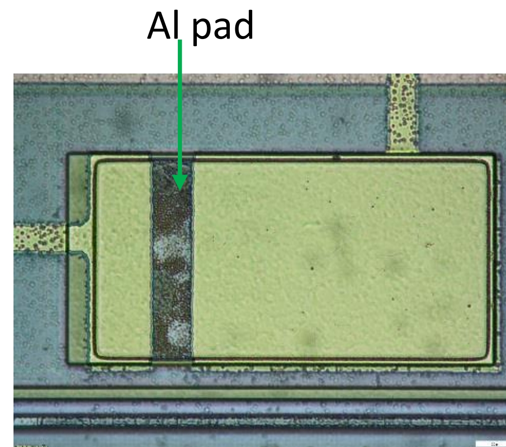
Front side UBM

- Electrical characterization
  - Results in line with expectation on UBM layer
    - Critical dimensions
    - Sheet resistance
    - Planar insulation
    - **Contact with Al pads**

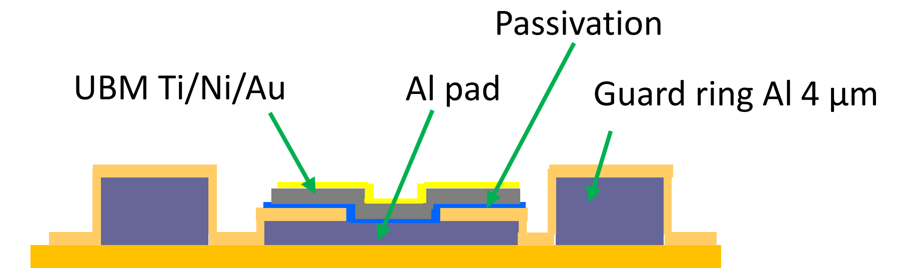


UBM pads – optical inspection





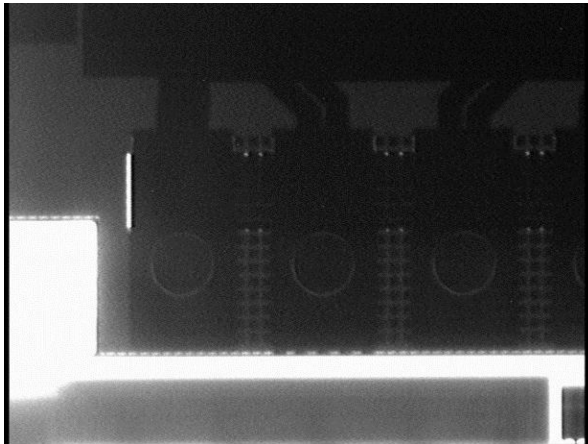
Contact structure on pad



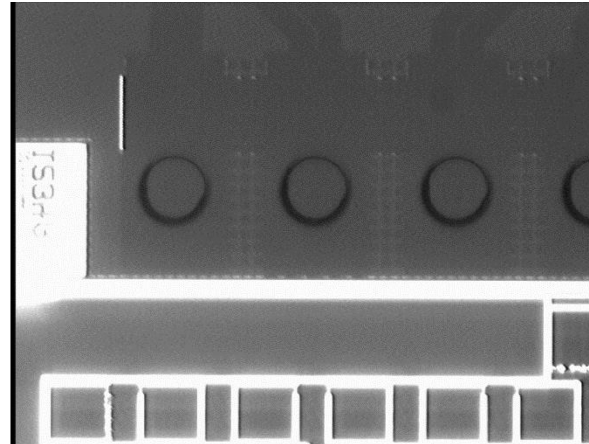
TSV last – Oxide etch mask

- IR image of Oxide DRIE mask
- Circles are mask
- Good alignment to M1

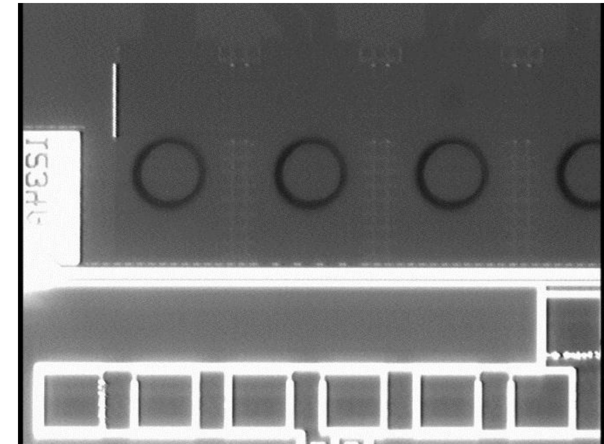
Wafer 01



Wafer 02

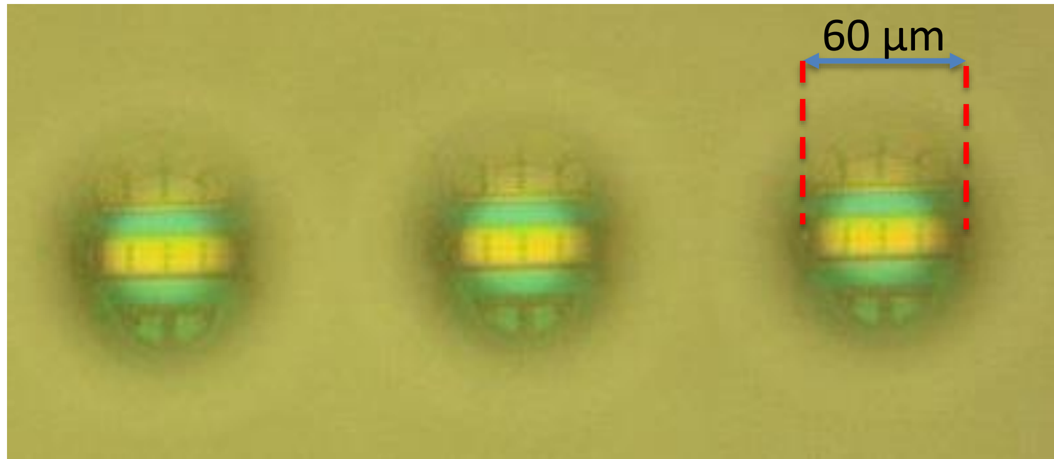


Wafer 03

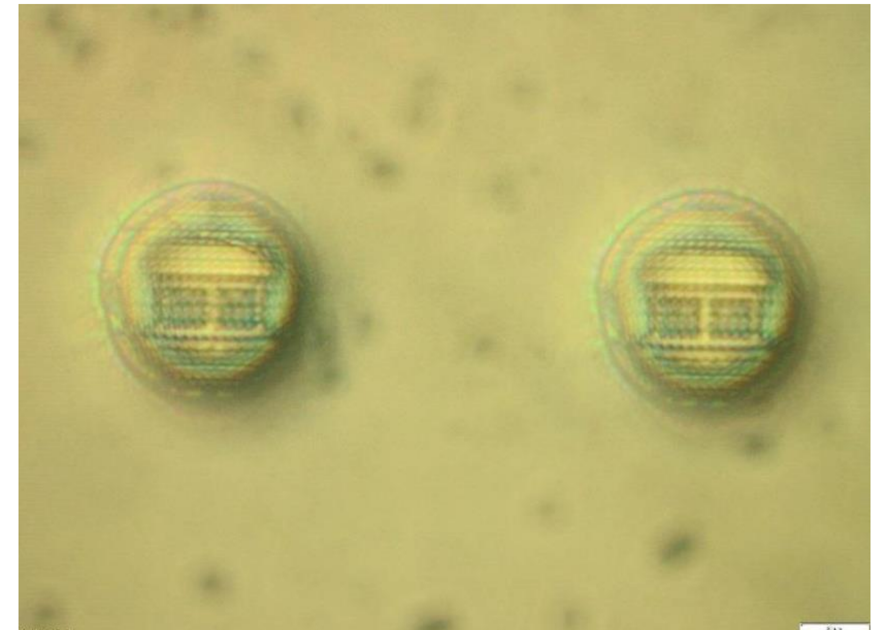


TSV etched through to the M1

- TSV etched through silicon down to M1



- TSV lined using full wafer Silicon Oxide & Silicon Nitride deposition
- Etch back full wafer to open the oxide/nitride on the bottom of the TSV
- Damascene process to fill with copper



- 3 µm oxide liner on inside of TSV walls
- All oxide removed at the bottom of the via

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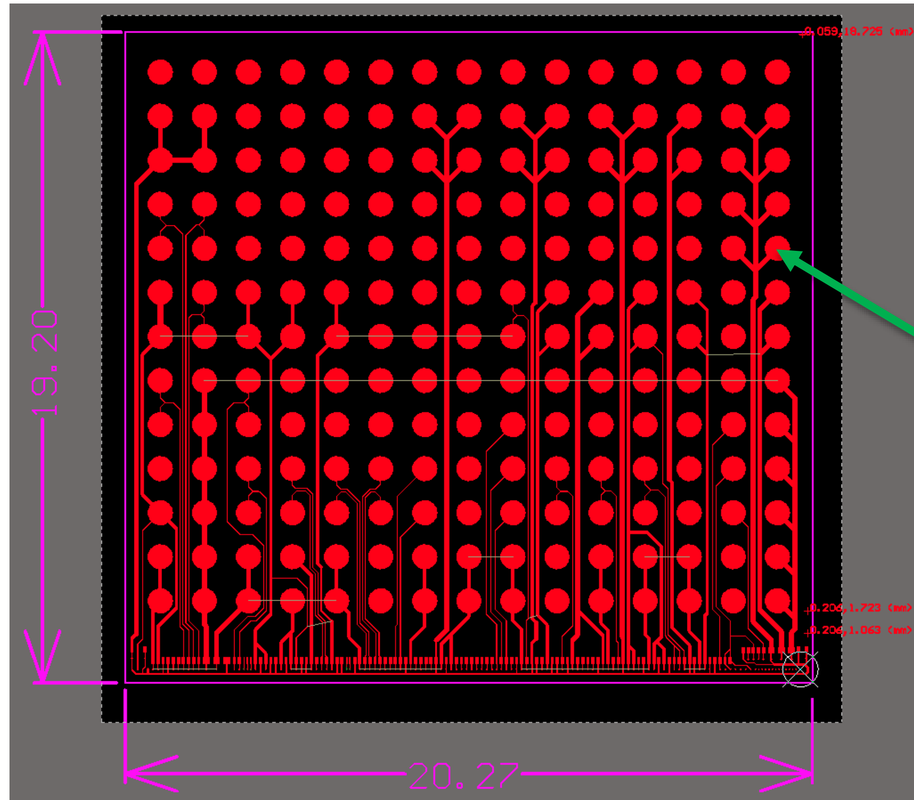
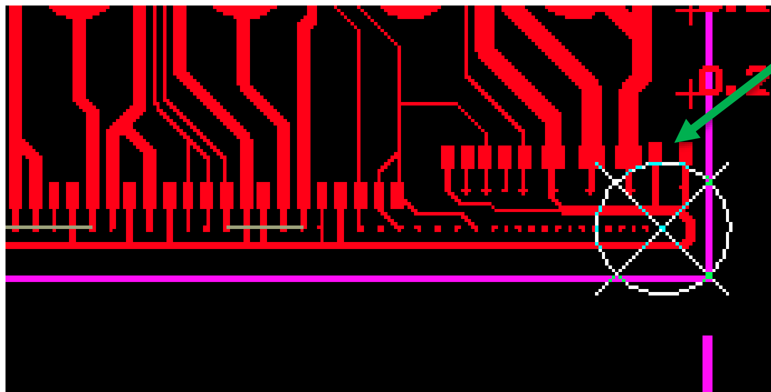
FEI4 ReDistribution Layer

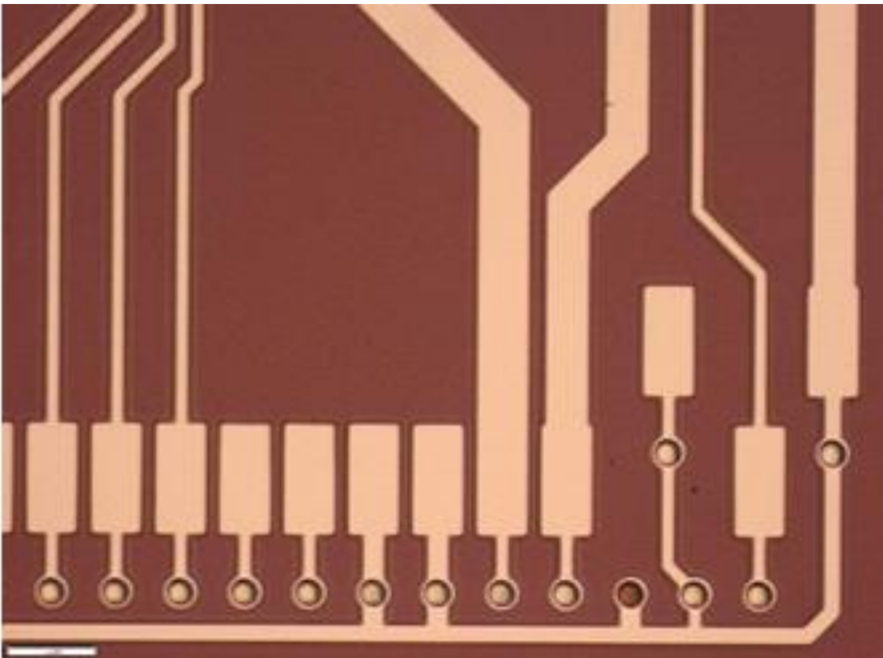


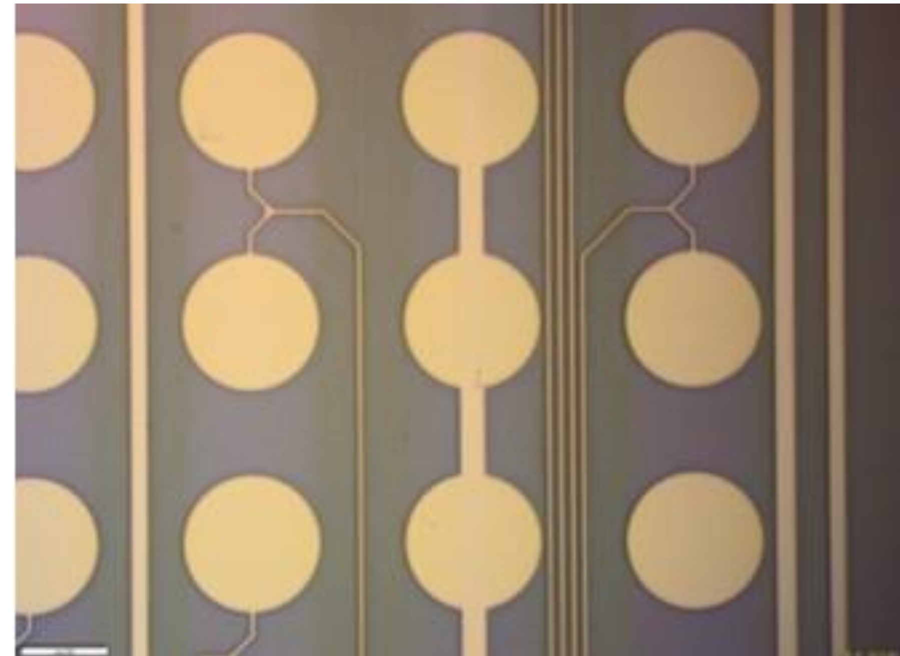


- RDL design for FE-i4B
  - Copper layer on back side of chips
  - Large solder pad array compatible with direct laser soldering
  - Solder pads over full chip to compensate thin die bow – eases flip-chip
  - Include probe pads/wire-bond pads near TSV to allow testing with mirrored test card after processing or wire-bonding after processing
  - Designed at CERN and reviewed by LETI and ATLAS module experts, mask processed at LETI
- RDL metal stack compatible with Bump Grid Array solder technology

Lithography for RDLs

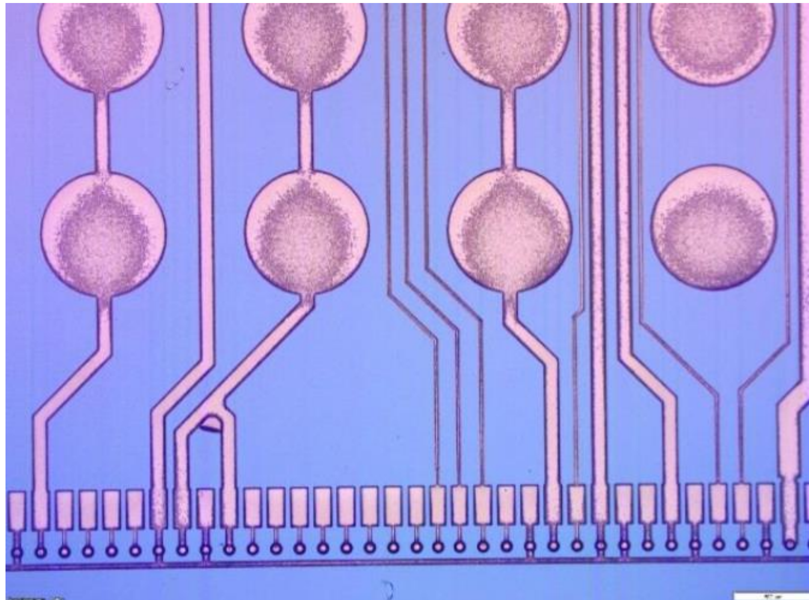
- Wafer is coated uniformly with a thin copper seed layer
- Resist is deposited and developed to realise the RDL pattern
- Electroplating of thick copper in the exposed RDL pattern
  - TSV filled during this stage
- Blank etch to remove thin seed layer

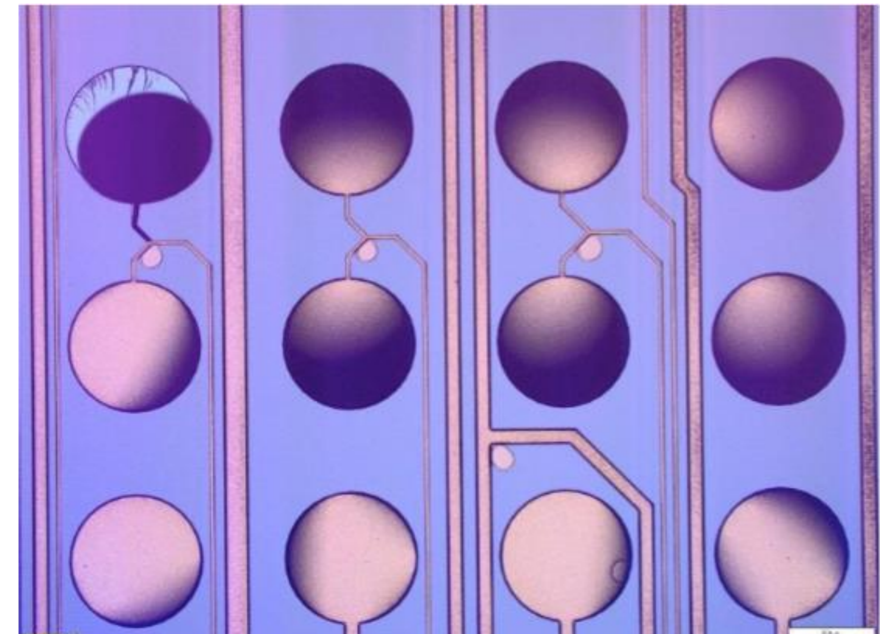




First RDL results

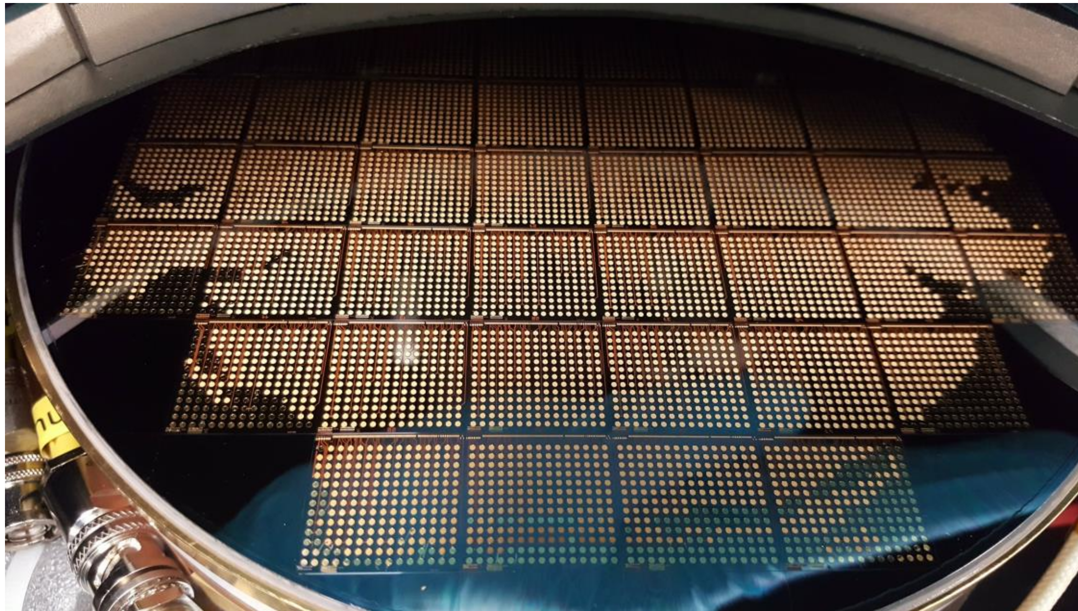
- Excessive copper applied
  - Aim was to reduce TSV resistance
  - 6-8 µm requested c.f. standard thickness < 5 µm
- Caused delamination of large RDL laser solder pads
  - Pulling away underlying oxide layer as well
  - 1 of the 3 wafers not so bad and useable for module building
- TSV contact on front side metal : low and repeatable contact between 2 ground TSVs
  - 6 Ohm including RDL line and probe resistance

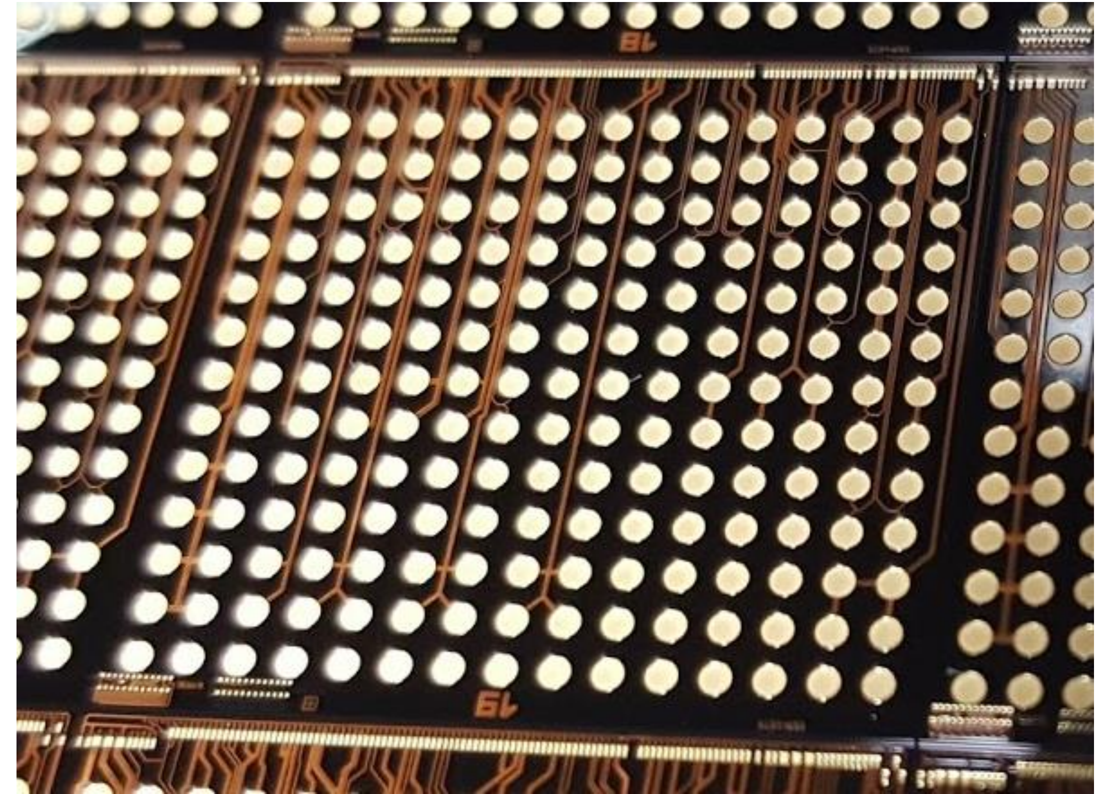




Frist Wafers

- 4 wafers started
  - 1 broke during processing
  - 2 had bad RDL delamination
  - 1 has good RDL in wafer central region





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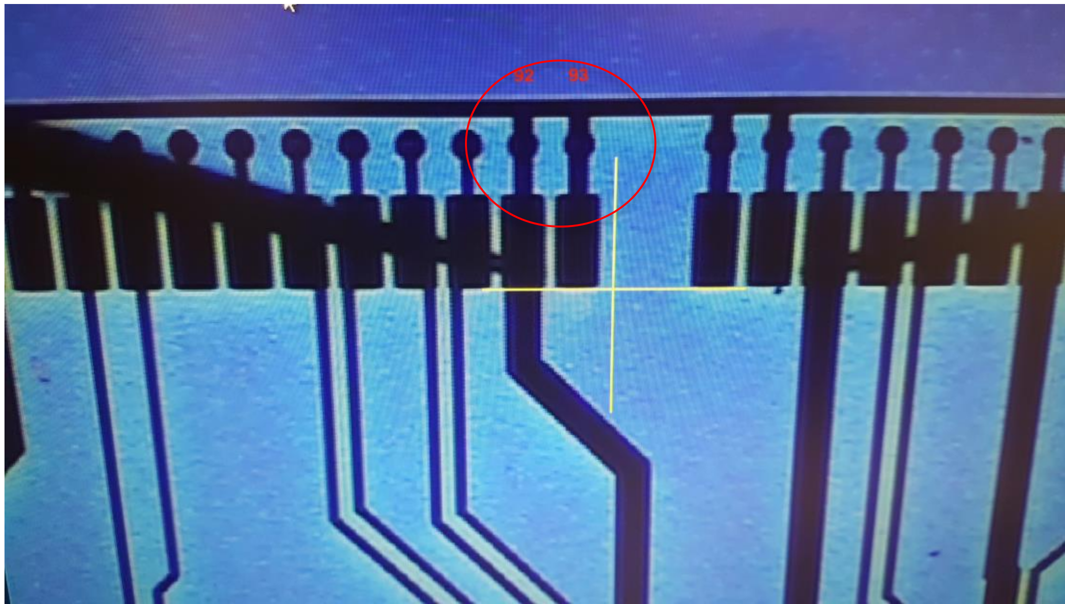
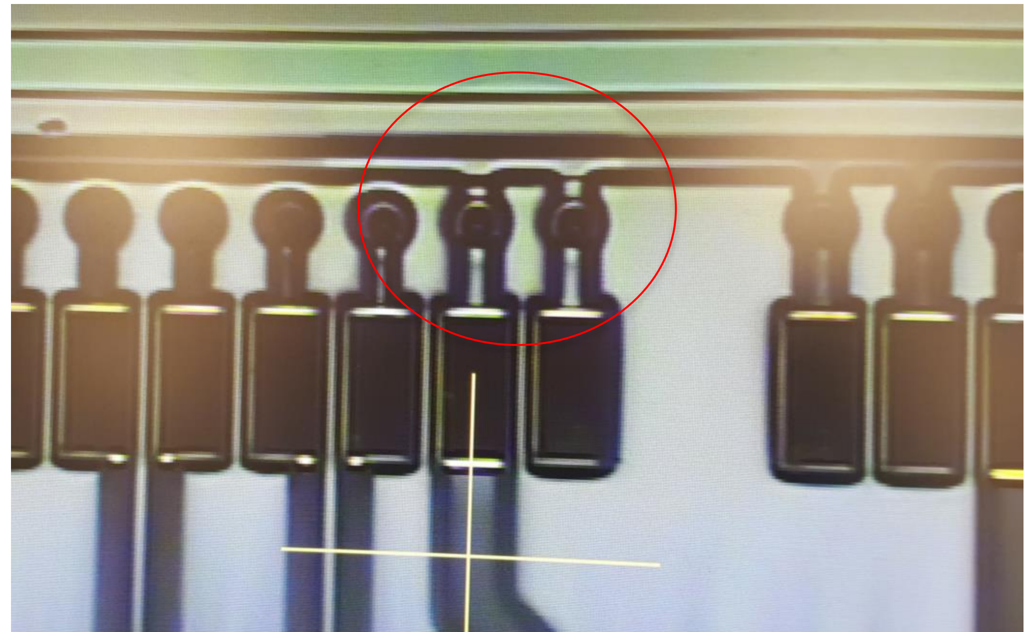
Frist wafer testing

- Wafer level testing started Jan 2017
- Soon realised that there was an RDL error

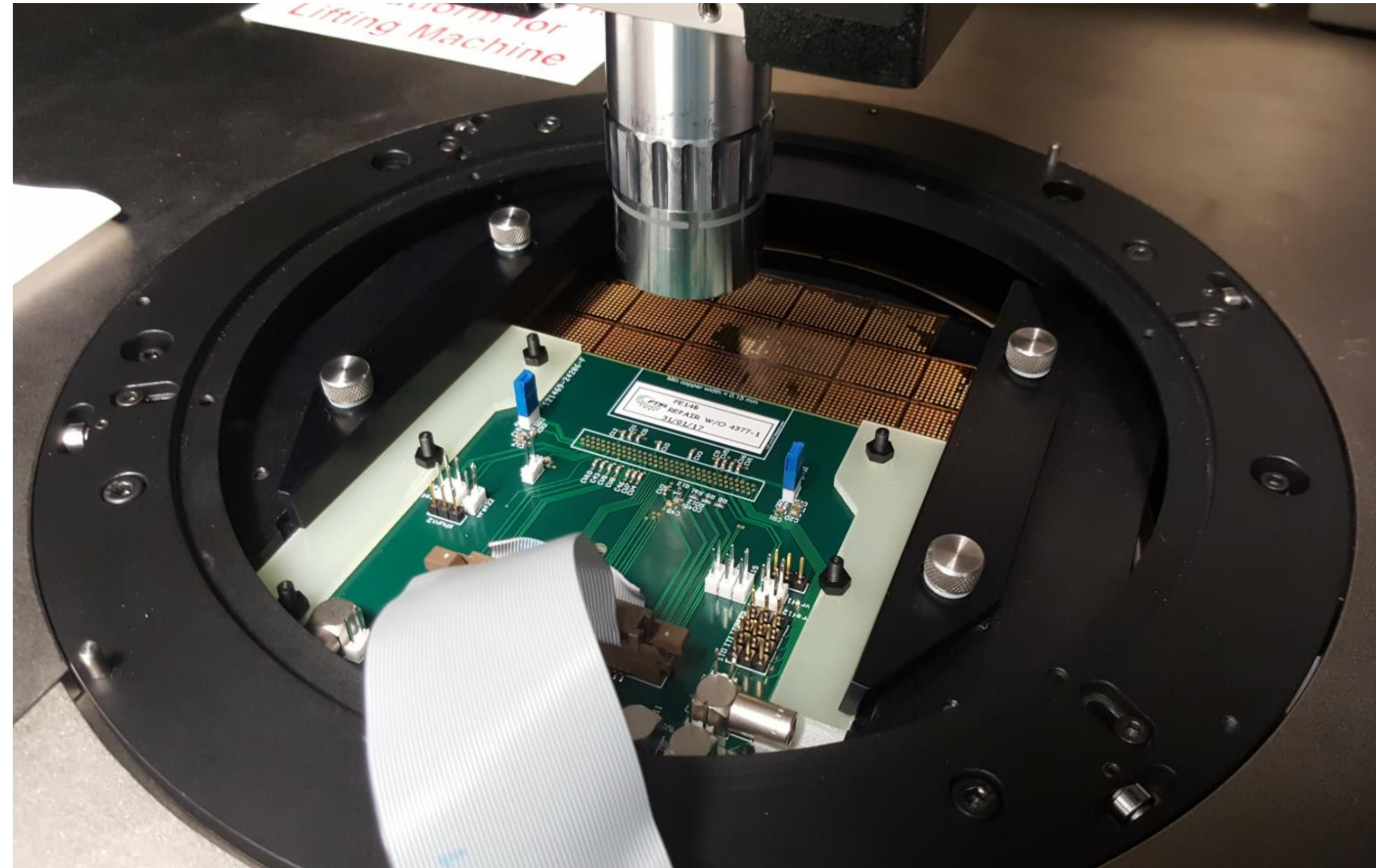


- VDDD line connected to GND bus
  - Error during translation of RDL design to wafer design software
  - Chip not testable
- Probed all power lines and currents reasonable
  - TSVs connected to M1 and isolated from wafer
- Wafers retuned to LETI for FIB
  - Only central die edited due to FIB reach
  - Error corrected
  - Tested on probe – no shorts!



Post TSV testing

- Wafer level chip testing
  - On probe station
  - Arrived yesterday
  - Electrical contact to chip via TSV, probe on mirrored pad array



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Next steps

- Poor wafers from first run will be diced and used for flip-chip and soldering trails
- Second run of wafers being processed at CEA LETI
  - Front side with Solder bumps
  - Front side processing finished
    - Bumps inspected and appear perfect
  - Ready for transfer to support wafer for backside processing
- Aluminum flex PCB for laser soldering
  - Designed
  - Soldering trails with dummy parts taking place
    - Using Medipix scrap parts
- Flip-chip to sensor to take place after bare chip testing
  - Sensors with solder bumps ready at Advacam

Summary

- TSV and laser solder module concept worked out
- CEA LETI TSV process well demonstrated on Medipix chip set
- FEI4 chip set modified to aid TSV formation
- TSV + RDL designed and processed
  - Contact to M1 and low electrical resistance
- Wafer probing (re-)started
- Testing and laser solder processes understood

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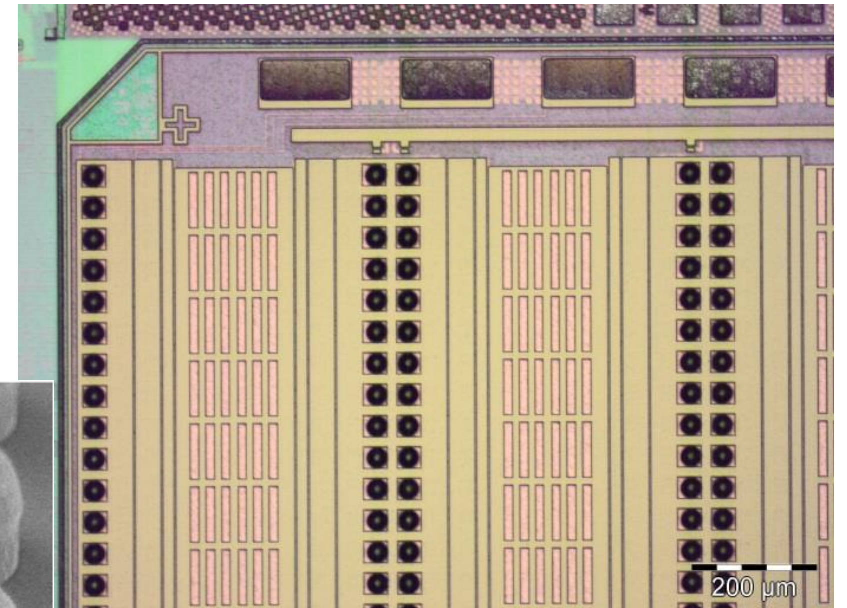
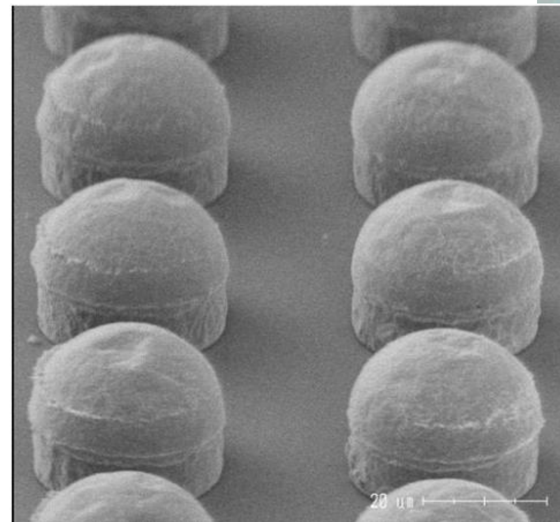
Backup

Bump deposition at CEA LETI

- Developed process for SnAg solder capped copper pillars on FEI4 200 mm wafers
  - Minimum pitch 50 µm in one direction
  - 10µm Cu & 8µm SnAg solder cap
  - Electro-chemical deposition of bumps on seed layer



- High yield (<99%) obtained after significant effort on process
- Future work to transfer this to 300 mm wafer line for RD53 pixel chip



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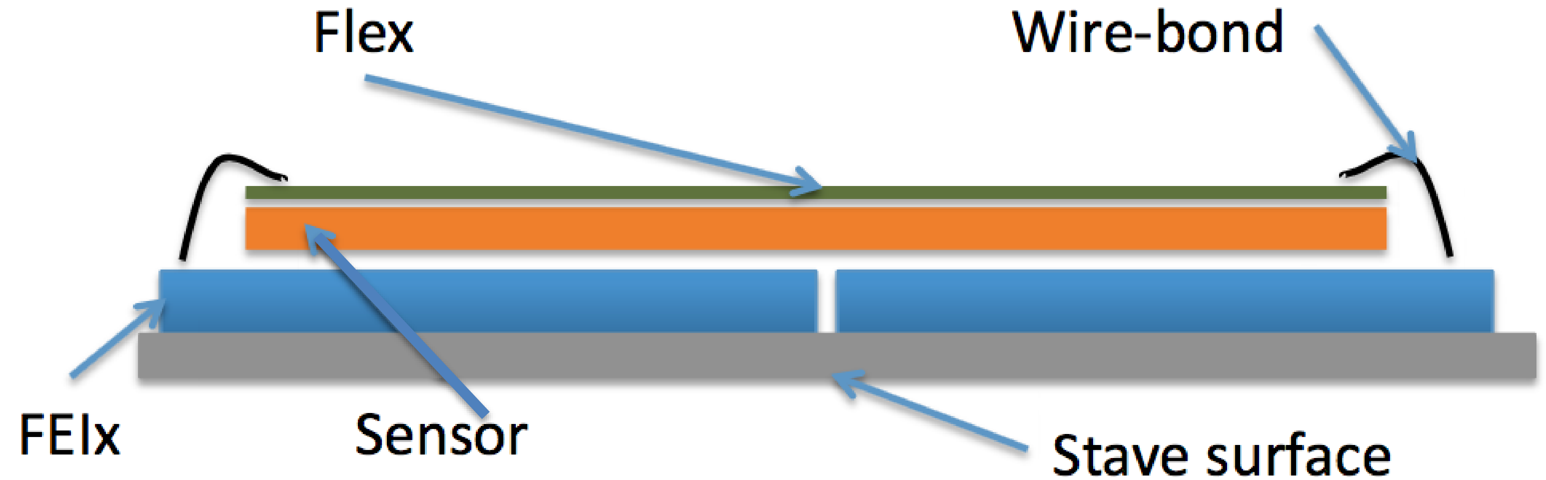
RD53 chip preparation

- Process will be different on RD53 wafers
  - Difference in tool set on 200 mm and 300 mm wafer lines
  - 50 μm pitch in both x & y direction
  - Difference in chip surface topology
- Building a test wafer for bump deposition and wafer handling tests
  - Presently obtaining quotes
- Daisy chain feature to measure bump and flip-chip yield
- Allows:
  - Early access to 300 mm wafer bump deposition experience
  - 300 mm wafer handling, thinning and dicing
  - Use of automated visual inspection tool
  - Flip-chip practice on large high density arrays

Hybrid pixel modules

- Hybrid pixel are:



Inherent limitations

- Wire bonds connect FE to flex:
  - Oscillation in magnetic field
  - Protection required or desired “To pot or not to pot”
  - Limit on envelopes
- Access to bond area on FE limits the sensor active area (not 4- side buttable)
- Requires expensive die-to-die assembly
- Wire bond Inductance limits signal speed
- Edge access -> power distribution over large chip challenging

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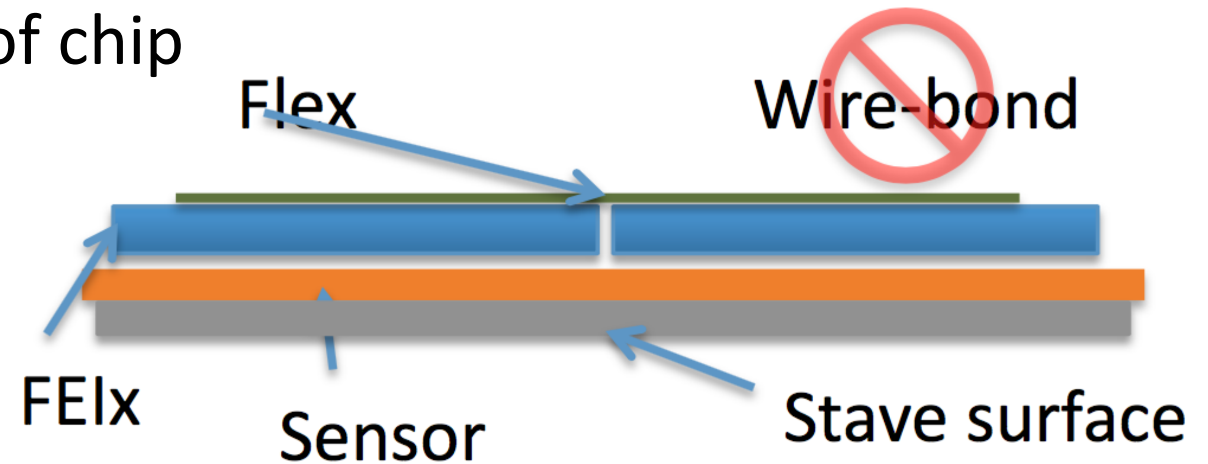
TSV module concept

- Using a TSV last process
  - Use existing chip set with post-processing technology
  - Build on Medipix experience with CEA Leti
- Remove wire bonds from the module
  - Connect flex via solder balls on back of chip
  - Less fragile module
  - Reduced interconnect inductance
- Remove wire bond pads
  - Reduced chip edge
- Compact, low mass hybrid pixel modules with minimal modification to the FE layout and using standard CMOS technology



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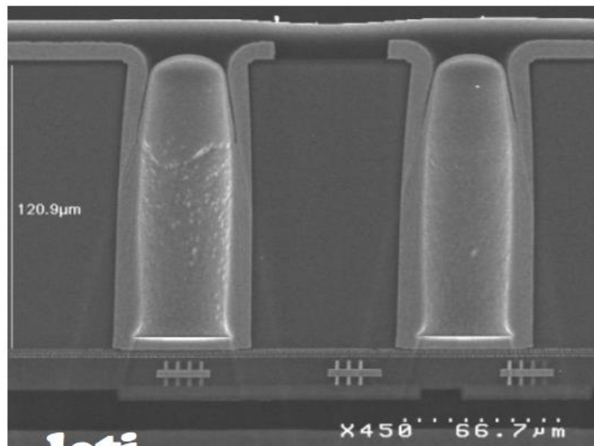
Wirebond less TSV enabling technologies

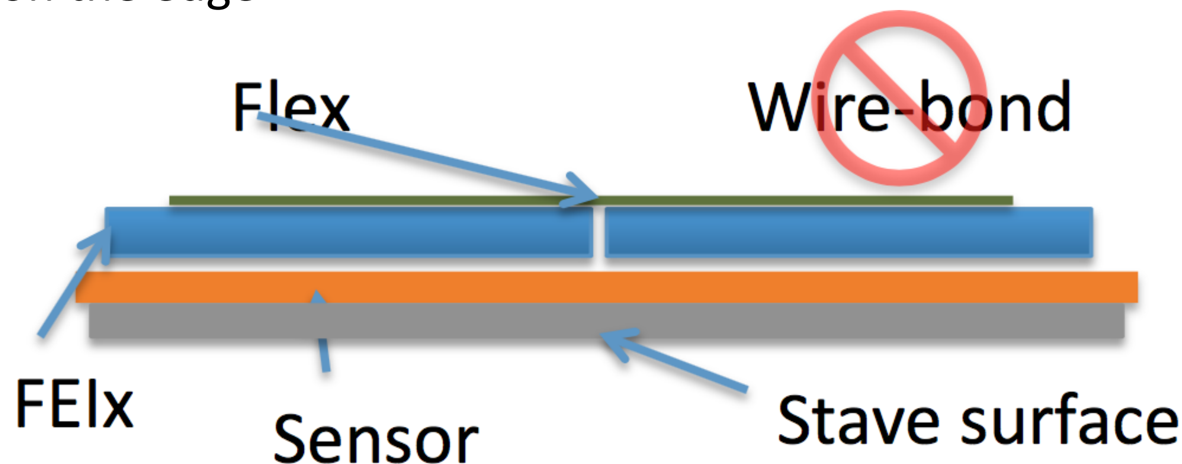
TSV-last + RDL

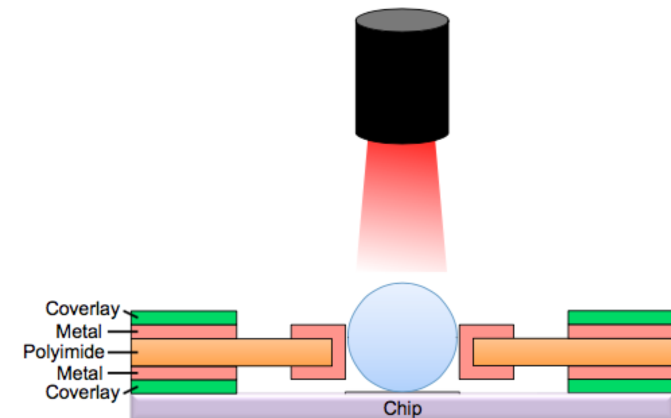
- TSV connect chip M1 from front to back of chip
  - TSV aspect ratio 2:1
- RDL distributes FEI4 connections over full chip surface.
  - Do not need fine-pitch connections.
  - Power can be brought to chip at several places , not just on the edge

Direct laser soldering: flex to FEIx

- Thin 2-layer Al flex
- No glue layer needed
- Connections are solder 1-by-1, module stays at RT
- Re-workable







TSV + RDL project in FEI4

- Working with CEA LETI on TSV last process in FEI4
  - Connect chip M1 from front to back of chip via TSV
- Front side processing in two batches
  - UBM only (4 wafers) – solder on sensors
  - Bumps (3 wafers) – UBM on sensors
- Backside RDL distributes all FEI4 connections over full chip surface
  - Same specs as Medipix but with dedicated FEI4B layout for laser soldering to flex
  - Pad layout to compensate thermal stresses during reflow after flip chip (SCL)
    - Stress compensation has been previously demonstrated between Glasgow & LETI

TSV process description

- Under Bump Metallisation is deposited on the front side of the wafer.
  - Identical to the step used normally by the bump bonding suppliers
  - Finished die can be flip-chip assembled to sensors with solder bumps.
  - Second batch with have solder bumps
- Wafer thinning
  - Wafer front side bonded using a temporary adhesive to a dummy support wafer.
  - The wafer is thinned to 120 um (2 times the diameter of the TSV opening).
- TSV formation
  - Vias are drilled in the wafer using deep reactive ion etching
  - Vias are coated conformally with an insulating layer.
  - Contact holes are etched through the insulation in the bottom of the vias
  - 5um thick Cu layer is deposited on the side of the vias and on the back side of the wafer.
- Redistribution layer
  - The Cu layer is then etched to form the redistribution layer on the backside.
  - The back side of the wafer is passivated and the openings for the solder contacts etched.
  - UBM metallization deposited on the solder pads the same way as on the front side.
- Wafers are probed for electrical functionality
- Die release
  - Wafers are released from the support wafer and transferred onto a dicing tape.
  - Wafers are shipped for subsequent dicing and flip chip assembly.