WP4: microelectronics and interconnections

- WP Coordinators: Christophe de la Taille, Valerio Re

- Goal : provide chips and interconnections to detectors developed by other WPs

- Task 1: Scientific coordination (CNRS-OMEGA, INFN-UNIBG)
- Task 2 : 65 nm chips for trackers (CERN)
  - Fine pitch, low power, advanced digital processing
- Task 3 : SiGe 130nm for calorimeters/gaseous (IN2P3)
  - Highly integrated charge and time measurement
- Task 4 : interconnections between 65 nm chips and pixel sensors (INFN)
  - TSVs in 65 nm CMOS wafers, bonding of 65 nm chips to sensors, exploration of fine pitch bonding processes

AIDA WP4 milestones

MS4.1	**Architectural review of deliverable chips in 65nm run**	**M14 (accomplished)**
MS4.2	**Final design review of 65nm**	**M30 (October 2017)**
MS4.3	Test report of deliverable D4.1	M46 (February 2019)
MS4.4	**Selection of SiGe foundry**	**M14 (accomplished)**
MS4.5	**Final design review of deliverable chips in SiGe run**	**M30 (October 2017)**
MS4.6	Test report of deliverable D4.2	M46
MS4.7	**Selection of TSV process**	**M14 (accomplished)**
MS4.8	**Final design review of deliverable D4.3 (TSV in 65nm)**	**M30 (October 2017)**
MS4.9	Test report of deliverable D4.3	M46

- **Deliverable chips in 65 nm**

  - This work is carried out in the frame of the CERN RD53 international R&D program developing a first generation of pixel readout chip prototypes for ATLAS and CMS at HL-LHC
  - Develop expertise on TSMC 65 nm CMOS selected by CERN for HEP
  - Two small size prototypes were fabricated and are available for testing with sensors
  - A large-scale prototype will be submitted May 2017 in an engineering run
  - This will deliver full wafers for the interconnection with pixel sensors (task 4.4)

Small-medium size 65 nm CMOS prototypes

- Two different chips with a 64x64 50 µm x 50 µm pixel matrix (about 16 mm^2) with different architectures for the analog front-end and the digital readout, different techniques for digital-to-analog isolation,…

- FE65_P2 (Bonn, LBNL), submitted end of September 2015, delivered by the foundry in December 2015 and successfully tested by UBONN with good results. FE65-P2 chips were connected to pixel sensors and the resulting modules were tested in a beam at CERN and SLAC

- CHIPIX65 demonstrator (INFN): submitted July 2016, delivered by the foundry at the end of September 2016. This chip is also fully functional, and tests gave very good results in terms of noise and threshold dispersion. The CHIPIX65 prototype will be soon connected to 3D and planar pixel sensors.

Submission of large-scale 65 nm chip RD53A

- Full design review (with external experts) at CERN in December 2016.

- The review was successful: reviewer's recommendations provided useful guidelines towards the submission of the chip

- Schedule is probably going to shift by a month of two (May 2017)

WP4.3 : SiGe 130 nm

(CNRS-IPNL, CNRS-OMEGA, DESY, AGH-UST)

- Select best SiGe 130/180 nm process for high speed/high dynamic range ASIC design to upgrade current SiGe 350 nm AMS process MS22 M14

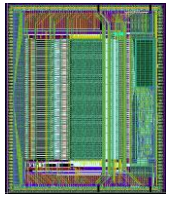
- Deliver SPIROC3 SiPM readout for calorimeter readout of WP14
- Deliver RPC high timing readout chip for WP13
- D4.2 M36 resp CNRS (OMEGA)

- Share expertise within SiGe HEP community

- Studies for LHC run 2, ILC…

SiGe processes evaluation

- 130 nm SiGe processes evaluated
  - Tower Jazz design kit not supplied
  - ST Micro 130 nm SiGe
- Evaluation on different test vehicles
  - ATLAS LAr upgrade
  - CMS HGCAL
  - ATLAS HGTD high speed timing
  - CMS muon RPCs high speed timing
- No significant improvement compared to regular CMOS
  - Better transconductance hindered by Rbb'



- Proposal to choose TSMC 130 nm
  - Qualified by CERN for high radiation environment
  - Wider community (see examples next slides)

Task 4.4 Interconnections and TSVs

(CERN, INFN-GE, INFN-PV, INFN-PG, CNRS-CPPM, CNRS-LAL, MPG-MPP, UBONN, UNIGLA)

- Produce through-silicon vias on wafers from Task 4.2
- Connect chips with TSVs to detectors from WP7
- Test radiation hardness of interconnections

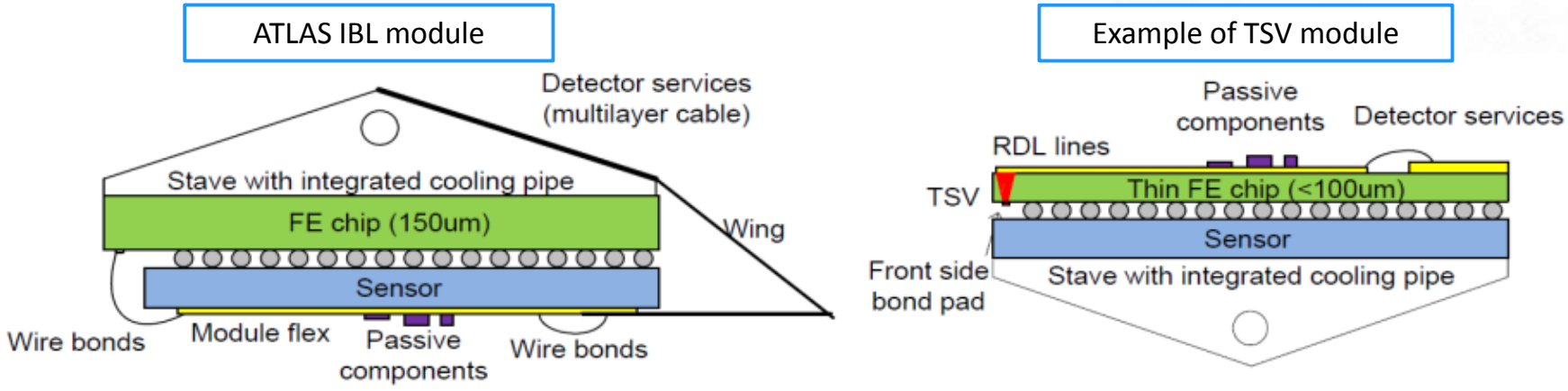
Candidate processes for TSV

WP4 groups are currently working with two different technology providers for Through-Silicon Vias in 130 nm CMOS FE-I4 pixel readout chips:

- IZM (via last tapered TSVs) **(Bonn)**
- CEA-LETI (via last TSVs + RDL + direct wafer-to-wafer bonding) **(Glasgow)**

Results are available. Plans are to extend this study to 65 nm CMOS wafers from the RD53 engineering run.

- Modules with TSV can be used for the outermost detector layers at the HL-LHC to provide full detector coverage over the large area



Goals of TSV processing

- Test processes for peripheral TSVs on the 130 nm FEI4 chip, and apply them to the 65 nm RD53A chip
  - Allow for 4 side buttable modules
  - Enable wafer-to-wafer assembly
  - Remove wirebonds for greater module robustness

- The RD53A chip will be designed so that it is “TSV enabled” (i.e. , compliant with TSV design rules); this involves the peripheral bonding pad regions

- **MS4.7 Selection of TSV process M14 (June 2016) was accomplished: both processes (IZM and CEA-LETI) were selected for the following stages of WP4**

WP4 outlook

- WP4 appears to be on track with respect to the 2017 milestones (delay possible in MS4.8)
- Pixel readout chip prototypes in 65 nm CMOS are available for testing sensors from WP7
- Thanks to synergies with RD53 (65 nm CMOS engineering run), also longer term schedule looks reasonable

AIDA WP4 deliverables

- D4.1 CMOS 65 nm engineering run *(availability of the run with the "ATLAS/CMS" and CLICPIX pixel chips)* (CERN)

  M36 (April 30, 2018)

- D4.2 BICMOS SiGe engineering run *(availability of run with SiPM calorimeter-WP14 and gas detectors-WP13 chips)* (CNRS)

  M36 (April 30, 2018)

- D4.3 Through Silicon Vias production *(fabrication of TSV in wafers of deliverable 4.1)* (INFN)

  M42 (October 31, 2018)