Report on Trigger Logic Unit status

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New TLU design

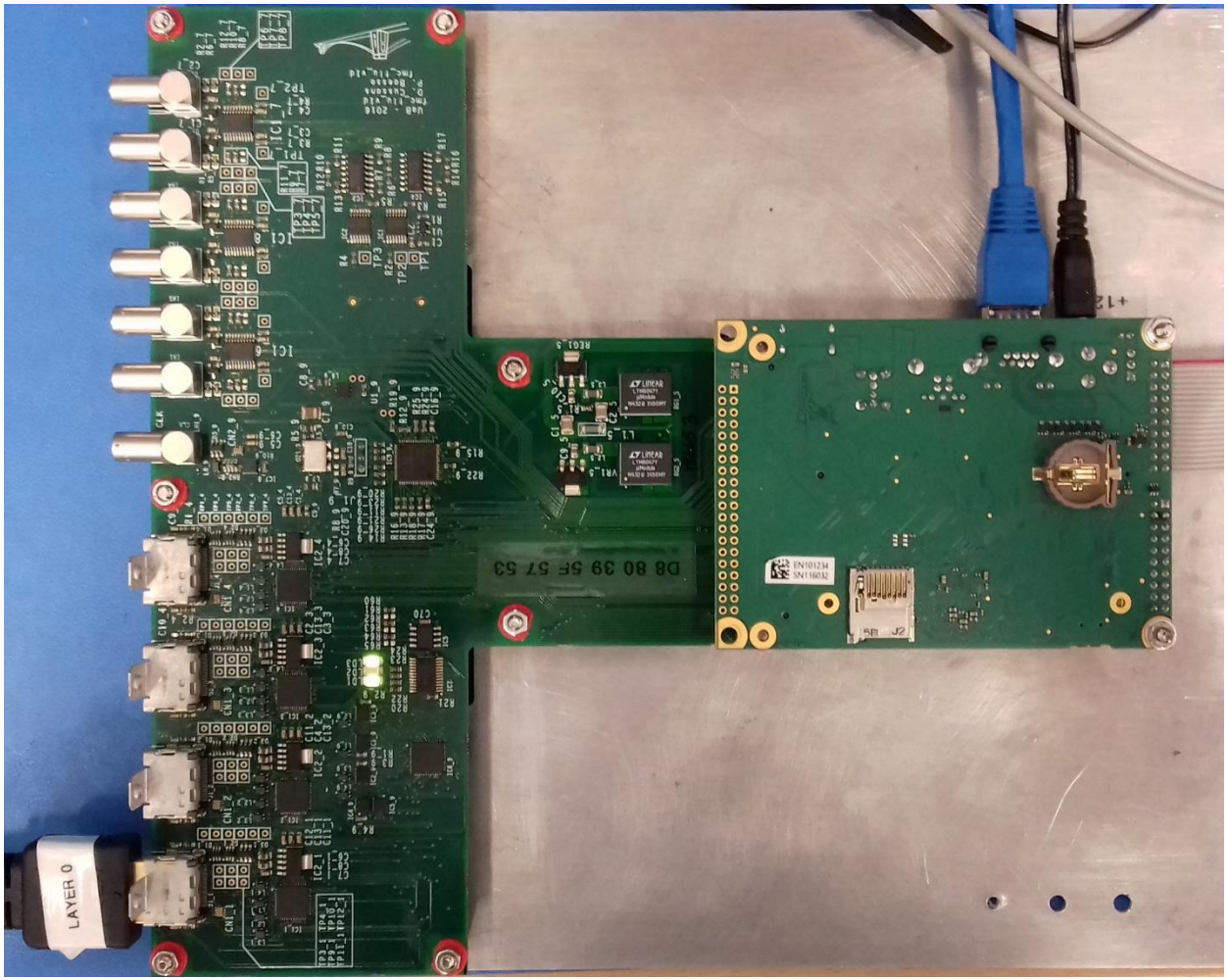
New hardware design based on the successful miniTLU one

- Increased number of DUT
  - from 3 to 4
- Increased number of trigger inputs
  - from 4 to 6
- Multiple clock generation options
  - On-board oscillator
  - DUT
  - Differential LEMO
  - Highly configurable clock chip
- Replaced mini-HDMI with HDMI connector for DUTs interface
- Fast threshold discriminators for trigger detection
- Firmware port to work with Xilinx series 7 devices

New TLU status overview

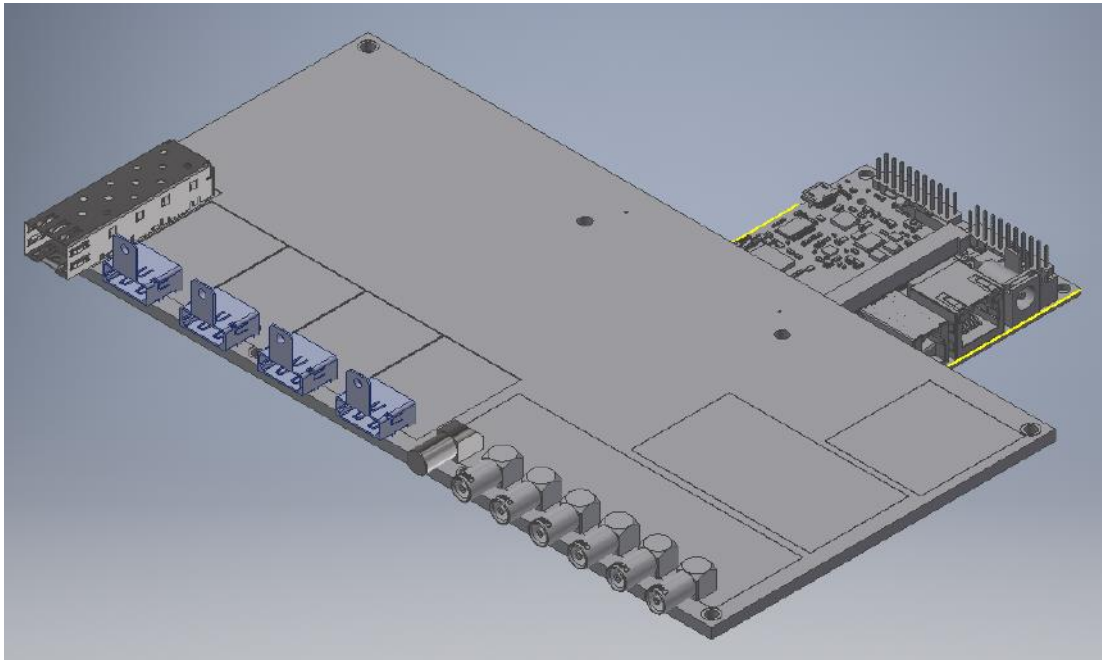
- 2 boards in Bristol + 1 shipped to DESY
- Completed the test on hardware
  - No obvious failures/problems detected
  - A few tweaks desirable for next iteration
  - Schematic for next iteration almost completed
- Completed porting of firmware from old to new hardware
  - Maintain all functionalities from old TLU
  - Tested new functionalities (clock generator, discriminators)
- Basic TLU producer working with EUDAQ2

New TLU hardware



Next hardware implementation

- Maintain FMC connector
- Include SFP cage and CDR chip
  - Recover data and clock from optical or copper link
- Add LED indicators on front panel
- Core circuit maintained from tested design
- Current work in progress
- 1, 2 weeks away from submission to manufacturer

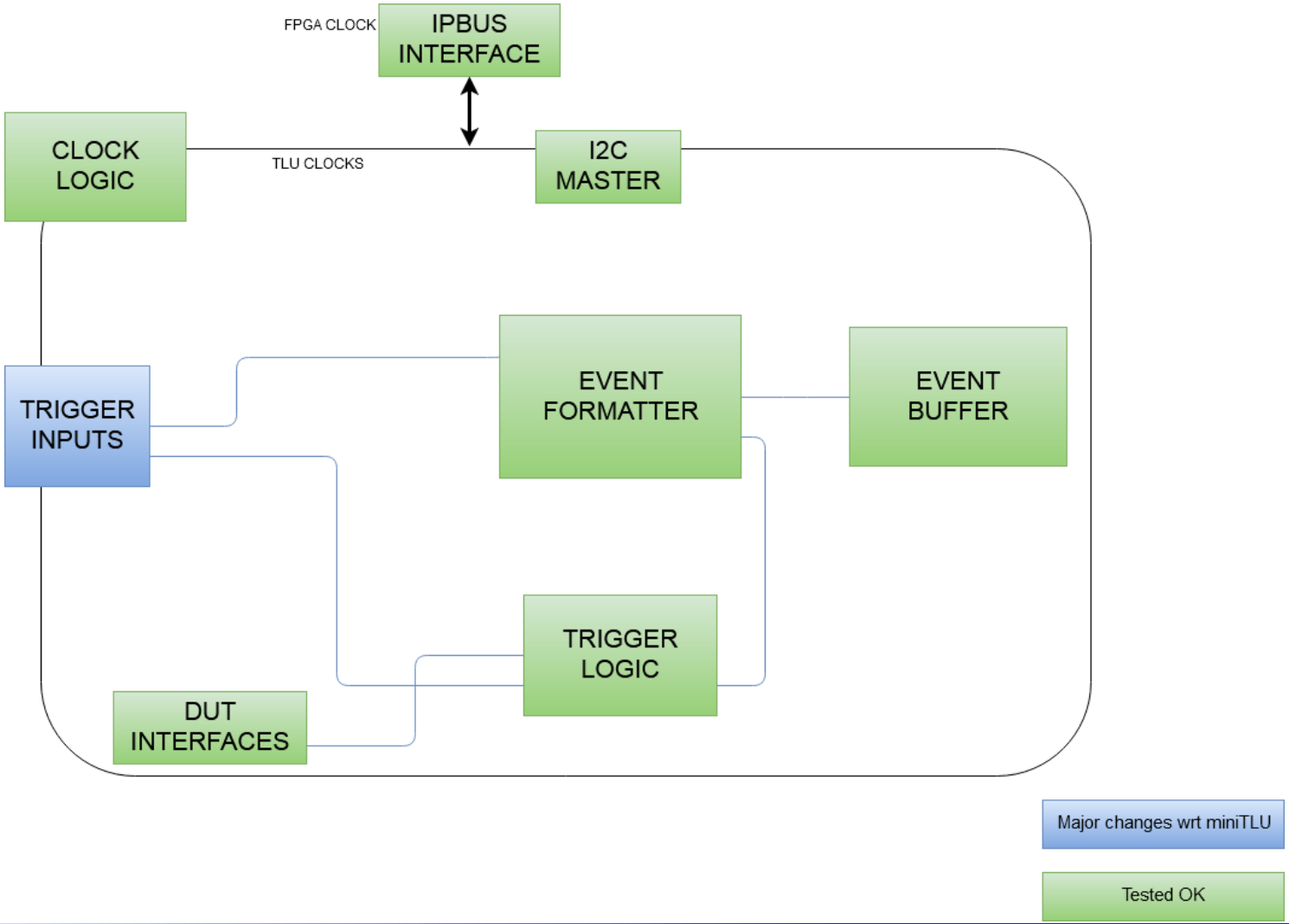


Number of PCB to manufacture depends on requests & funds available.
Still in time to add extra features.
Please talk with D. Cussans or me if interested.

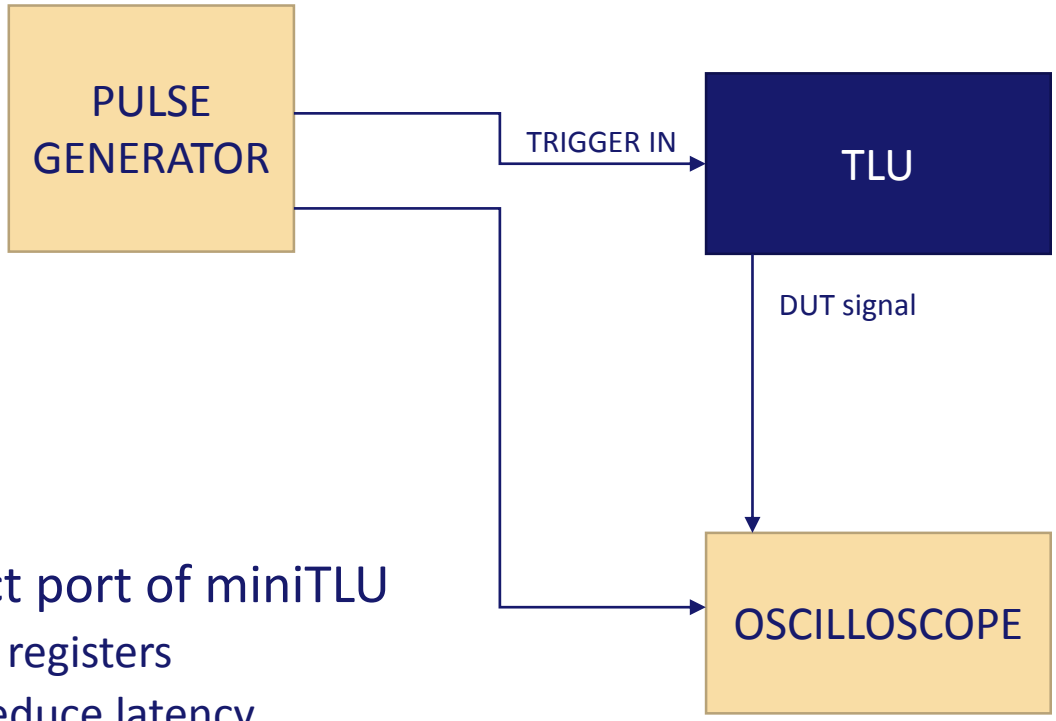
TLU firmware

- Transition from FPGA Series 6 to Series 7 forced us to re-think a few solutions adopted for the miniTLU
  - All blocks now tested and working on bench
  - Still need to implement a more realistic test-setup (master-slave)
- If new hardware feature are added, the firmware will need to be updated
  - The current version would still work (new features disabled)

TLU firmware block diagram

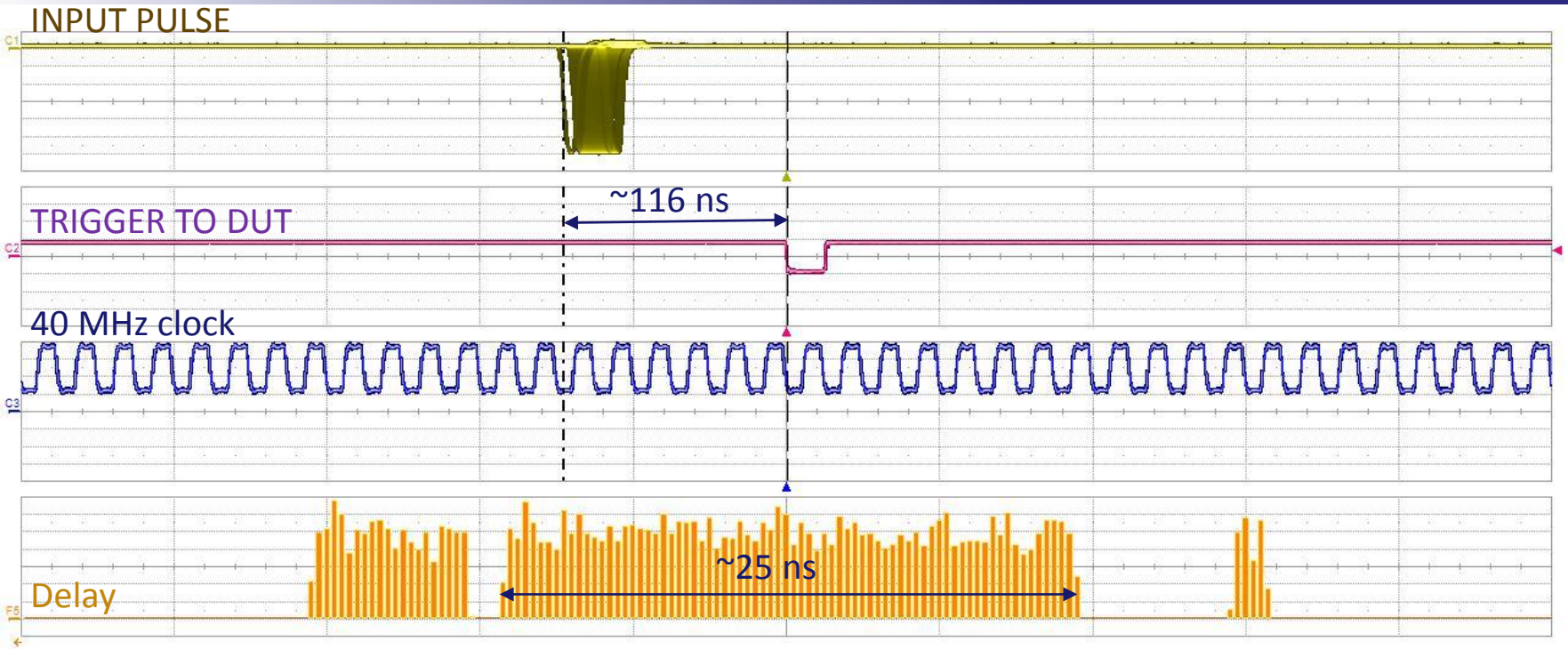


Latency test

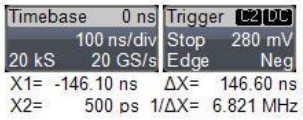


- Testing TLU latency
- Current firmware direct port of miniTLU
  - Includes extra “safety” registers
  - Not yet optimized to reduce latency

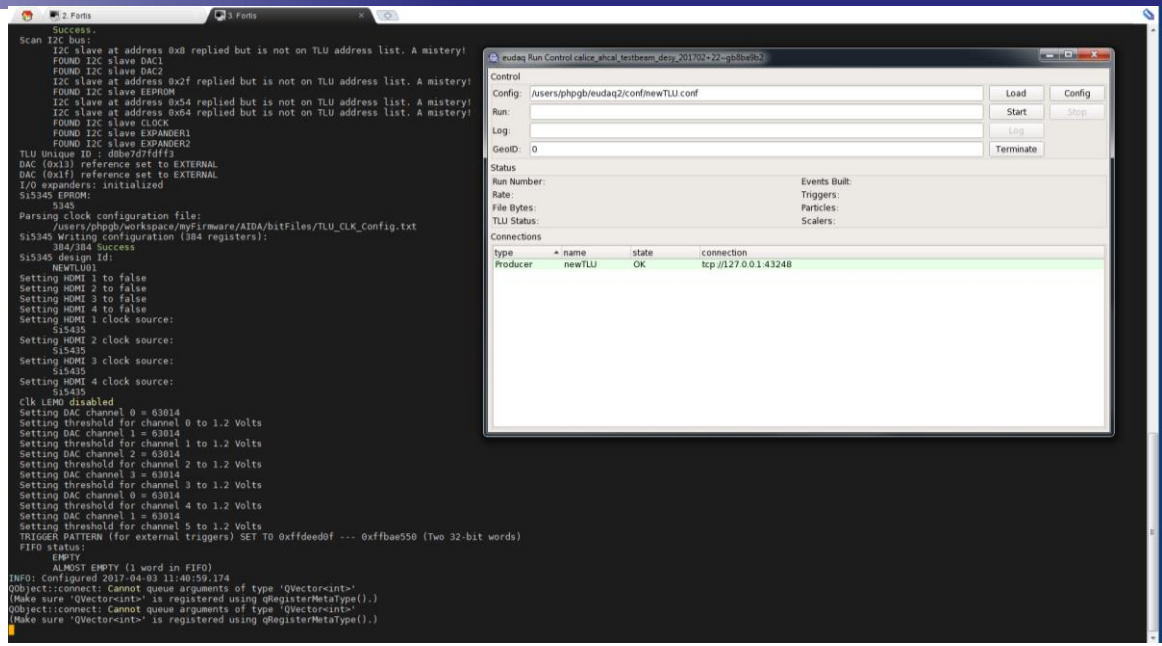
Latency test (non optimized)



Measure	P1:dt@lv(C1,C2)	P2:freq(C4)	P3:- - -	P4:- - -	P5:freq(C4)	P6:- - -	P7:- - -	P8:- - -
value	135.0389 ns	39.6383 MHz						
mean	128.499 ns	40.0063 MHz						
min	114.7949 ns	38.8166 MHz						
max	146.1616 ns	41.2087 MHz						
sdev	7.984 ns	271.6 kHz						
num	14.050e+3	607.737e+3						
status	✔	⚠						



Interfacing with EUDAQ2



- Integration with EUDAQ2:
  - Successfully compiled from sources, added classes for new hardware (clock chip, IO expanders)
  - Configure working correctly (including clock chip)
  - More development/testing needed for run and data writing
- A stable version ready to be pushed on Yi's git repository for testing/merging with his code

Documentation

- Started working on documentation “on the go”
  - Still a very early draft but provides some guidelines to setup and start using the board
- Far from being near to completion, but at least it is moving forward

Summary

- TLU status progressed on all fronts (hardware, firmware, software, documentation)
- We now have a deployable unit
  - Polishing needed on all fronts
  - In this phase it would be useful to have some “real-world” tests, especially with EUDAQ2
- 1-2 weeks away from sending schematics to manufacturer for new boards
  - Still time to add a few features
- Once submitted, 4 weeks to get hardware + time for testing
- Firmware in good status
- We are on time to meet milestone 66 (September 2017) with a fully functional TLU