



AIDA 2020

Advanced European Infrastructures
for Detectors at Accelerators

Report on Trigger Logic Unit status

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New hardware design based on the successful miniTLU one

- Increased number of DUT
 - from 3 to 4
- Increased number of trigger inputs
 - from 4 to 6
- Multiple clock generation options
 - On-board oscillator
 - DUT
 - Differential LEMO
 - Highly configurable clock chip
- Replaced mini-HDMI with HDMI connector for DUTs interface
- Fast threshold discriminators for trigger detection
- Firmware port to work with Xilinx series 7 devices

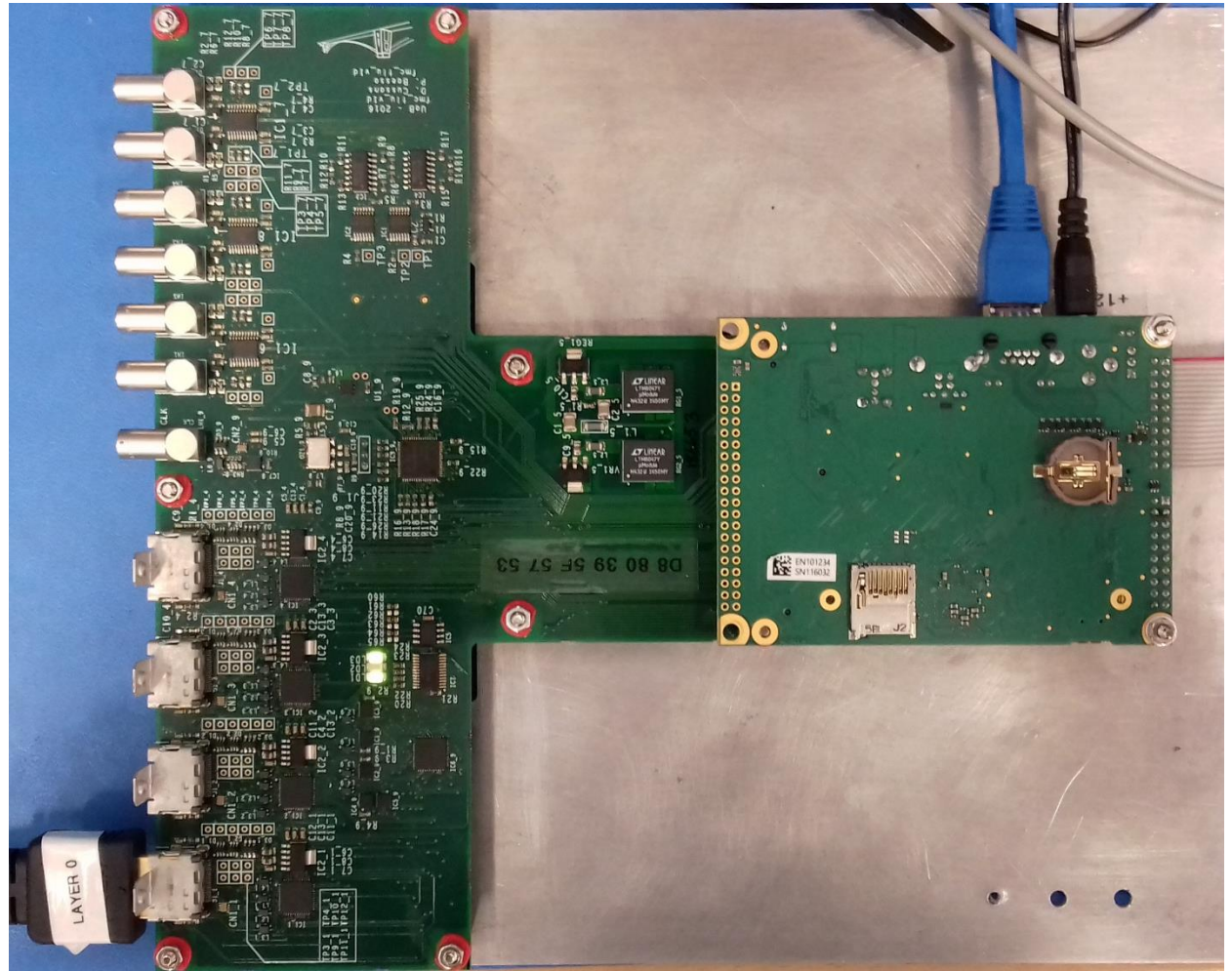


- 2 boards in Bristol + 1 shipped to DESY
- Completed the test on hardware
 - No obvious failures/problems detected
 - A few tweaks desirable for next iteration
 - Schematic for next iteration almost completed
- Completed porting of firmware from old to new hardware
 - Maintain all functionalities from old TLU
 - Tested new functionalities (clock generator, discriminators)
- Basic TLU producer working with EUDAQ2



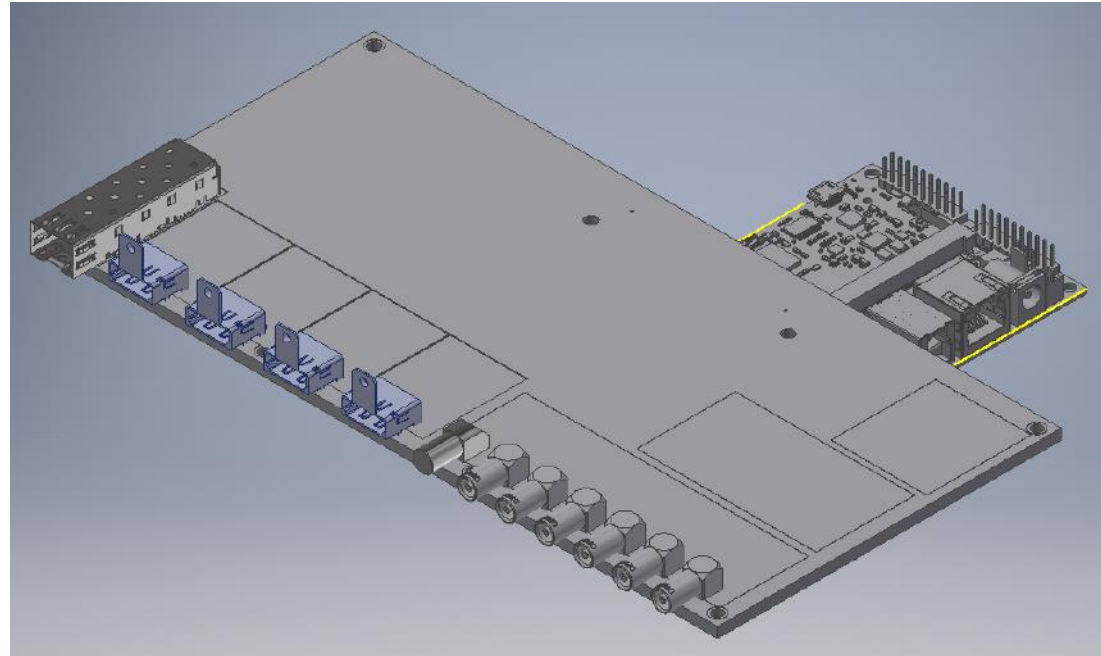
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New TLU hardware





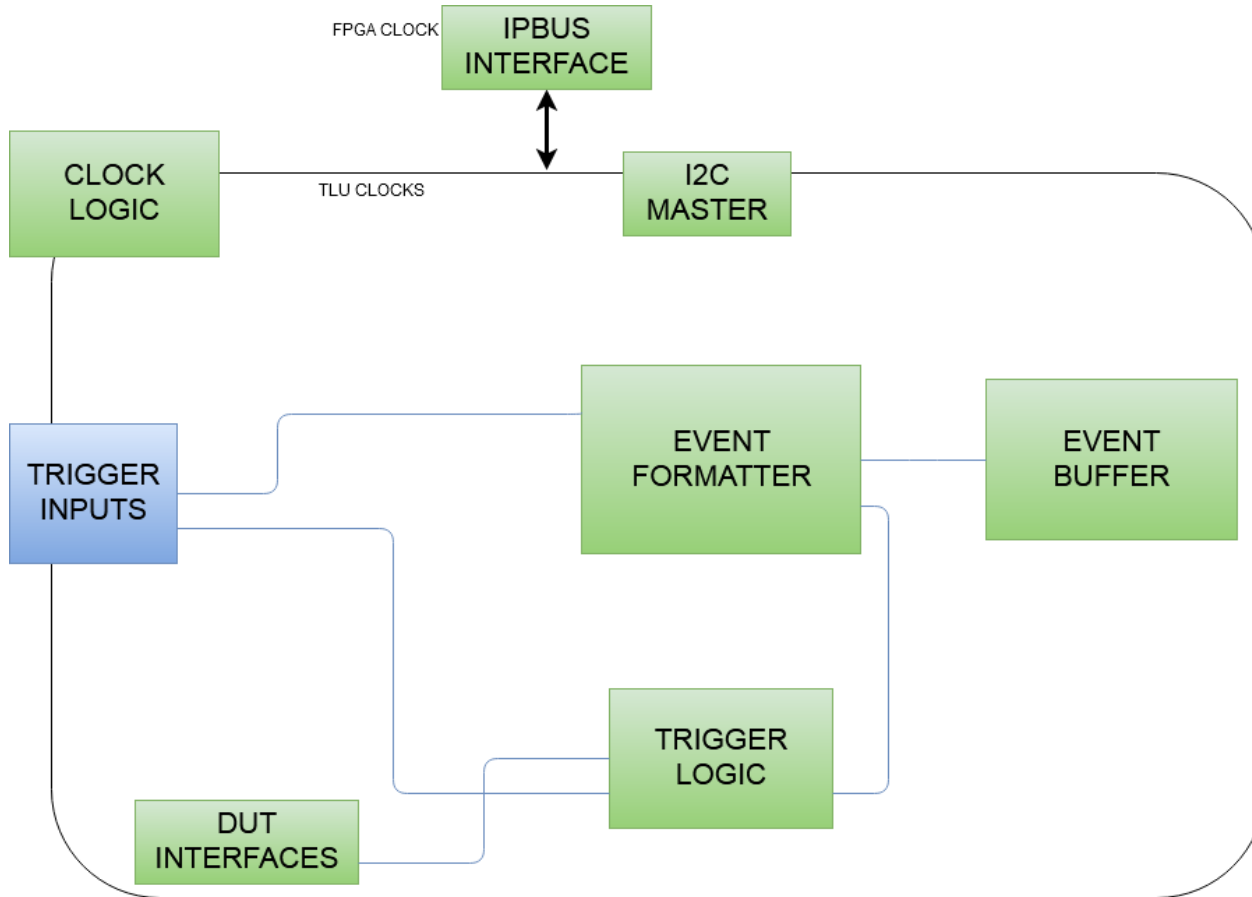
- Maintain FMC connector
- Include SFP cage and CDR chip
 - Recover data and clock from optical or copper link
- Add LED indicators on front panel
- Core circuit maintained from tested design
- Current work in progress
- 1, 2 weeks away from submission to manufacturer



Number of PCB to manufacture depends on requests & funds available.
Still in time to add extra features.
Please talk with D. Cussans or me if interested.

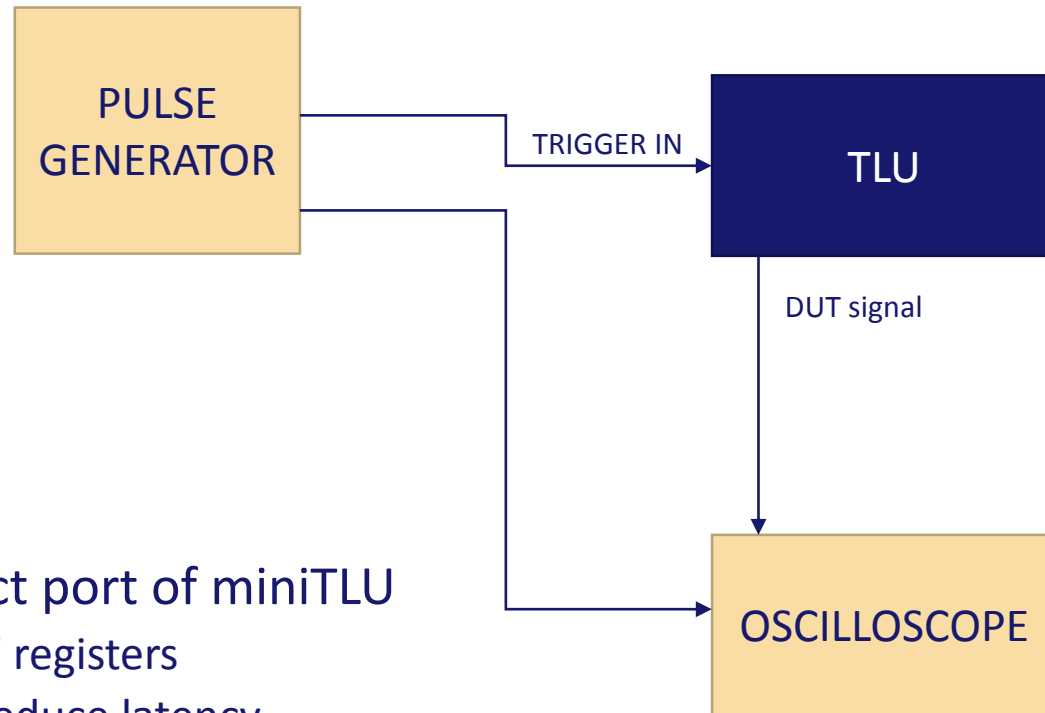


- Transition from FPGA Series 6 to Series 7 forced us to re-think a few solutions adopted for the miniTLU
 - All blocks now tested and working on bench
 - Still need to implement a more realistic test-setup (master-slave)
- If new hardware feature are added, the firmware will need to be updated
 - The current version would still work (new features disabled)

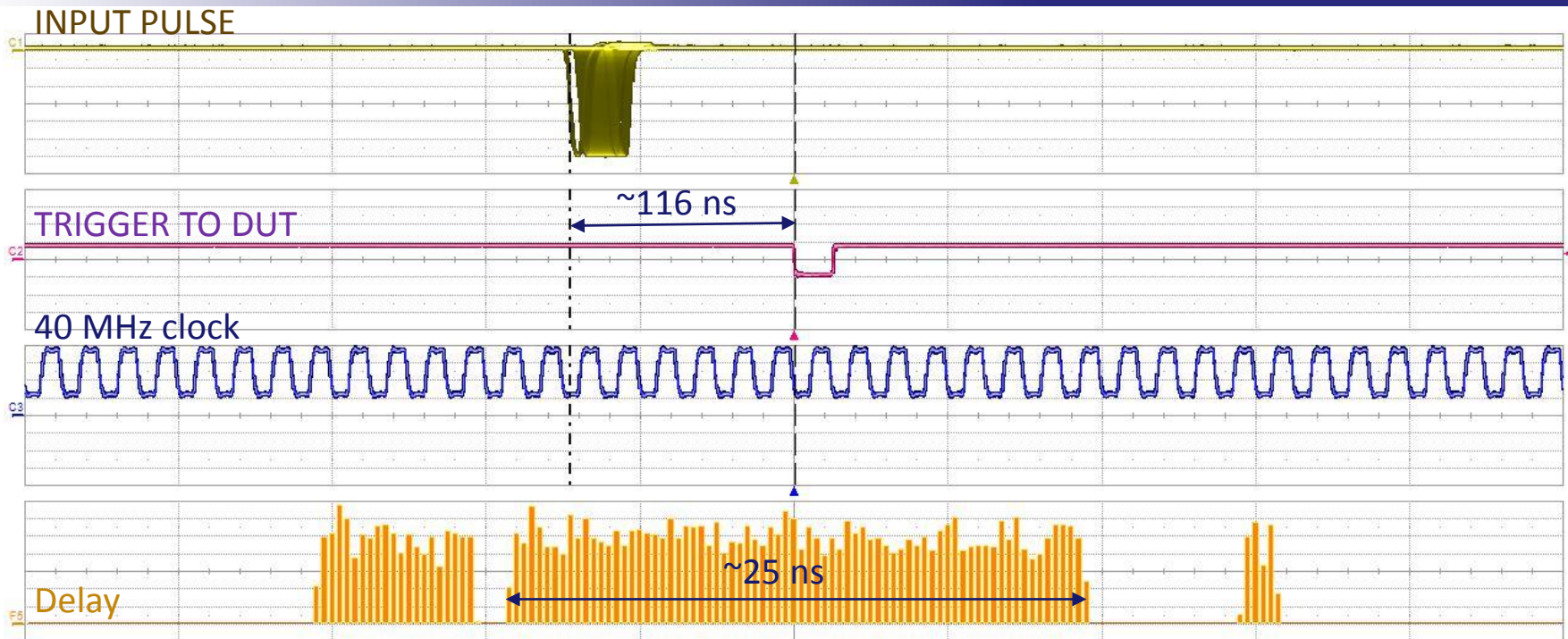


Major changes wrt miniTLU

Tested OK



- Testing TLU latency
- Current firmware direct port of miniTLU
 - Includes extra “safety” registers
 - Not yet optimized to reduce latency



Measure	P1:dt@lv(C1.C2)	P2:freq(C4)	P3:---	P4:---	P5:freq(C4)	P6:---	P7:---	P8:---
value	135.0389 ns	39.6383 MHz						
mean	128.499 ns	40.0063 MHz						
min	114.7949 ns	38.8166 MHz						
max	146.1616 ns	41.2087 MHz						
sdev	7.984 ns	271.6 kHz						
num	14.050e+3	607.737e+3						
status	✓	⚠						

C1	C2	C3	F5
DC1M	DC50	DC1M	hist(P1)
200 mV/div	1.00 V/div	500 mV/div	10.0 #/div
595.0 mV	0 mV offset	0 mV offset	5.00 ns/div
			5.000 k#
↓	↓	↓	↓
Δy	Δy	Δy	Δy

Timebase	0 ns	Trigger	C2 DC
	100 ns/div	Stop	280 mV
20 kS	20 GS/s	Edge	Neg
X1=	-146.10 ns	ΔX=	146.60 ns
X2=	500 ps	1/ΔX=	6.821 MHz



```
Success.
Scan I2C bus:
  I2C slave at address 0xd replied but is not on TLU address list. A mystery!
  FOUND I2C slave DAC1
  FOUND I2C slave DAC2
  I2C slave at address 0x2f replied but is not on TLU address list. A mystery!
  FOUND I2C slave EEPROM
  I2C slave at address 0x54 replied but is not on TLU address list. A mystery!
  I2C slave at address 0x55 replied but is not on TLU address list. A mystery!
  FOUND I2C slave EXPANDER1
  FOUND I2C slave EXPANDER2
TLU Unique ID : d8be7d7dff3
DAC (0x13) reference set to EXTERNAL
DAC (0x1f) reference set to EXTERNAL
I/O expanders: initialized
S15345 EEPROM:
  5345
Parsing clock configuration file:
  /users/phpgb/eudaq2/conf/newTLU.conf
S15345 Writing configuration (S84 registers):
  384/384 Success
S15345 design ID:
  NEWTLU01
Setting HDMI 1 to false
Setting HDMI 2 to false
Setting HDMI 3 to false
Setting HDMI 4 to false
Setting HDMI 1 clock source:
  S15435
Setting HDMI 2 clock source:
  S15435
Setting HDMI 3 clock source:
  S15435
Setting HDMI 4 clock source:
  S15435
Clk LEMO disabled
Setting DAC channel 0 = 63014
Setting threshold for channel 0 to 1.2 Volts
Setting DAC channel 1 = 63014
Setting threshold for channel 1 to 1.2 Volts
Setting DAC channel 2 = 63014
Setting threshold for channel 2 to 1.2 Volts
Setting DAC channel 3 = 63014
Setting threshold for channel 3 to 1.2 Volts
Setting DAC channel 4 = 63014
Setting threshold for channel 4 to 1.2 Volts
Setting DAC channel 5 = 63014
Setting threshold for channel 5 to 1.2 Volts
TRIGGER PATTERN (for external triggers) SET TO 0xffdeedf --- 0xffbae550 (Two 32-bit words)
FIFO status:
  EMPTY
  ALMOST EMPTY (1 word in FIFO)
INFO: Configured 2017-04-03 11:40:59.174
QObject::connect: Cannot queue arguments of type 'QVector<int>'
(Make sure 'QVector<int>' is registered using @registerMetaType().)
QObject::connect: Cannot queue arguments of type 'QVector<int>'
(Make sure 'QVector<int>' is registered using @registerMetaType().)
```

Control window details:

- Config: /users/phpgb/eudaq2/conf/newTLU.conf
- Run: []
- Log: []
- GeoID: 0
- Buttons: Load, Config, Start, Stop, Log, Terminate
- Status: Run Number, Rate, File Bytes, TLU Status
- Events Built, Triggers, Particles, Scalers
- Connections table:

type	name	state	connection
Producer	newTLU	OK	tcp://127.0.0.1:43248

- Integration with EUDAQ2:
 - Successfully compiled from sources, added classes for new hardware (clock chip, IO expanders)
 - Configure working correctly (including clock chip)
 - More development/testing needed for run and data writing
- A stable version ready to be pushed on Yi's git repository for testing/merging with his code



- Started working on documentation “on the go”
 - Still a very early draft but provides some guidelines to setup and start using the board
- Far from being near to completion, but at least it is moving forward



- TLU status progressed on all fronts (hardware, firmware, software, documentation)
- We now have a deployable unit
 - Polishing needed on all fronts
 - In this phase it would be useful to have some “real-world” tests, especially with EUDAQ2
- 1-2 weeks away from sending schematics to manufacturer for new boards
 - Still time to add a few features
- Once submitted, 4 weeks to get hardware + time for testing
- Firmware in good status
- We are on time to meet milestone 66 (September 2017) with a fully functional TLU



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