Update on small-pitch active-edge planar sensor studies for the CLIC vertex detector

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Outline

- Introduction
- Timepix3 thin active-edge sensor studies
- CLICpix thin active-edge sensor studies
- CLICpix2
- Summary/Outlook

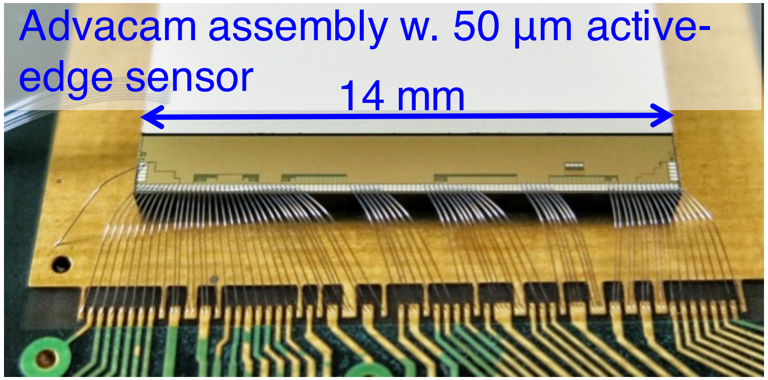
Thin sensor studies for CLIC

Challenging vertex-detector requirements at CLIC:

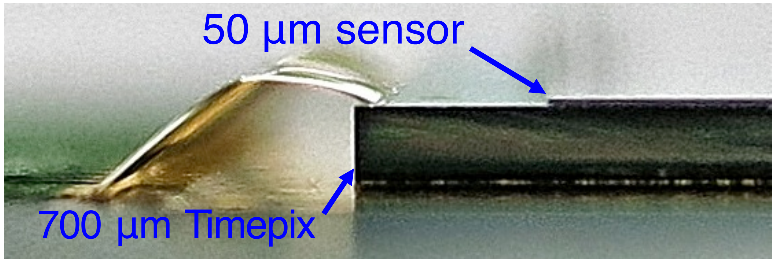
- Ultra-thin (50 µm active silicon)
- High spatial resolution (~3 µm → ~25x25 µm² pitch)
- Precise timing (~10 ns)

→ R&D on hybrid detectors with ultrathin planar sensors

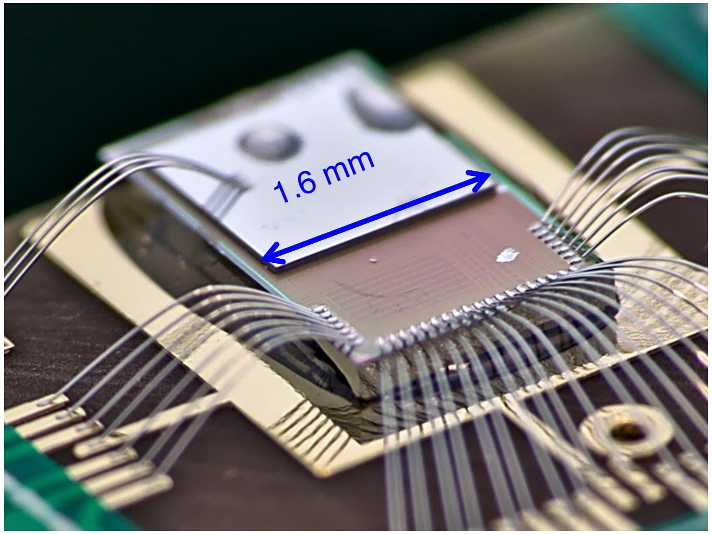
- Timepix3 r/o ASIC (55x55 µm²) to test hybrid assemblies with ultra-thin active-edge sensors (50-150 um)
- More recently: CLICpix r/o ASIC (25x25 µm²) bump-bonded to ultra-thin active-edge sensors (50, 200 µm)



Advacam assembly w. 50 µm active-edge sensor

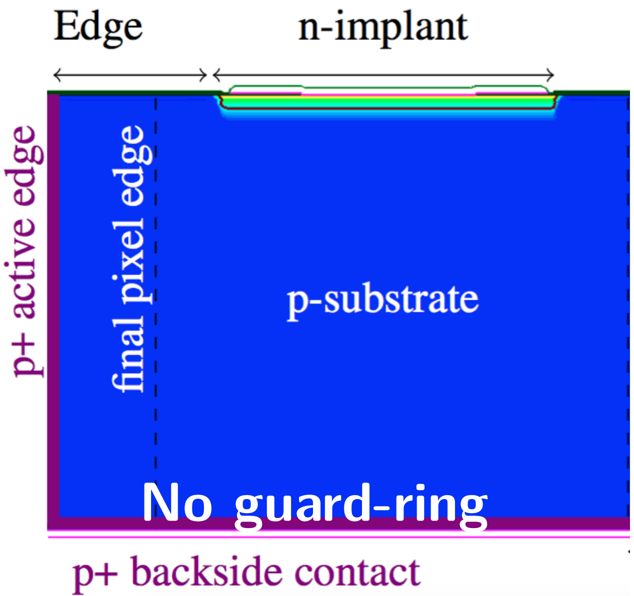


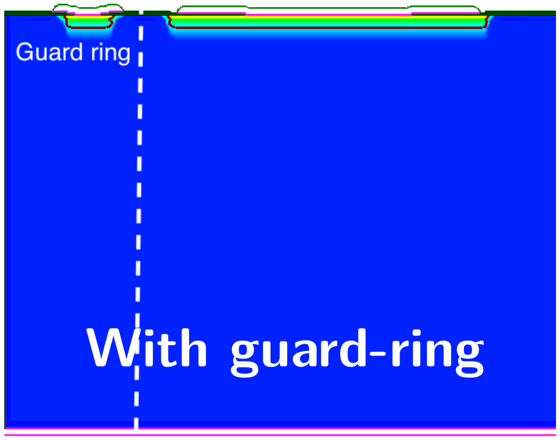
CLICpix with 50 µm sensor



Active edge sensors on Timepix3 ASICs

- Study feasibility of thin sensors with active edge using Timepix3 ASICs
- 50 µm to 150 µm thick n-in-p sensors, 55 µm pixel pitch
- Deep Reactive-Ion Etching is used to cut the edge of the silicon sensor
- Implantation on the sidewall of the sensor ⇒ extension of the backside electrode on the edge ⇒ Charge created in the edge region can be collected by the first pixel
- Reduction of inactive area, good coverage without overlapping sensor tiles, reduction of material budget

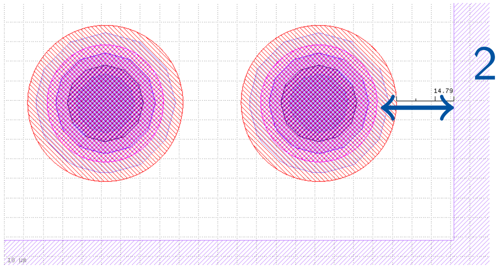




Guard-ring layouts

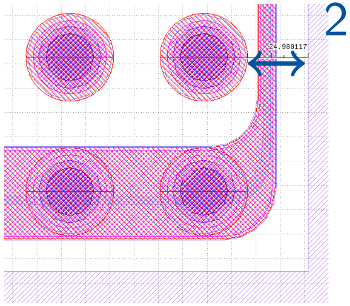
- 4 different guard ring layouts implemented
- Edge distance is defined as the distance between the last n-implant and the cut edge

- 20 µm edge, no guard-ring



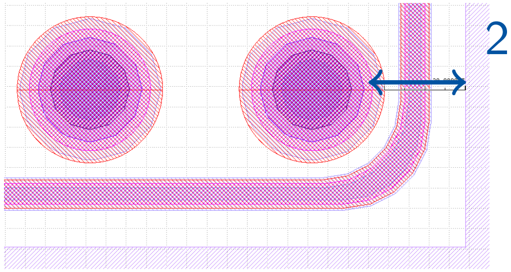
20 µm

- 28 µm edge, GND guard-ring



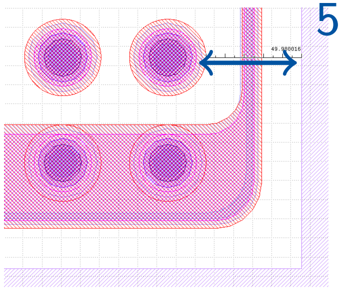
28 µm

- 23 µm edge, floating guard-ring



23 µm

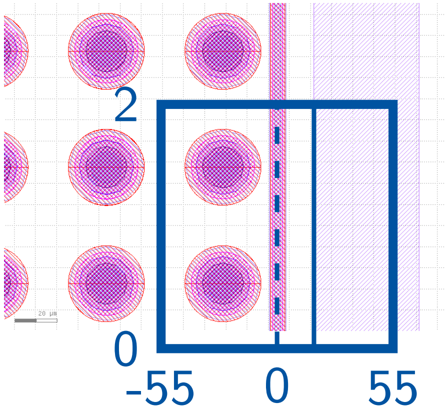
- 55 µm edge, GND guard-ring



55 µm

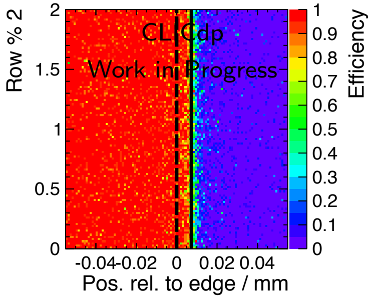
Edge performance evaluation

- Performance at the edge:
  - Consider only tracks close to the sensor edge
  - Tracks are periodically mapped into a 2 by 2 pixel cell
  - For illustration, end of the periodic pixel matrix (dashed line) and physical edge of the sensor (solid line) are indicated in the following plots

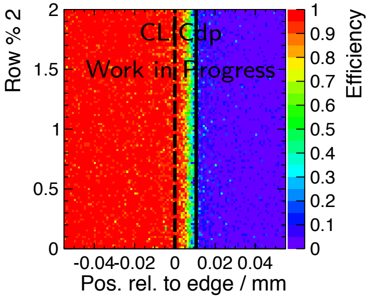


Efficiency and signal at the edge

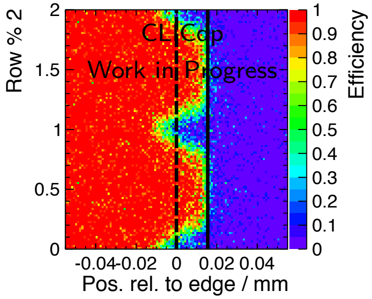
- 50 µm thick, 20-noGR



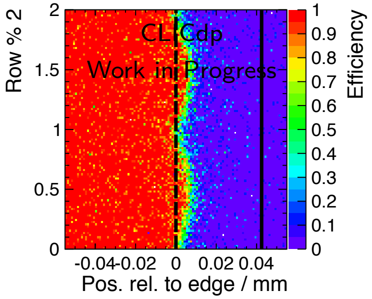
- 50 µm thick, 23-floatGR



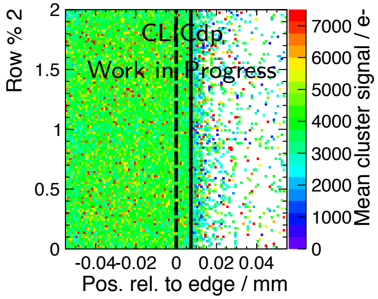
- 50 µm thick, 28-groundGR



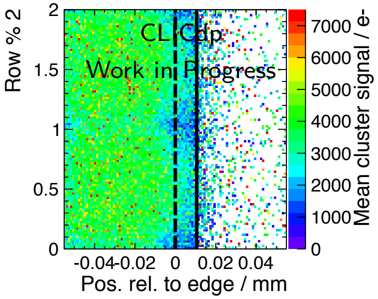
- 50 µm thick, 55-groundGR



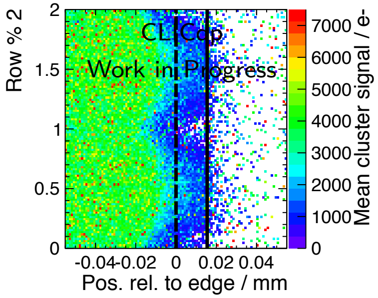
- 50 µm thick, 20-noGR



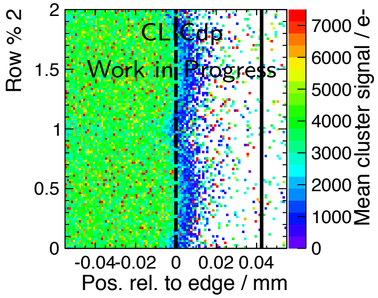
- 50 µm thick, 23-floatGR



- 50 µm thick, 28-groundGR

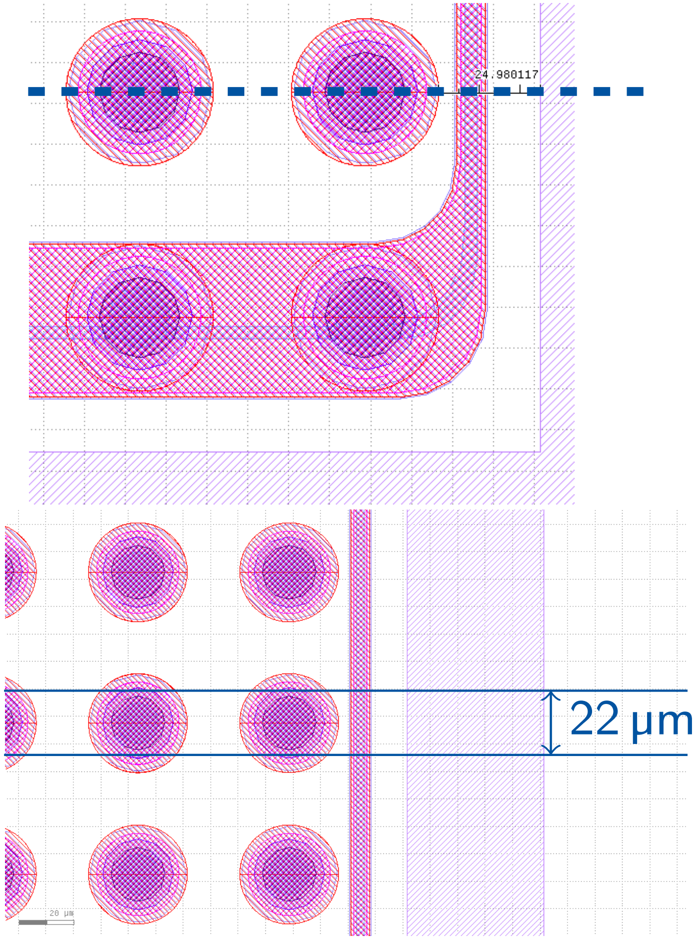


- 50 µm thick, 55-groundGR



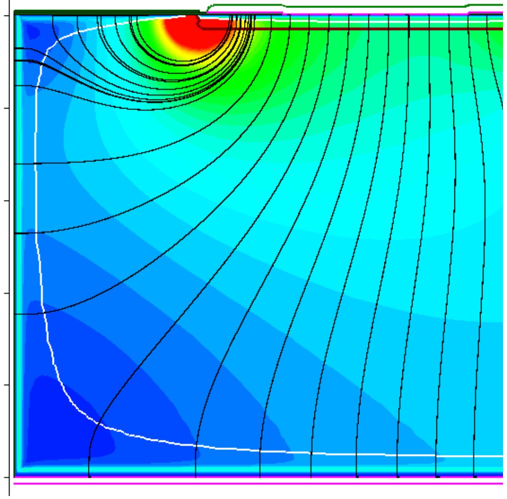
TCAD simulation

- Implementation of different edge geometries and guard ring layouts in Synopsys Sentaurus
- 2D simulation → cut at center of pixel implant
- Static (electric field) and transient simulation (MIP scan)
- Simplified: noise, threshold and landau fluctuations not included
- For better comparability in 2D simulation: restrict data to tracks passing close to pixel center



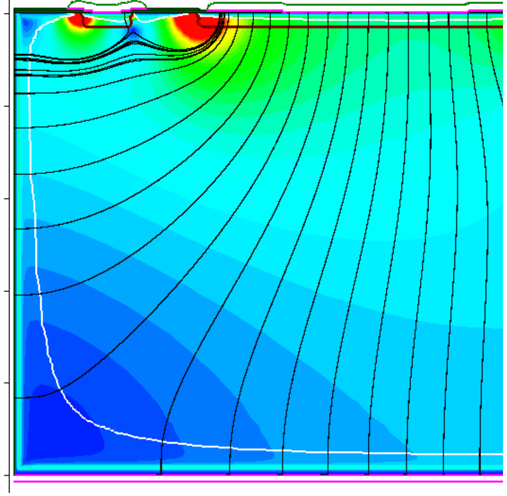
Electric field for different guard-ring layouts

- $\sim 20\,\mu\text{m}$ edge, $50\,\mu\text{m}$ thick
- Electric field and depleted region extend towards the edge



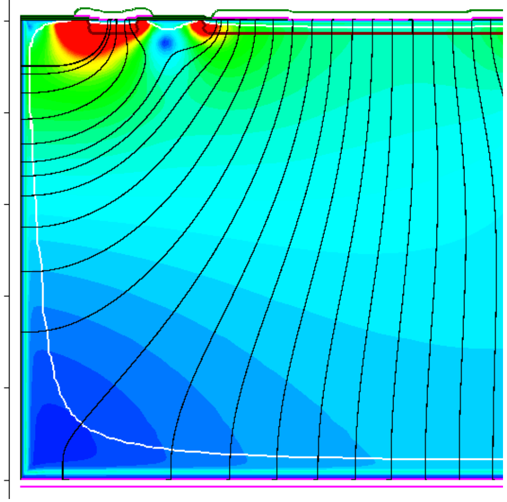
No guard-ring

- Field lines end at the last pixel
- Expect no charge loss



Floating guard-ring

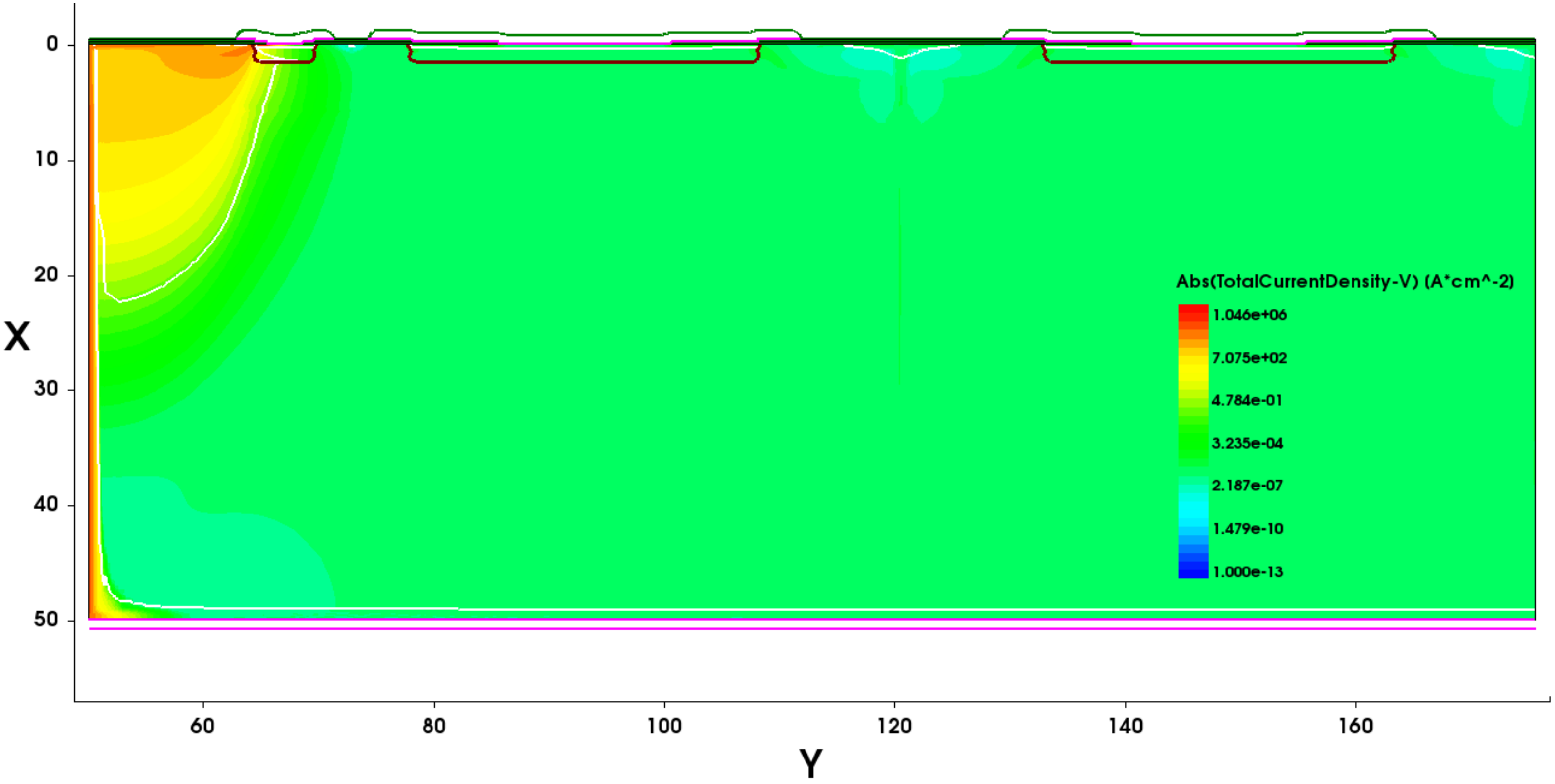
- Most field lines end at the last pixel
- Small charge loss



Grounded guard-ring

- Some of the lines end at the GR
- Significant charge loss to GR

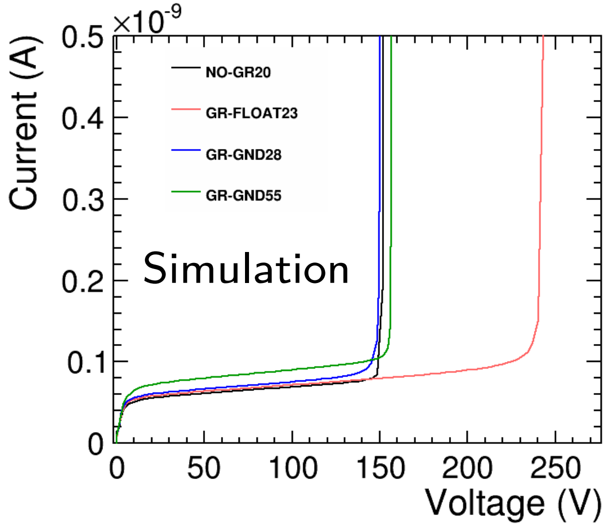
Current breakdown simulation

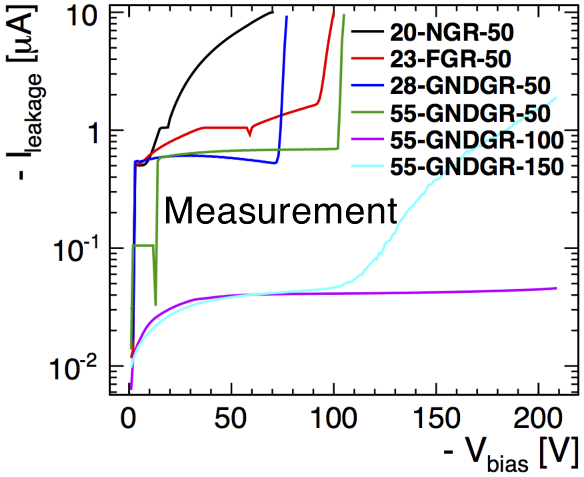


- Total current density
- 50 µm thick, grounded guard ring
- Breakdown occurs between the edge and the first implant

Current breakdown simulation vs. data

- 50 µm thickness: no guard ring and grounded guard ring break down around 150 V
- Similar distance between edge and first grounded implant
- Floating guard ring smoothens potential drop
- Lower electric field at given bias → higher V_{bd}
- Comparison to measurements not easy, measurement not very reproducible
- Extra row of bumps influencing floating guard ring and/or active edge

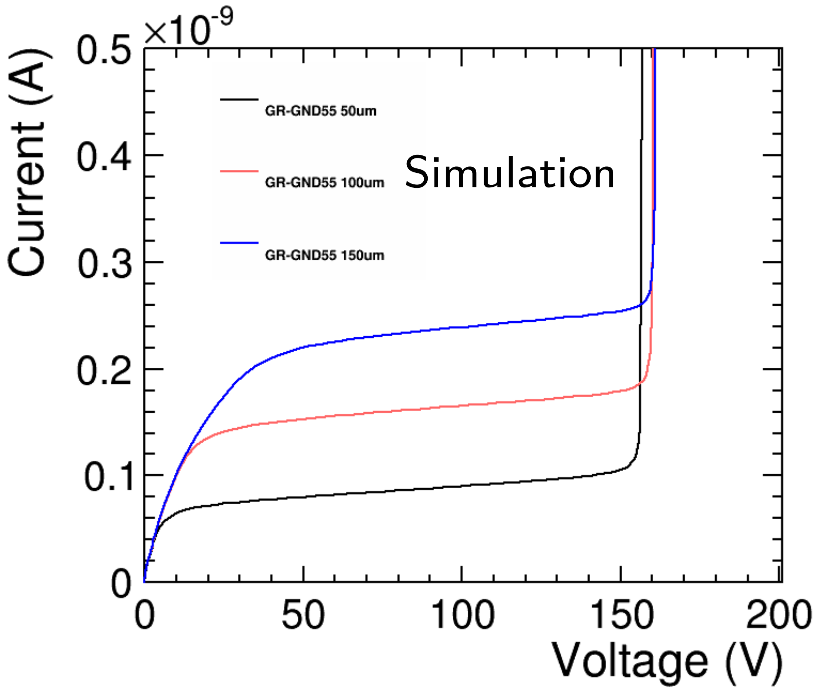




V_{dep} between -7 V (50 µm) and -15 V (150 µm)
→ all assemblies can be operated well beyond V_{dep}

I/V – dependence on sensor thickness

- Thicker devices, grounded guard ring, 55 µm edge
- For given guardring layout, field at the surface not depending on the sensor thickness → V_{bd} not depending on the thickness



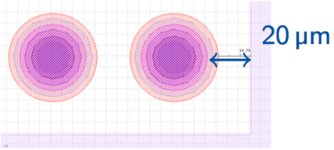
I/V for new assemblies

- 4 additional 50 µm sensor assemblies produced by Advacam
  - modified bump mask: first row in Timepix3 not bumped (used normally for grounding the guard ring)
    → better suited for floating and no GR (no risk of shorting edge)
  1) No GR, 20 µm edge → improved breakdown ~125 V
  2) No GR, 50 µm edge → similar breakdown as 1) (design previously not tested)
  3) Floating GR, 52 µm edge → high breakdown voltage ~180 V (design prev. not tested)
  4) Floating GR, 23 µm edge → breakdown ~90 V, similar to previous assemblies

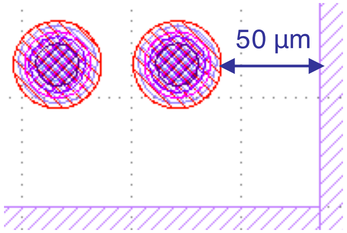
→ Designs w/o GR work well

→ Designs with floating GR work well, except for 23 µm edge distance (distance between GR and pixel implant too small?)

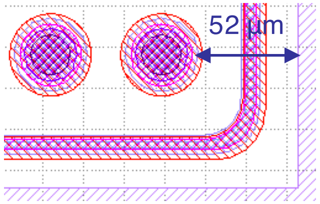
1)



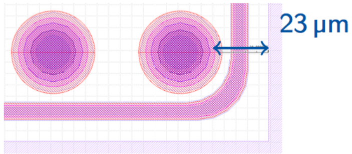
2)

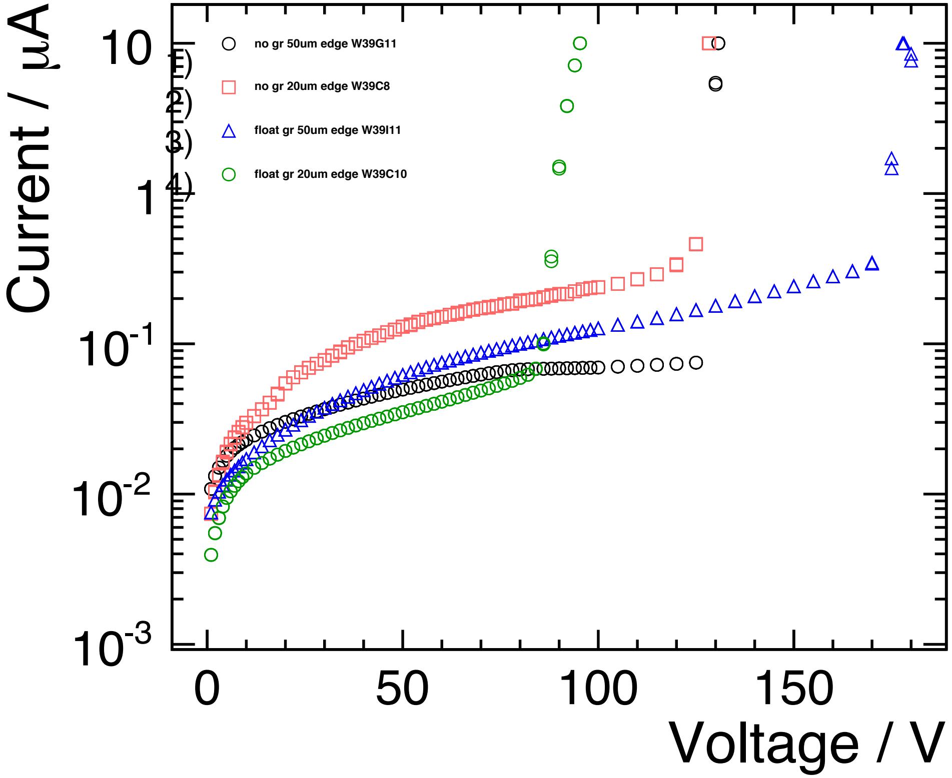


3)



4)



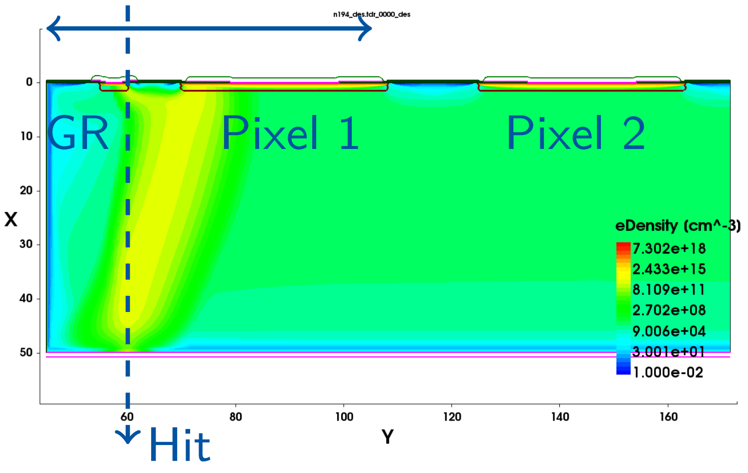


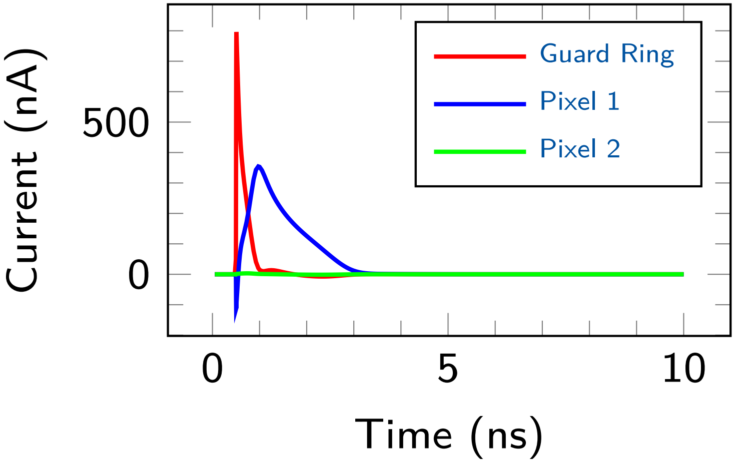
Transient simulation

- Create charge along particle path, constant ionization
- Collect charges at the electrodes
- Record transient current in electrodes
- Integrate to obtain charge signal
- Scan particle over the edge region

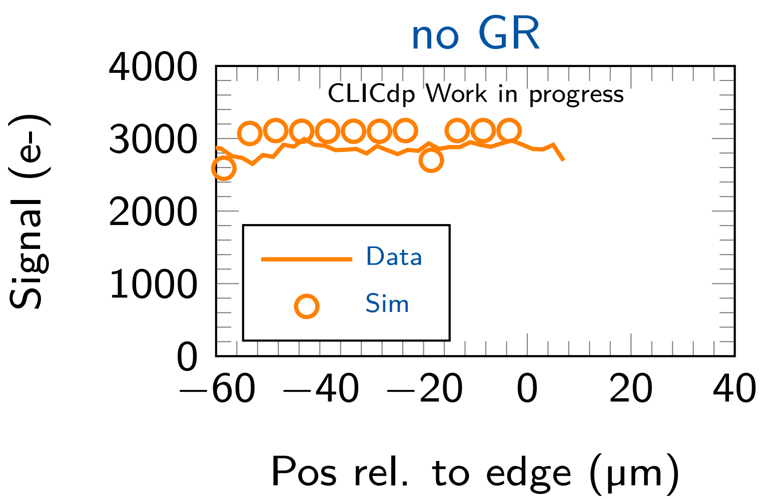
- Example for a 50 μm thick sensor with grounded guard ring:

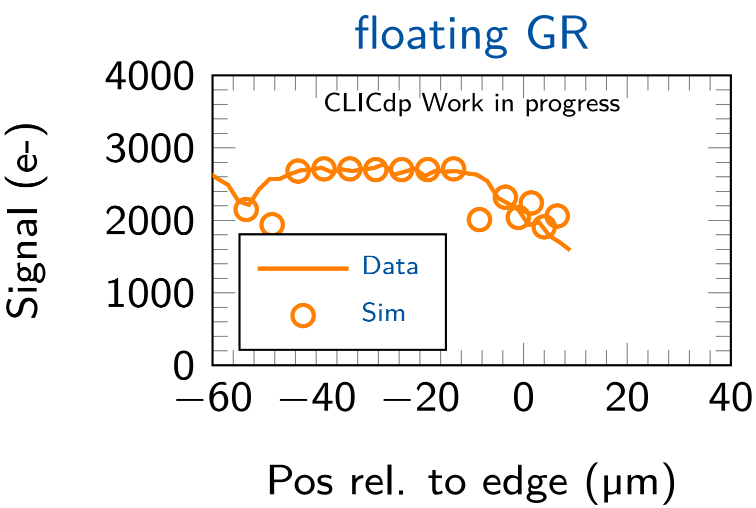
Electron density

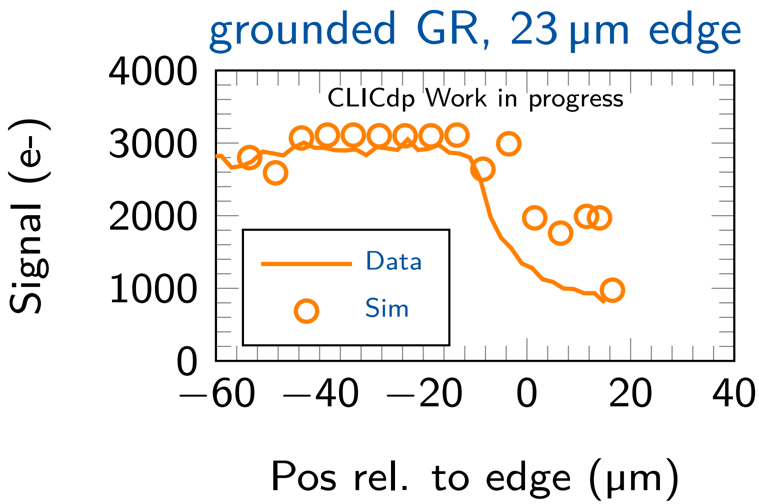


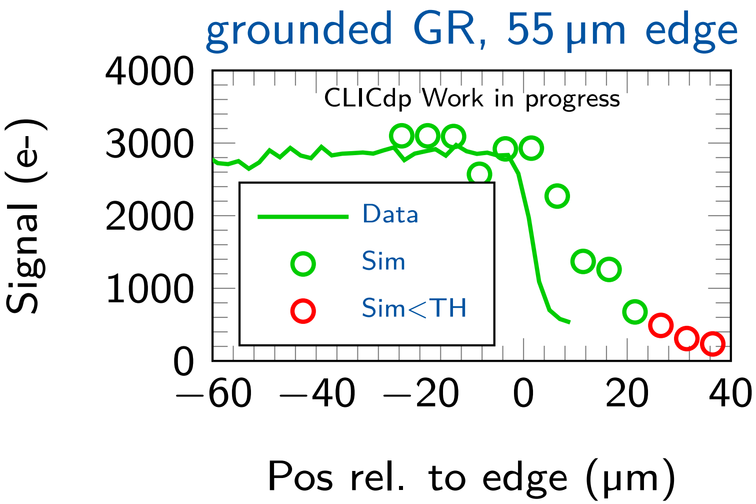


Signal at the edge – TCAD vs. data


no GR

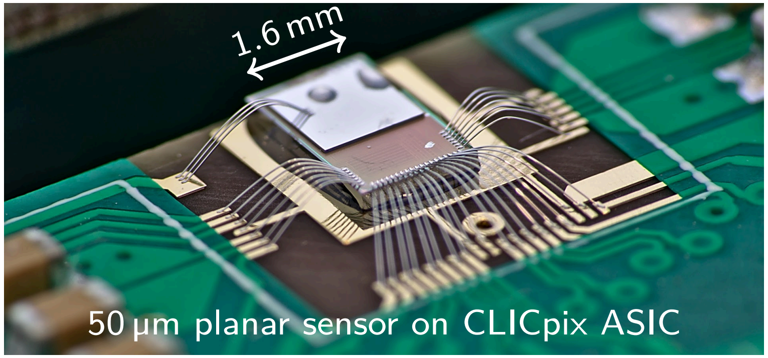

floating GR


grounded GR, 23 µm edge

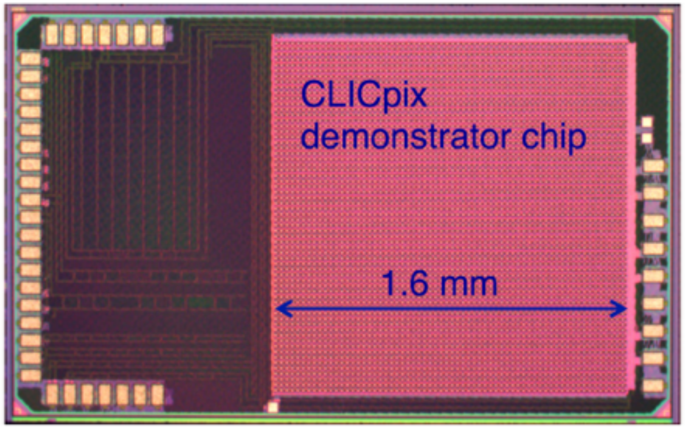

grounded GR, 55 µm edge

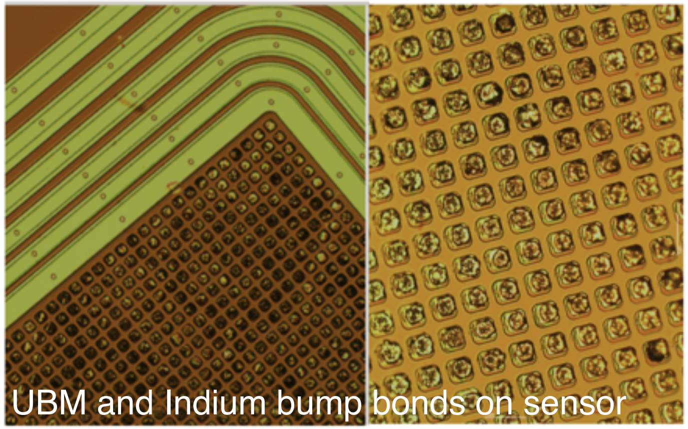
CLICpix planar sensor assemblies

- Single-chip Indium bump-bonding process for 25 µm pitch developed at SLAC
- Assemblies produced with 200 µm, 150 µm and 50 µm n-in-p sensors
- 200 µm assembly tested in AIDA telescope at SPS in 2015
- This talk: 50 µm assembly tested in Timepix3 telescope at SPS in August 2016



50 µm planar sensor on CLICpix ASIC

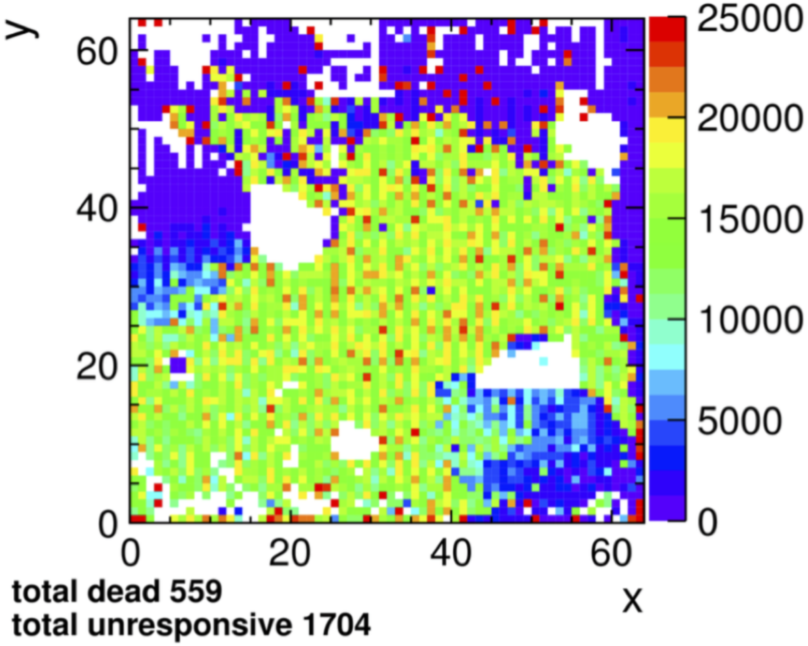




UBM and Indium bump bonds on sensor

CLICpix with 50 µm thin active-edge sensor

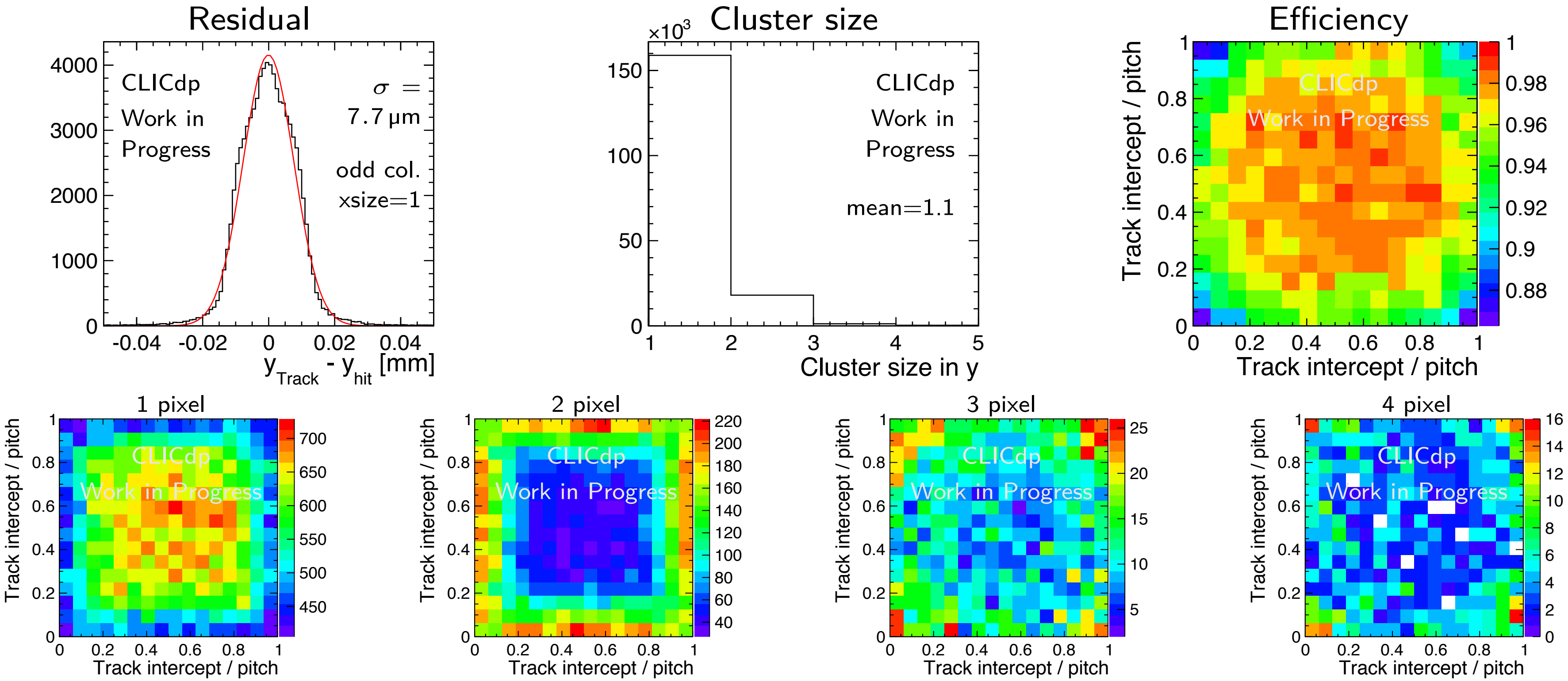
- Advacam 50 µm thin planar n-on-p sensor with active edge
- Assembly shows large dead regions and can only be biased up to 5 V
  → Possible improvements in bump-bonding process identified, more assemblies to come
- Our first 50 µm assembly with 25 µm pixels → Testbeam → focus analysis on good regions
- No edge efficiency results



total dead 559
total unresponsive 1704

CLICpix thin-sensor analysis results

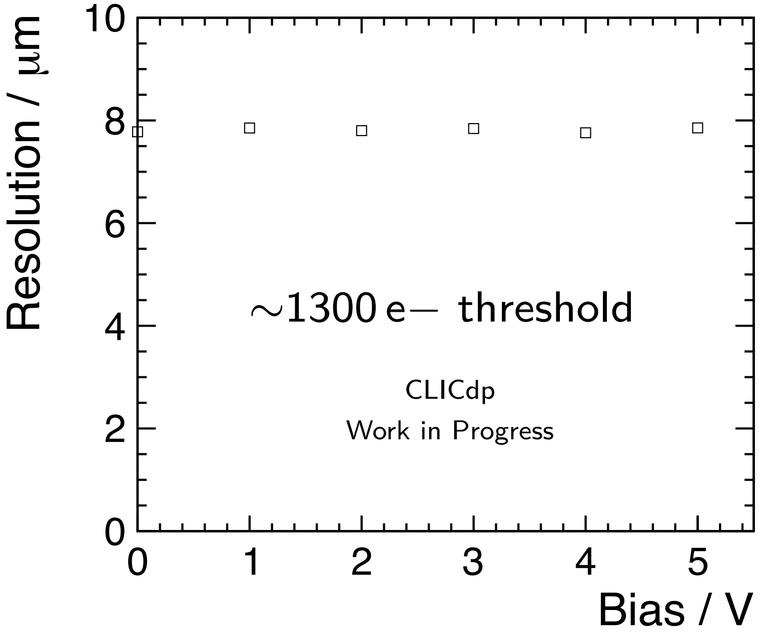
- 5V bias, $\sim 1300\,e^-$ (lowest possible threshold for this assembly)

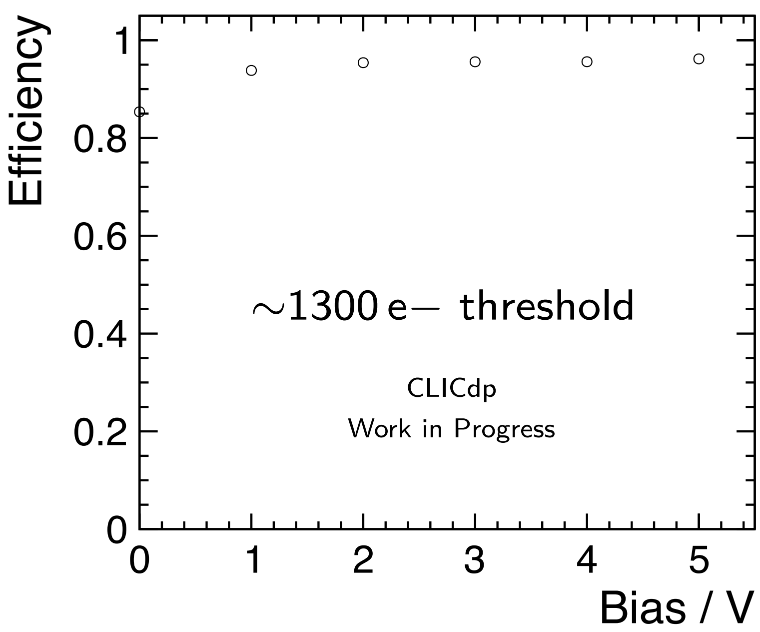


- DUT performance as expected from 50 µm thin sensor at this threshold
- Telescope pointing resolution of ~ 2 µm allows for in-pixel studies even with 25 µm small pixels

CLICpix thin-sensor bias scan

- Bias scan from 0 V to 5 V
- Very low depletion voltage around 1 V

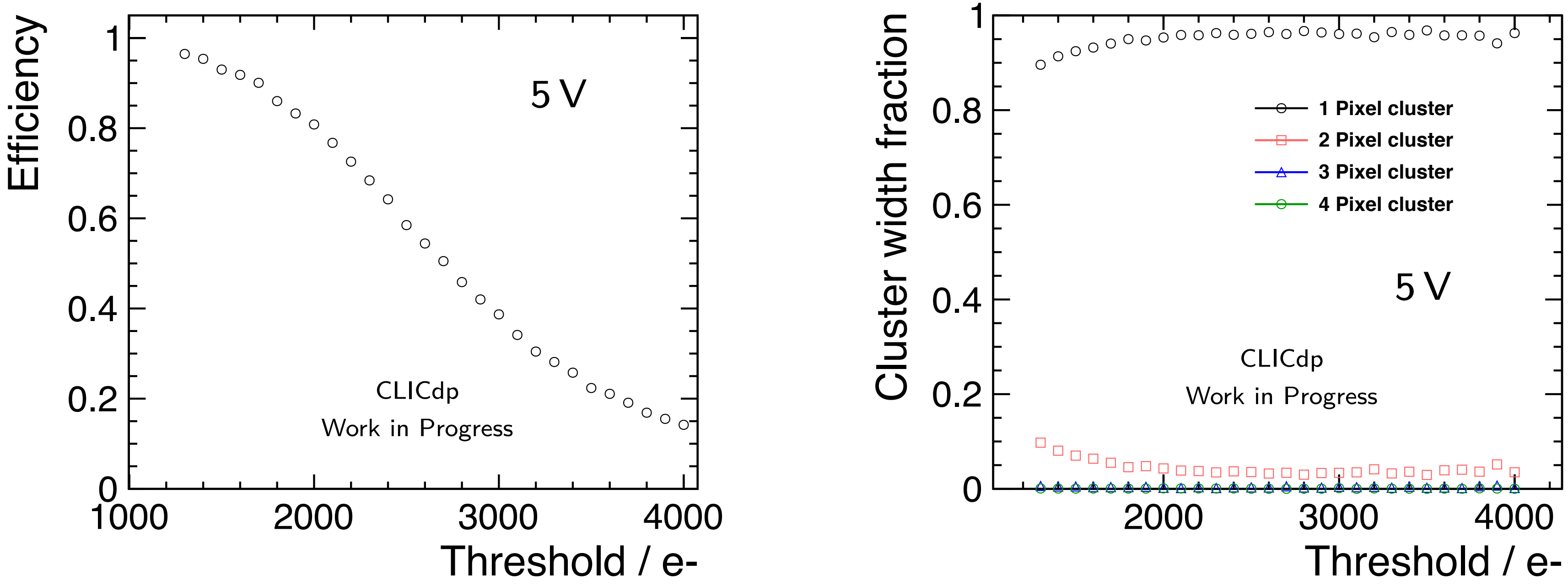




- Cluster size and resolution almost independent from bias voltage
- Efficiency constant above full depletion

CLICpix thin-sensor threshold scan

- Threshold scan from 1300 e$^-$ to 4000 e$^-$

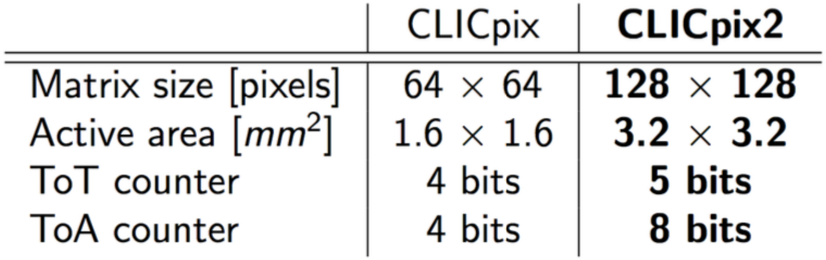


- High efficiency reached at lowest possible threshold, non-responsive regions masked
- Efficiency drops quickly with threshold, as expected for 50 μm thin sensor
- ⇒ Threshold has to be set as low as possible for efficient operation

CLICpix2

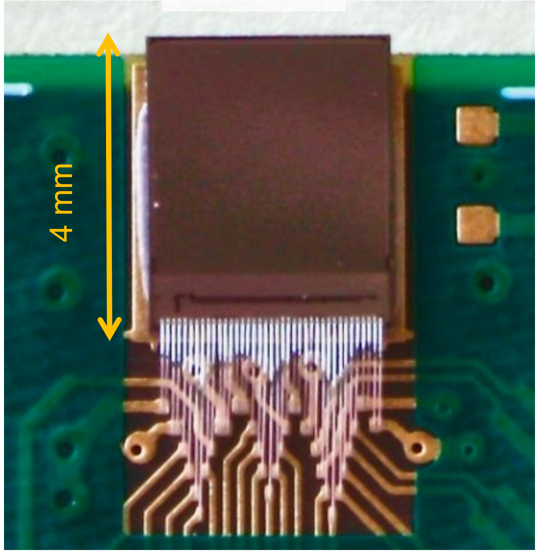
New CLICpix2 65 nm ASIC:

- 4x larger matrix
- reduced threshold
- Increased TOA and TOT dynamic range
- Currently under test with new Caribou r/o system
- Additional submission with RD53 and MPA (submission end of May 2017)
  → access to full wafers
  → bump bonding process development

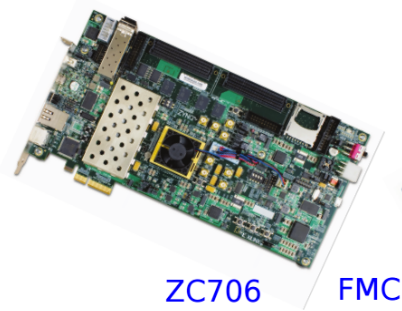


	CLICpix	**CLICpix2**
Matrix size [pixels]	64 × 64	**128 × 128**
Active area [mm^2]	1.6 × 1.6	**3.2 × 3.2**
ToT counter	4 bits	**5 bits**
ToA counter	4 bits	**8 bits**

CLICpix2



Caribou universal readout system


ZC706


FMC cable (optional)


CaR board


chipboard

Summary/Outlook

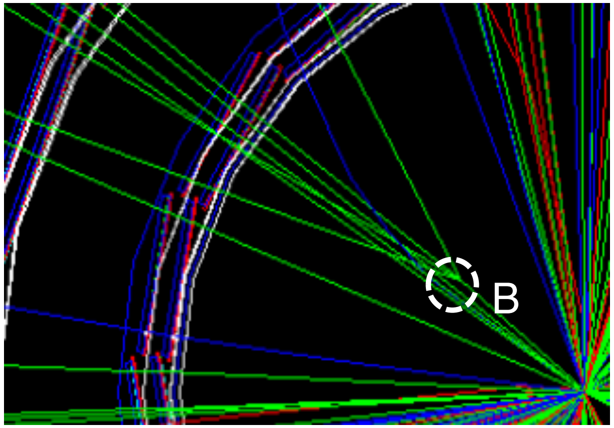
- Thin planar active-edge sensors with Timepix3 readout
  - Guard-ring design affects edge signal, efficiency and I/V breakdown
  - T-CAD simulations compatible with measurements (D7.2, D7.6)
  - >99% efficiency up to physical edge for 50 µm thick sensors
  - Improved I/V breakdown with new bump mask
- 50 µm thin planar active-edge sensor with CLICpix readout
  - Low bump yield, but assembly is operational
  - Small amount of charge sharing in thin sensor limits resolution
  - Degraded detection efficiency (~97%) due to high threshold (1300 e^-)

- Outlook:
  - CLICpix2 with larger matrix and reduced minimum threshold
    → expect improved resolution, increased efficiency
  - New active edge sensors from FBK: CLICpix2, Timepix3 footprints
  - Wafer-bonding trials with wafers from RD53/MPA 65 nm submission

Thanks to everyone who provided material for this talk!

Additional material

CLIC vertex-detector requirements



- efficient tagging of heavy quarks through precise determination of displaced vertices:

$$\sigma(d_0) = \sqrt{a^2 + b^2 \cdot \mathrm{GeV}^2/(p^2 \sin^3\theta)}$$

$$a \sim 5\ \mu m, \quad b \sim 15\ \mu m$$

  - → good single point resolution: $\sigma_{SP} \sim 3\ \mu m$
    - → small pixels <~25x25 μm², analog readout
  - → low material budget: X $\lessapprox$ 0.2% X_0 / layer
    - → corresponds to ~200 μm Si, including supports, cables, cooling
    - → low-power ASICs (~50 mW/cm²) + gas-flow cooling

- 20 ms gaps between bunch trains → trigger-less readout, pulsed powering
- B = 4 T → Lorentz angle becomes important

- few % maximum occupancy from beam-induced backgrounds → sets inner radius
- moderate radiation exposure (~10^4 below LHC!):
  - NIEL: < 10^{11} n_{eq}/cm²/y
  - TID: < 1 kGy / year

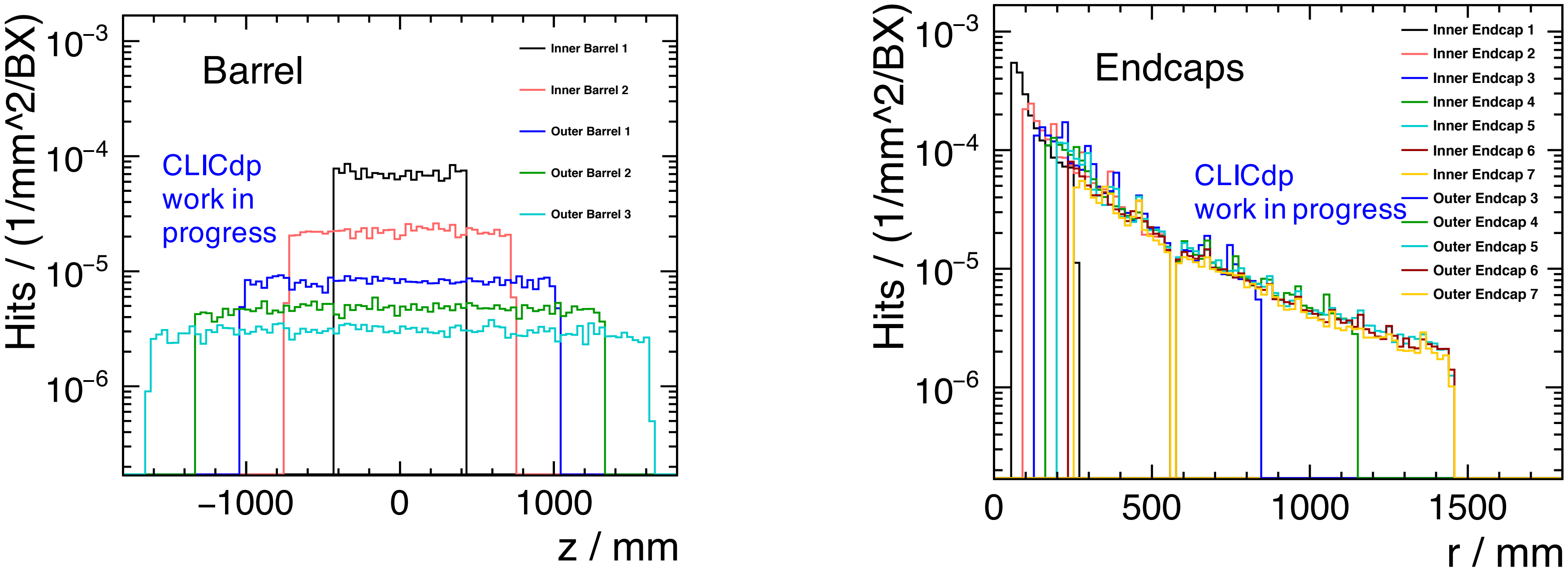
- Time stamping with ~10 ns accuracy, to reject background
  → depleted sensors (high resistivity / high voltage), readout with precise timing

CLIC tracker requirements

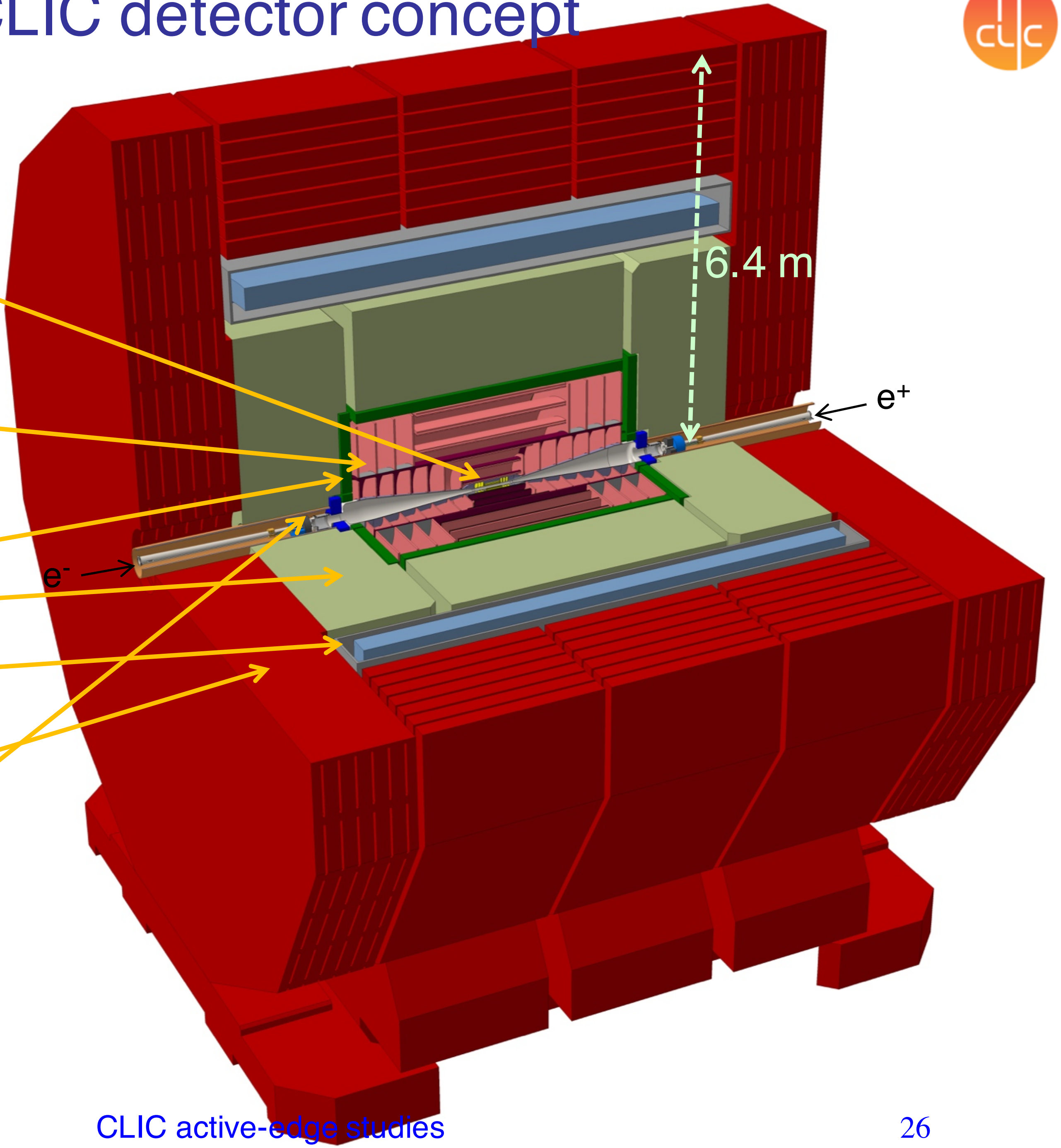
- Momentum resolution (Higgs recoil mass, H→μμ, BSM leptons):
  $\sigma(p_T) / p_T^2 \sim 2 \times 10^{-5}\ \mathrm{GeV}^{-1}$
  → 7 μm single-point resolution
  → ~1-2% X0 per layer (low-mass supports, cabling and cooling)

- few % maximum occupancy from beam-induced backgrounds
  → Time stamping with ~10 ns accuracy, to reject background
  → Readout granularity ~ 50 μm x 1-10 mm (t.b.c.: large pixels / small strips?)

Beam-induced background hits from γγ→hadrons and incoherent pairs:

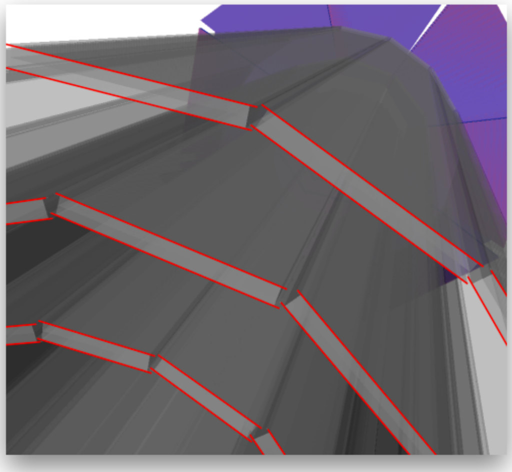


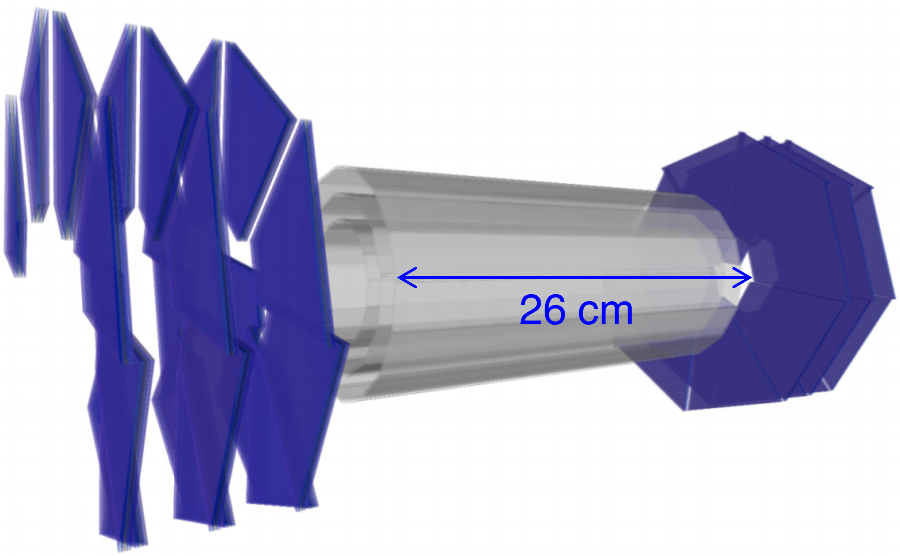
CLIC detector concept



- low-mass **vertex detector** with ~25x25 μm^2 pixels
- **silicon tracker**
- fine-grained **PFA calorimetry**, 1+7.5 Λ_i W-ECAL + Fe-HCAL
- 4 T **solenoid**
- **return yoke** with muon ID
- Complex instrumented **forward region**

Vertex detector layout



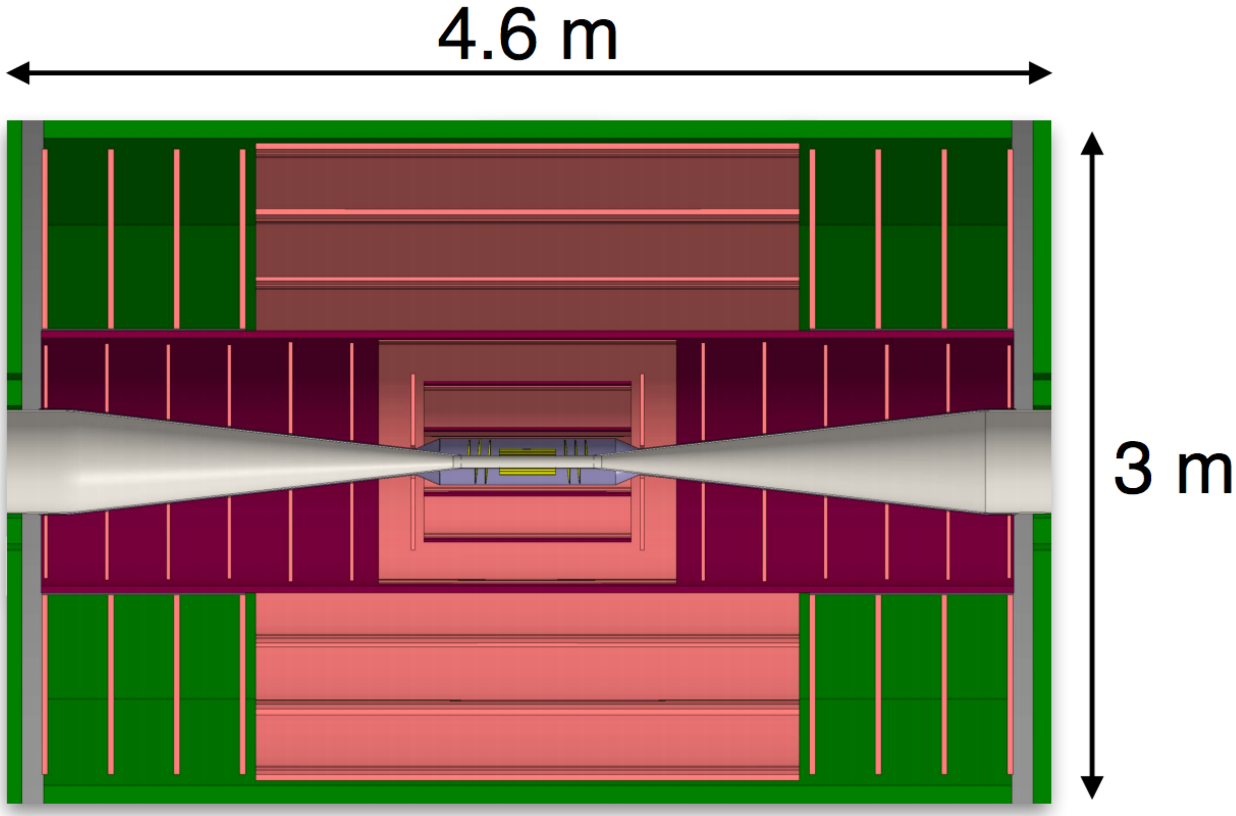


- Systematic optimization of geometries:
  - background occupancies
  - detector performance (flavor tagging, tracking resolution)
  - engineering constraints (cooling, powering, supports)

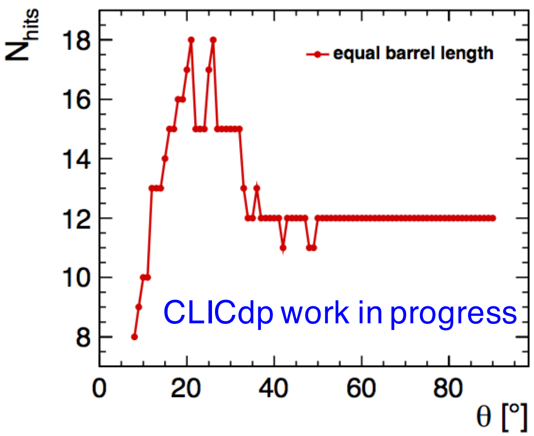
- Large coverage: $\theta > 7^o$ ($|\eta| < 2.8$)
- 3 double layers in barrel and endcaps
- 0.84 m^2 area, ~2G pixels (25 μm^2)
- $R_i \sim 30$ mm (background-occupancies)
- spiral endcap geometry (air flow cooling)

- Low material budget: 0.4%X_0 per double layer
- Single-point resolution ~3 µm

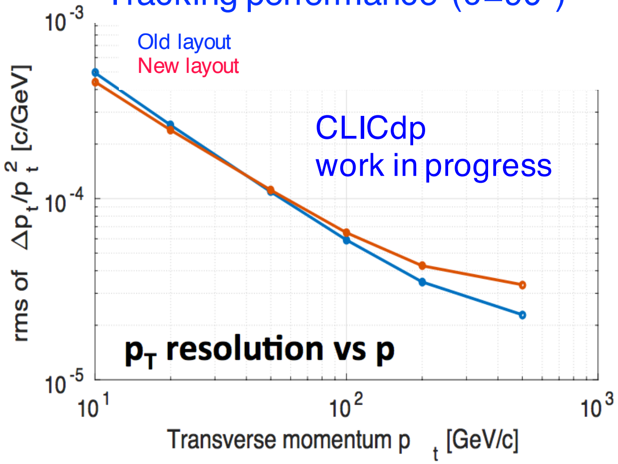
Outer tracking layout



coverage (vertex+tracker)

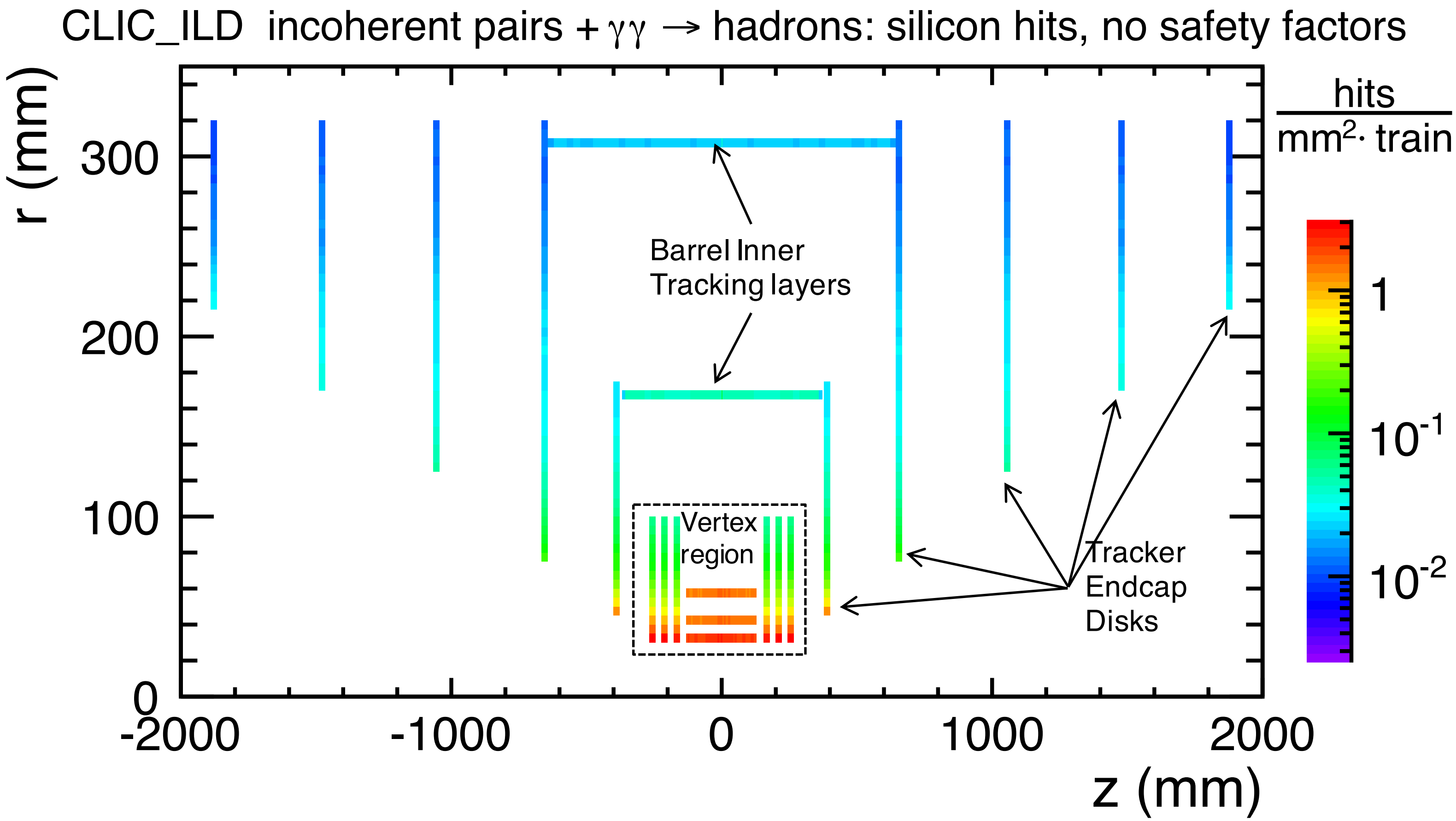


Tracking performance (θ=90°)



- Outer tracker:
  - 6 barrel, 7 forward layers, material budget 1-2%X_0 / layer
  - 90 m^2 silicon surface
  - >=8 hits for θ>8° (vertex+tracker)
  - Single-point resolution ~7 µm
  - beam pipes with conical sections (reduction of beam-induced backgrounds)
  - Layout optimized for tracking performance and backgrounds

Backgrounds in inner tracking region



CLIC_ILD incoherent pairs + γγ → hadrons: silicon hits, no safety factors

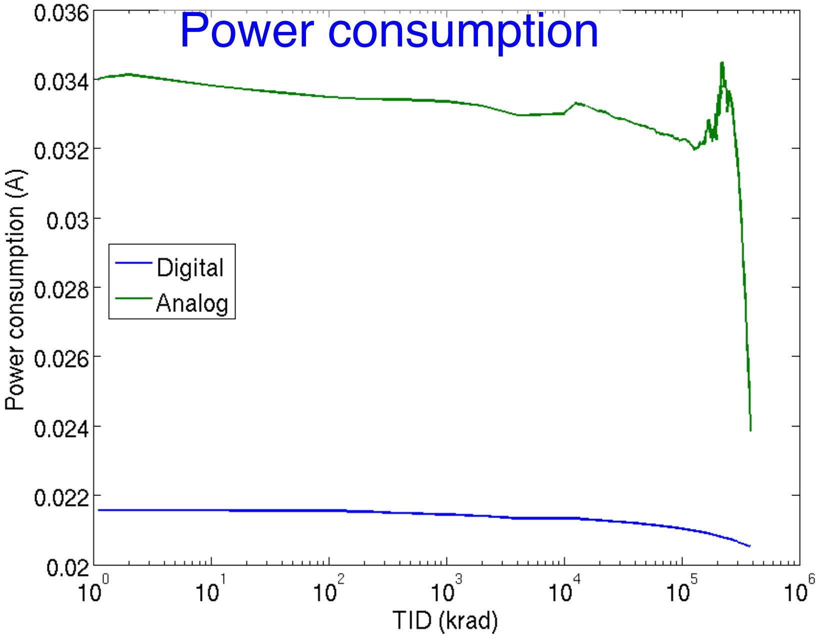
- Train occupancies up to 3% in vertex region (including clustering and safety factors)
- moderate radiation exposure, ~10^4 below LHC

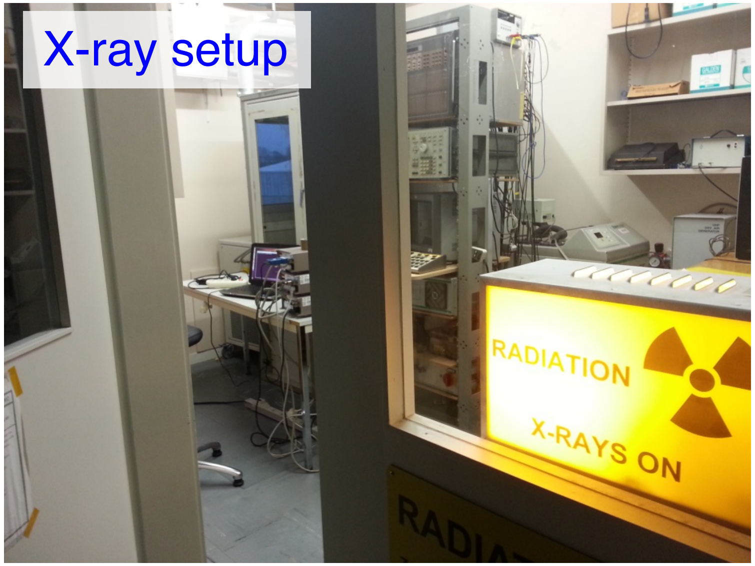
Region	Readout granularity	Max. occup.	NIEL [$n_{eq}/cm^2/y$]	TID [Rad/y]
VXB	20 µm x 20 µm	1.9 %	4×10^{10}	20k
VXEC	20 µm x 20 µm	2.8 %	5×10^{10}	18k
FTD pixels	20 µm x 20 µm	0.6%	2.5×10^{10}	5k
FTD strips	10 cm x 50 µm	290 %	1×10^{10}	700
SIT	9 cm x 50 µm	170 %	2×10^{9}	200

CLICpix: radiation qualification

- Moderate radiation-tolerance requirements at CLIC: <100 kRad TID
- However: building blocks can be re-used for RD53 (~1 GRad required)
- Results of radiation testing useful for gaining deeper understanding of the chip

→ performed radiation test up to 1 GRad (up to 150 kRad/minute) in calibrated X-ray setup





- No significant changes observed in sub-MRad range relevant for CLIC
- For >250 MRad: PMOS switches in current mirror fail

→ Break-down of analog power (note: band gap foreseen for final chip, instead of current mirror)

- digital components kept working normally

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