



## Status of WP6 Activities at KIT

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## Timeline/Status

- H35DEMO (CCPD)
  - 2cm x 2cm size sensor in AMS H35 process on high resistivity substrates
- LF\_ATLASPIX
  - LFA15 process on high resistivity substrates with 4 wells. Four monolithic matrices with total area of 1cm x 1cm.
- ATLASPIX and MUPIX sensors in AMS aH18 with total area of 2cm x 2cm

## Design overview

- CCPD and monolithic sensors
  - Readout types:
    - 1. Trigger-less (column drain)
    - 2. Triggered with parallel pixel to buffer connection (PPTB)
  - Pixel types:
    - 1. Smart diode pixel
    - 2. Small diode pixel

### Measurement results at a glance

- H35DEMO (Standalone)
- LF\_ATLASPIX and ALPHA monolithic sensors in LFA15 process













The H35Demo has four independent pixel matrices:

stand-alone nMOS matrix analog matrix A analog matrix B stand-alone CMOS matrix



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#### Monolithic detector

#### Capacitive coupled pixel detector - CCPD



Th = 1000 electrons

Efficiency [%]

102

100

98

96

94

92

90

88

86

0



- Test beam measurement at SPS (September-November 2016)
- > 99% detection efficiency has been measured with matrices
- > 99% of hits have timewalk less than 50ns



T. Weston et al.,

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"An overview of recent HV-CMOS results"

60

12th Trento Workshop on advanced Silicon Radiation Detectors

80





- The H35DEMO has the possibility to be read out as a monolithic sensor
- Histogram of the delay between trigger time stamp and sensor time stamp, measured on a pixel with a Time Walk Compensating Comparator for <sup>90</sup>Sr electrons. Two bins are occupied



0

40 60 80 100 120 140 160 Column

*Time resolution – difference between the time stamp and the* trigger moment



LF\_ATLASPIX





Project LF\_ATLASPIX Technology LFA15 (150nm) Substrates: 100, 500-1100, 1900, 3800 Ωcm 4-well HVCMOS process

Waveform sampling readout







Smart diode pixel in AMS H18 and all LFA15 sensors

Small diode pixel in LFA15





- Left: Column drain readout
- Right: Parallel pixel to buffer readout







- 1. Amplifier output in response to <sup>90</sup> Sr source
- 2. Test of the trigger readout
- 3. Threshold scan of full matrix





MUPIX/ATLASPIX



Project MUPIX/ATLASPIX Technology AMS aH18 (180nm) Substrates: 20, 50-100, 100-400, 600-1100 Ωcm 4-well HVCMOS process



2.3cm



MUPIX/ATLASPIX







MUPIX/ATLASPIX



Pixel size (um)

33x125	25x50	25x25	25x25
80x81 "HVMAPS"	50x60 "M"	0 40x128 "Simple	5 40x125 e" "IsoSimple"

MuPix8, ATLASPIX







MuPix8, all AMS H18 sensors except "IsoSimple"



#### IsoSimple in AMS aH18 and all LFA15 sensors





- Large scale (2cm x 2cm) HVCMOS sensors in AMS 350nm technology produced and tested
- The sensor is implemented of 4 different substrate materials, it contains various tests structures and can be attached (capacitively or with bumps) and readout by FEI4. Monolithic readout is also possible. The sensor can be used for development of interconnection technology. Test beams and irradiations are planned
- Various designs in LFoundry 150nm process have been submitted
- Sensors produced in LFoundry LFA 150 nm process are working. Parallel-Pixel-to-Buffer (PPtB) Readout Principle is working. Triggered Readout is working with an accuracy of the order of 20 ns
- Monolithic and CCPD designs have been submitted in AMS aH18 (180nm) process. Expected tape out by end of April 2017.





## THANK YOU !

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## **BACK UP**

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PCBs, FPGA firmware and software developed at IFAE







- 1) Hit driven, trigerless, readout (MuPix8, Simple ATLASPix)
- 2) Triggered ReadOut (ATLAS\_M2)



- priority circuit and bus
- All data will be sent in ascending order from pixels
  - without external trigger
  - Advantage: simple and small bus



- 16 pixels have 4 buffers
- pixel to buffer connection: parallel bus
  - trigger signal
  - Advantage: faster data transmission



## AIDA<sup>2020</sup> Structure of MuPix8











# AIDA<sup>2020</sup> The Digital Readout Concept







pixel blocks

buffer blocks







Fig. 22: Histogram of the delay between trigger time stamp and sensor time stamp, measured on a pixel without time walk compensation for <sup>90</sup>Sr electrons. Five bins are occupied.



Fig. 23: Histogram of the delay between trigger time stamp and sensor time stamp, measured on a pixel with a Time Walk Compensating Comparator for <sup>90</sup>Sr electrons. Two bins are occupied.