Latest news from big demonstrator designs and tests in LF technology

(report from Bonn, CPPM, IRFU, KIT collaboration)

A.Rozanov

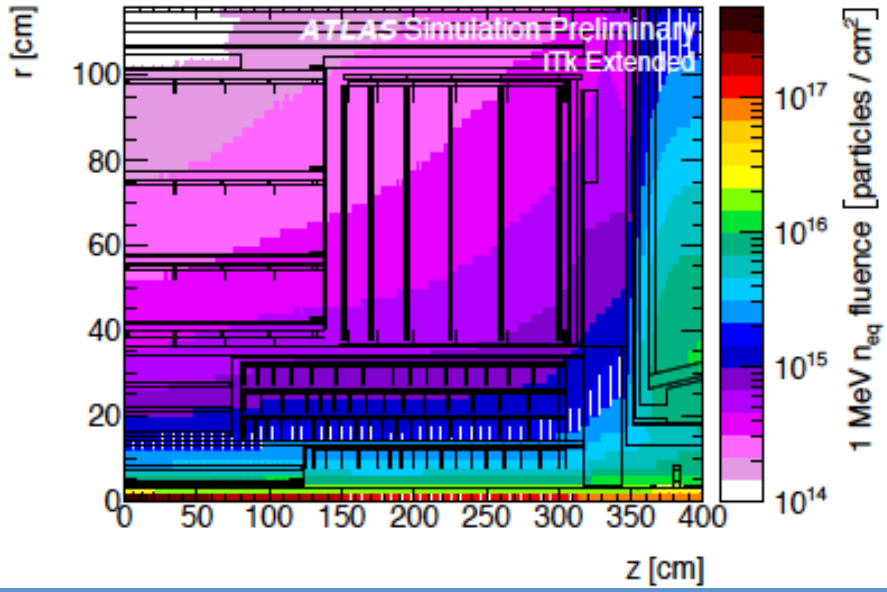
5.04.2017

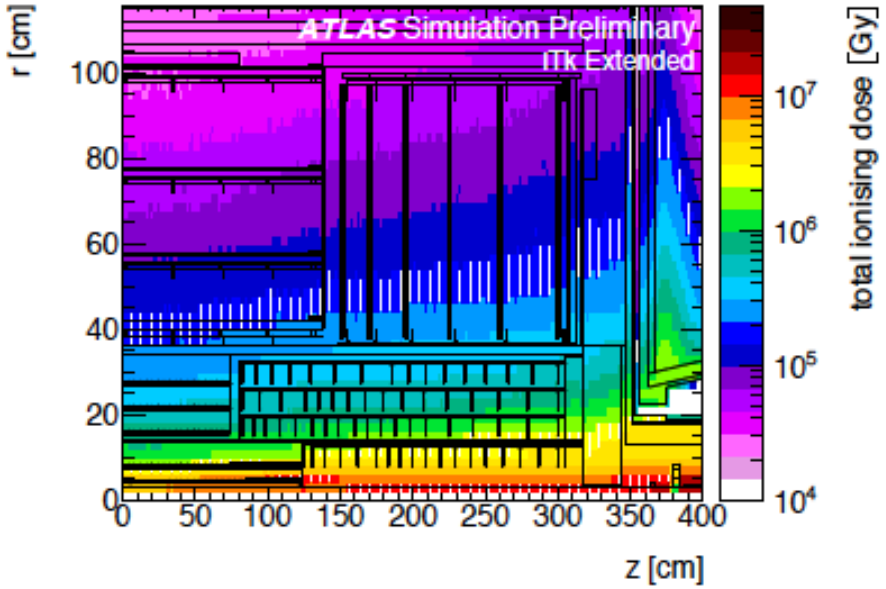
Collaboration

- University of Bonn I. Caicedo, T.Hirono, T.Hemperek, F.Hugging, H.Kruger, P.Rymaszevski, T.Wang, N.Wermes
- CPPM M.Barbero, P.Breugnon, S.Godiot, J.Liu, P.Pangaud, A.Rozanov
- KIT I. Peric
- IRFU CEA Y.Degerli, F.Guilloux, P.Schwemling, C. Guyot, J.-P. Meyer, A. Ouraou, M.Lachkar, M. Vandenbroucke

HL-LHC application

- After the Phase II upgrade ~2026
- The HL-LHC will operate at a ultimate leveled instantaneous luminosity of $7.5\times10^{34}cm^{-2}s^{-1}$.
- Total pixel silicon area of ATLAS Inner Tracker (ITk) is ~8.2m^2.
- L1 trigger rate 1 MHz, minimal latency 6 us , pileup 200 events



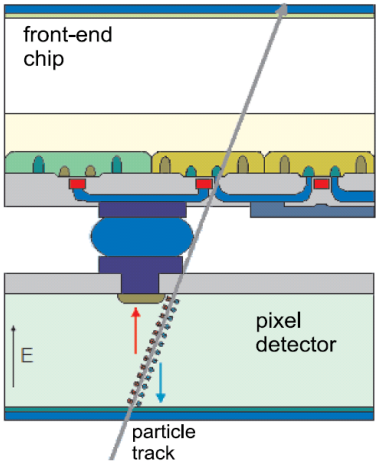


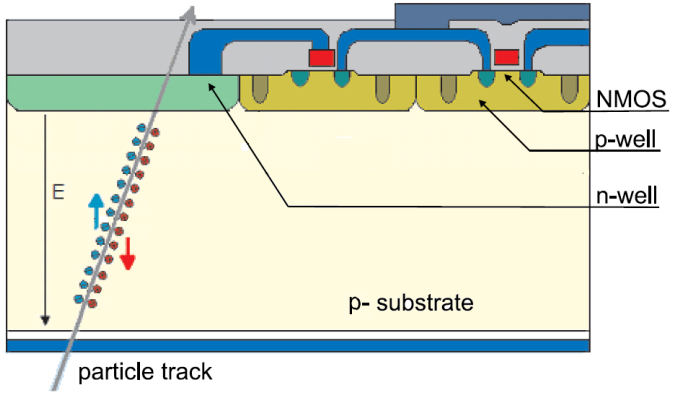
Fluence (safety factor 1.5) at the inner most pixel layer R=3.9 cm (exchangeable), for an integrated luminosity of 3000 fb^{-1} over 10 years:
NIEL: ~2.25×10^{16} n_{eq} cm^{-2}
TID: ~1710 MRads

Fluence at the outer most pixel layer R=27.1 cm, for an integrated luminosity of 3000 fb^{-1} over 10 years:
NIEL: ~1.2×10^{15} n_{eq} cm^{-2}
TID: ~61 MRads

Presently, the default option for upgrade is to use a hybrid pixel detector concept:
- Sensor: thin 100-150 um silicon planar or 3D
- Readout-Out Chip: deep-submicron rad-hard ICs (65nm), high granularity 50x50 um pitch

HV-HR CMOS for Phase-II Upgrade

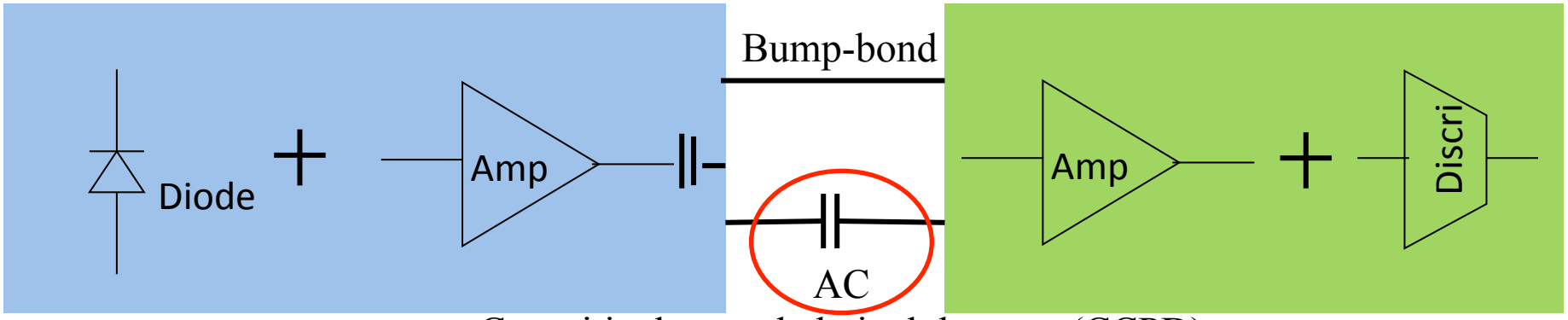




- Commercial CMOS technology → low price
- Thinned chips → material budget reduced
- Pixel size reduced → better resolution and two track separation
- Capacitively coupled CMOS chip →Option to glue (or bump bond) CMOS chip on standard digital chip (FE-I4 or FE-RD53)
- Use case for inner pixels: 25x25 um pixel size with inpixel encoding readout by FE-RD53
- Use case for outer layers: full monolithic chip, low price, fast and easy module production, pixel pitch not critical

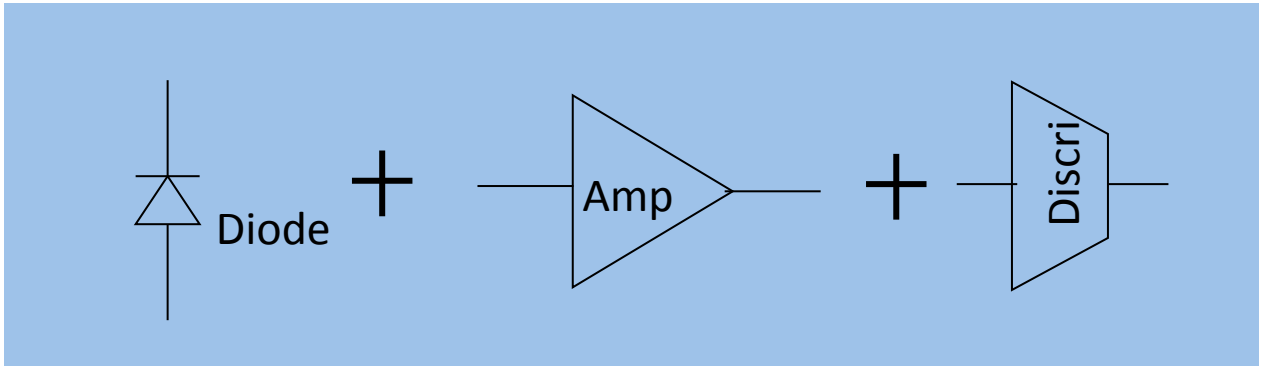
HV/HR CMOS architectures

Sensor capacitively coupled (or bump bonded) to digital IC:

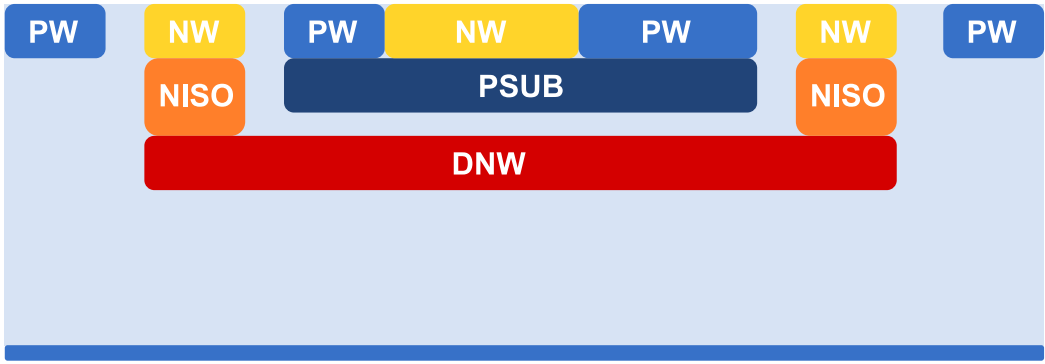


Capacitively coupled pixel detector (CCPD)

Monolithic (depleted CMOS pixel chips including the R/O architecture on-chip):



LFOUNDRY Technology and projects



LFoundry CMOS technology:

- 150nm CMOS (Avezzano, Italy)
- 2kΩcm p-type bulk
- Deep NWell available
- HV process
- Thinning and back size metallization possible, up to 7 metal layers, 8”
- MLM3 (multi-layer-mask) (25.840mm x 9.505mm)

LFoundry Projects

- CCPD-LF VA chip : 5 x 5 mm² (Bonn, CPPM,KIT) submitted july 2015
- CCPD-LF VB chip : 5 x 5 mm² (Bonn, CPPM,KIT) submitted july 2015
- LFCPIX V1 chip : 10 x 10 mm² (Bonn, CPPM, IRFU) submitted Feb 2016
- LFCPIX V2 chip : 10 x 10 mm² (Bonn, CPPM, IRFU) submitted Feb 2016
- LF_MONOPIX_01 chip : 10 x 10 mm² (Bonn, CPPM, IRFU) submission Sept 2016

LFOUNDRY development line

CCPD_LF (PROTO)

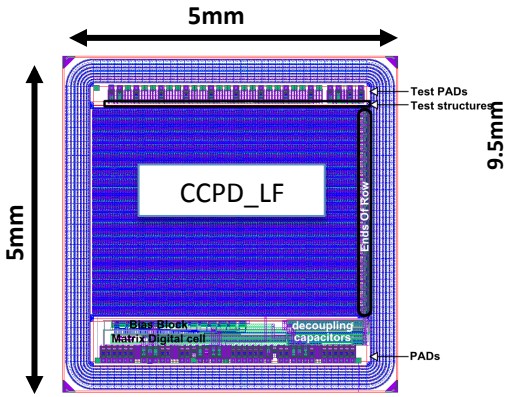
- Subm. in Sep. 2014
- 33 x 125 µm^2 pixels
- **Fast R/O coupled to FE-I4**
- Standalone R/O for test
- ***(Almost) Fully characterized***

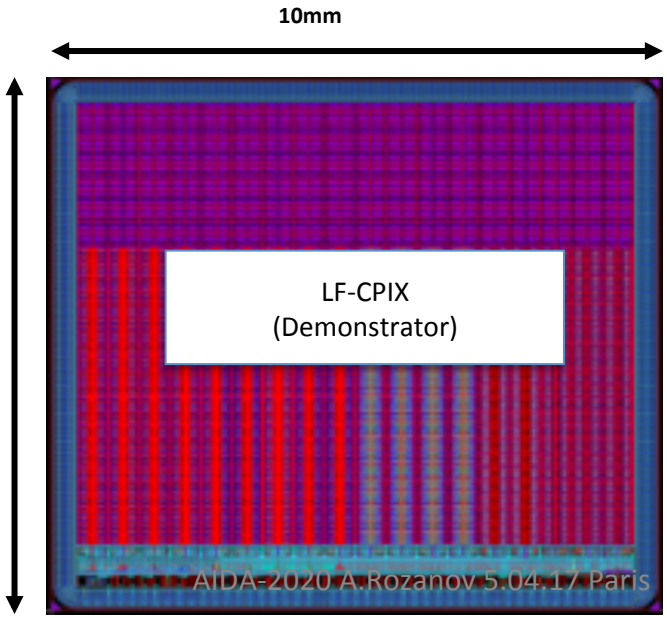
LF-CPIX (DEMO)

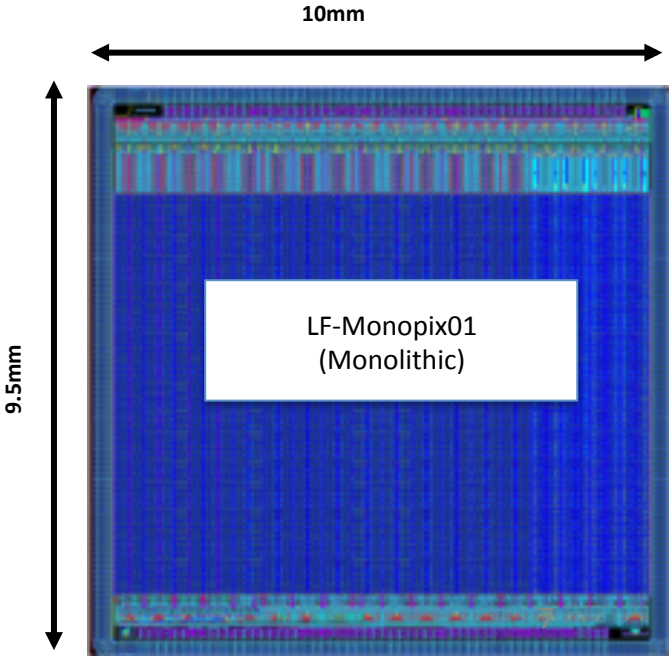
- Subm. in Mar. 2016
- ***CPIX demonstrator in LF***
- 50 x 250 µm^2 pixels
- 34 col of 168 pixels
- **Fast R/O coupled to FE-I4**
- Standalone R/O for test
- ***Many meas. available***

LF-Monopix01 (monolithic)

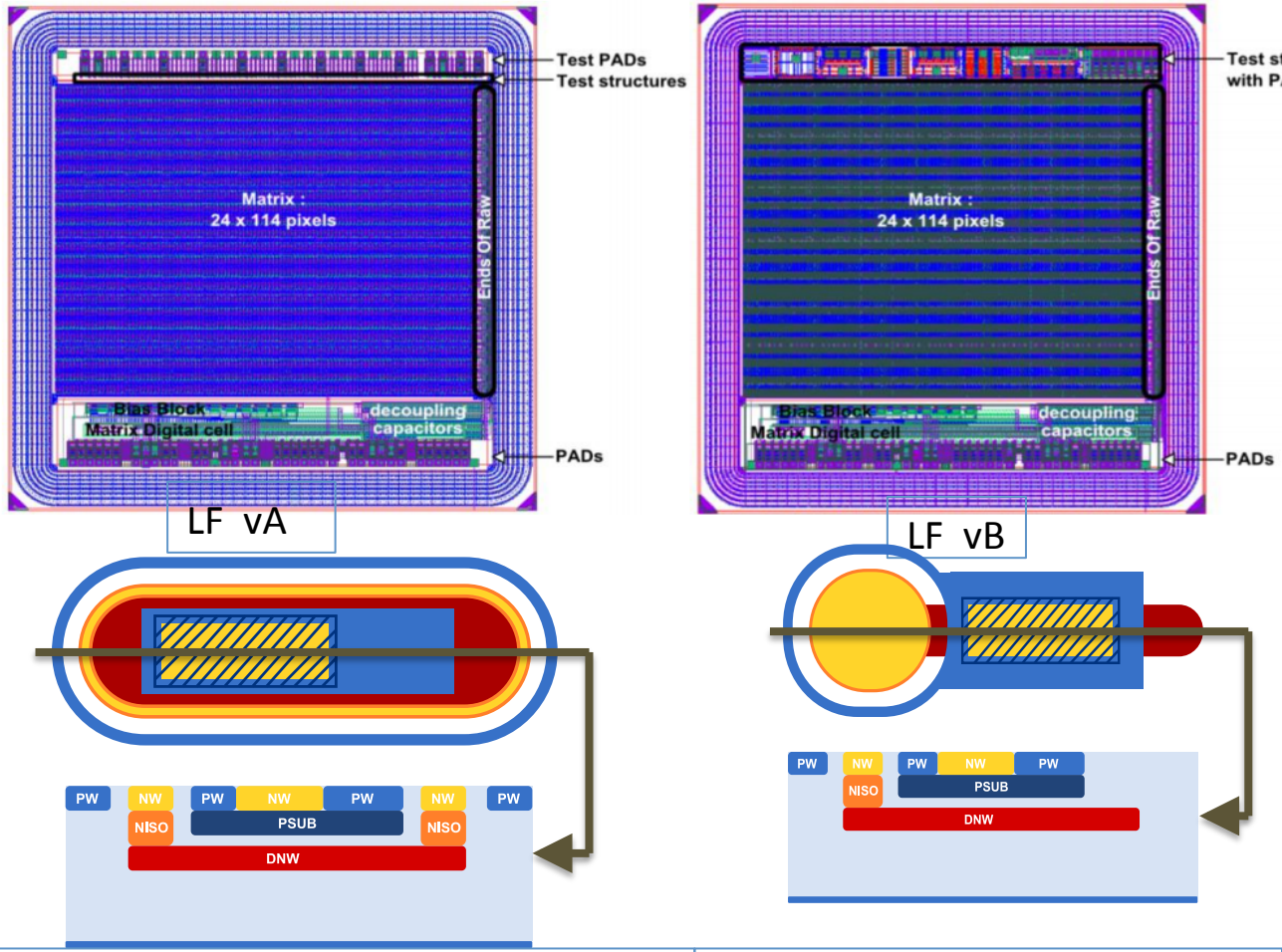
- Subm. in Aug. 2016
- "Demonstrator size"
- 50 x 250 µm^2 pixels
- 142x36 pixel matrix
- ***Fast standalone R/O***
- Standalone R/O like LF-CPIX
- **Just started measurements**

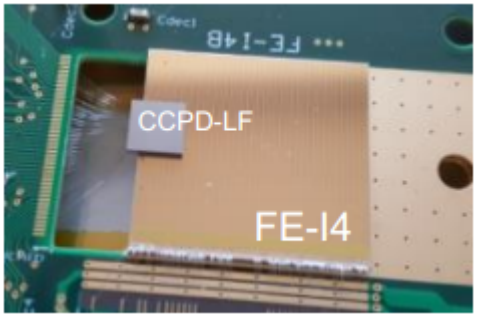






CCPD-LF 150 nm prototype in 2015





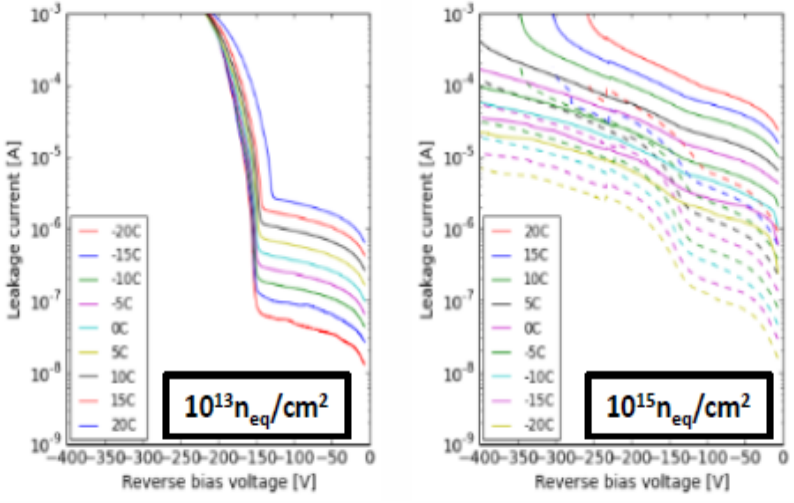
- Chip size is 5mm×5mm, 114x24=2736 pixels
- Pixel size is 33umx125um
- Test transistors are implemented in vA
- Test sensors and analog buffer are implemented in vB.

Version A sensor:
Larger DNW, larger input capacitance, electronics isolated with HV.

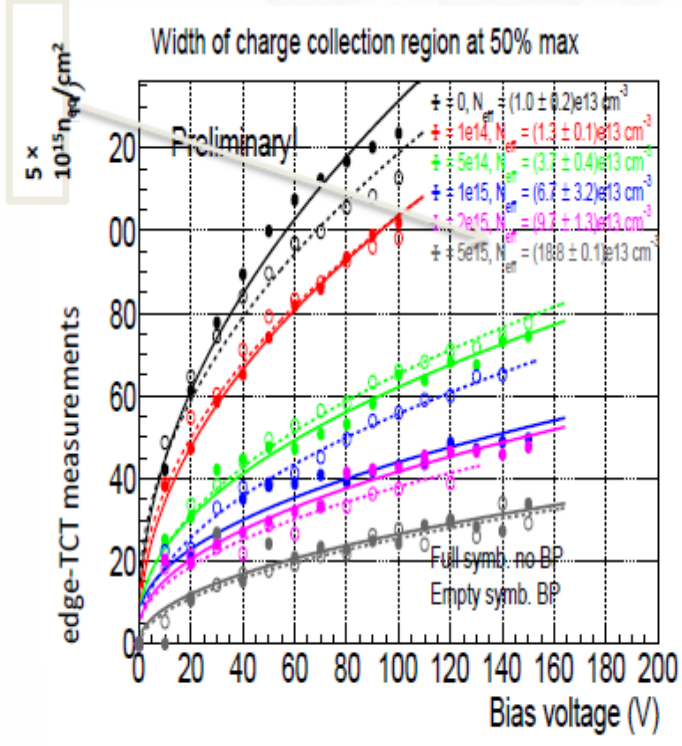
Version B sensor:
Smaller DNW, smaller input capacitance.

CCPD_LF: neutron irradiation performance

Sensor leakage current

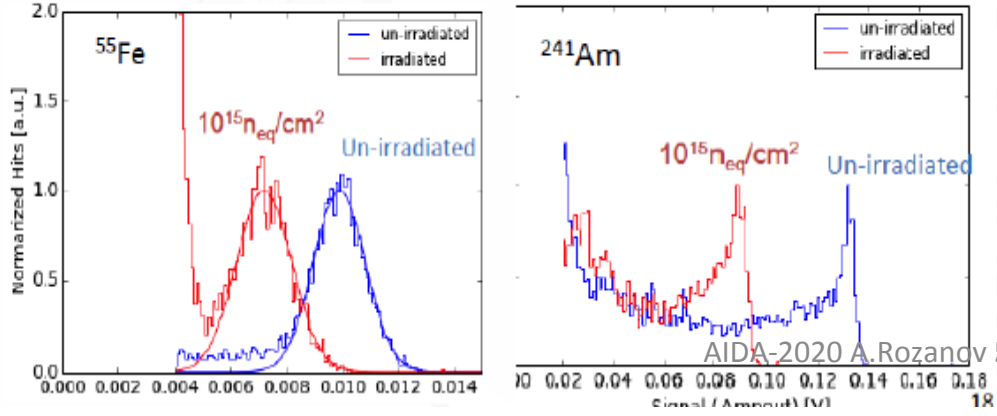


Non-ionizing fluence (NIEL)
eTCT measurements



I. Mandic, B. Hiti (Ljubljana)

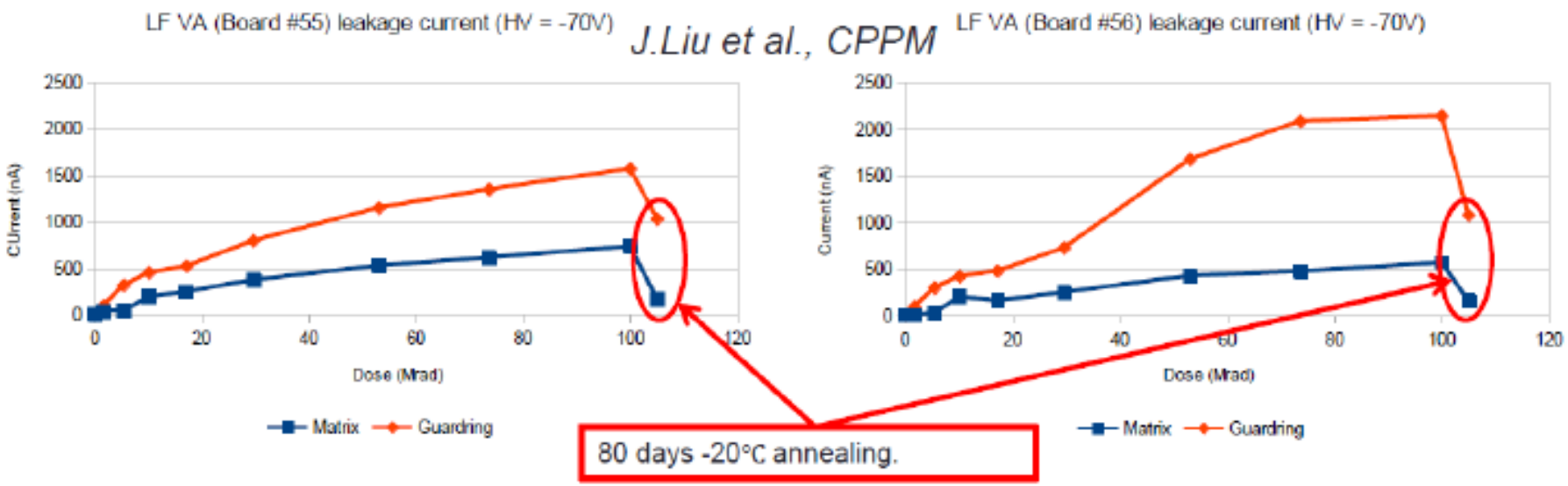
Spectra: ^{55}Fe and ^{241}Am after $10^{15}n_{eq}/cm^2$ (bias 100V/125 V)



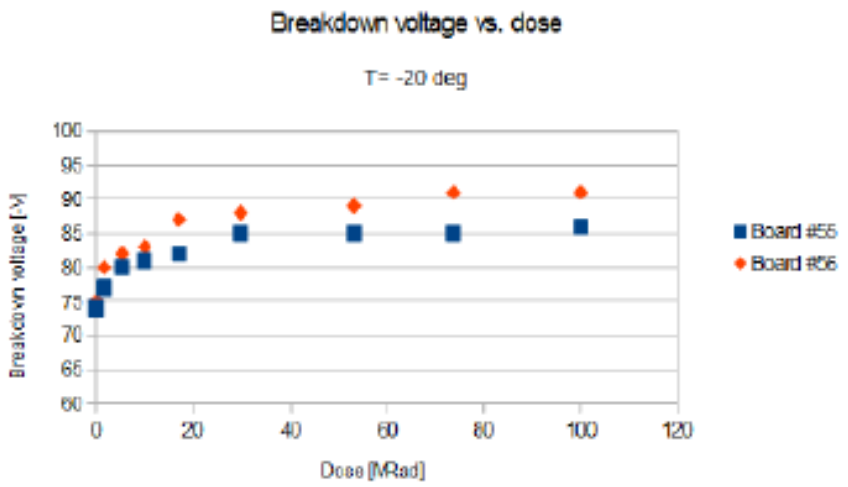
o(50µm) depletion after 10^{15} n_{eq}/cm^2

T.Hirono (Bonn)

CCPD-LF irradiated to 100 MRads protons



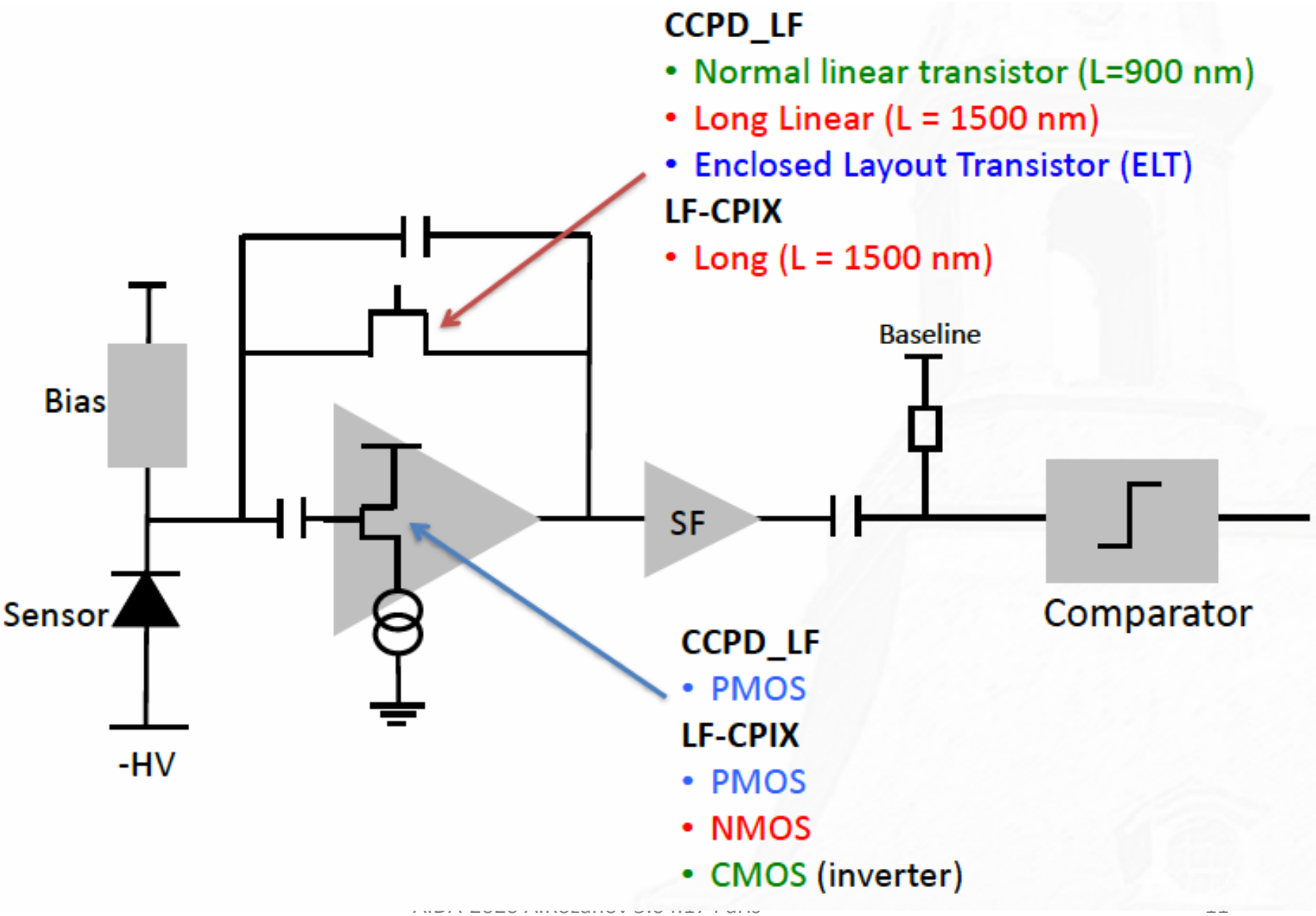
Leakage current reduced approximately by factor of 50, after annealing period.



Unusually, the Break Down voltage limit increases with the dose level.

AIDA 2020

Study of the different options of transistors



CCPD_LF : Gain and noise after irradiation

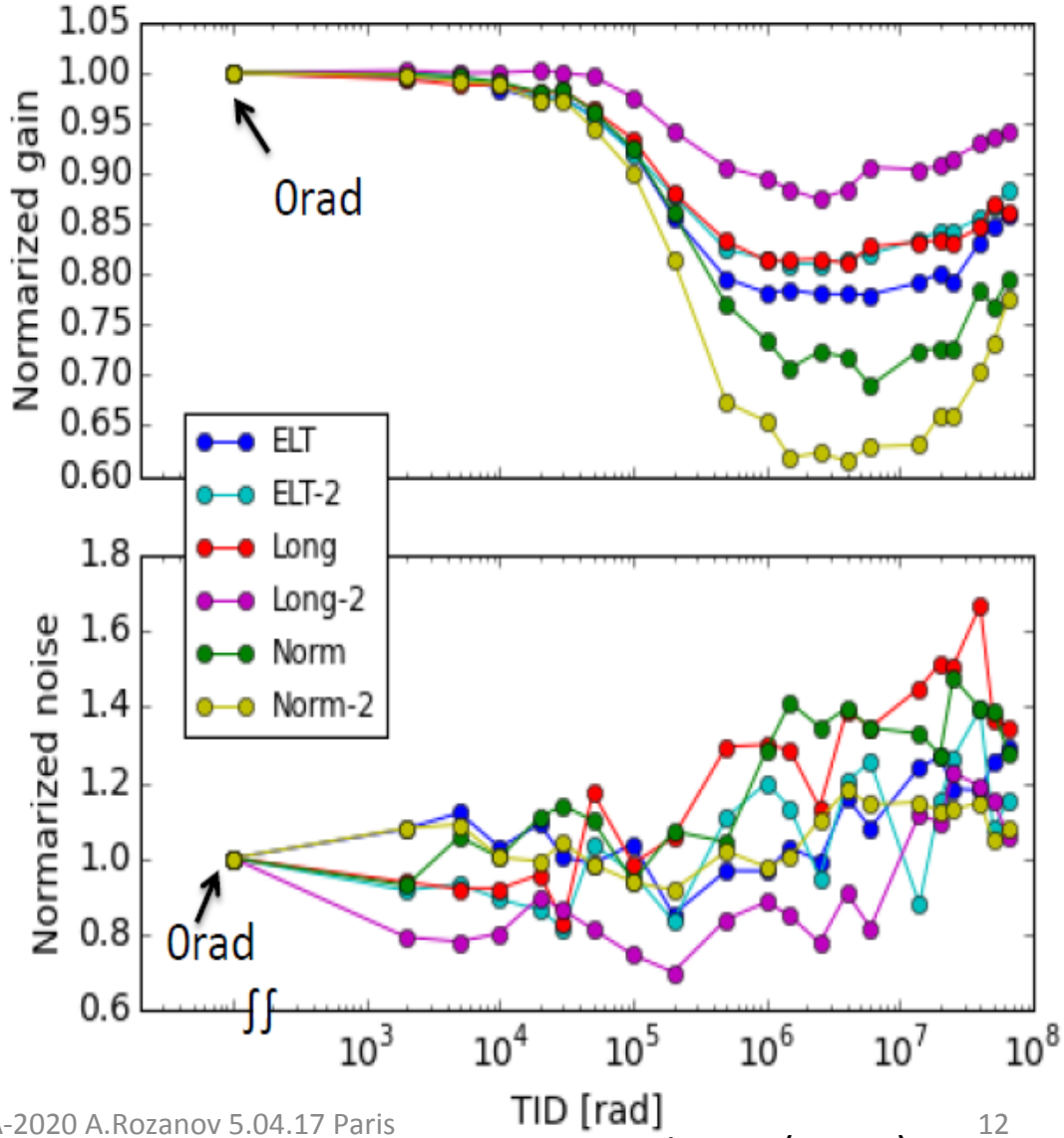
CCPD_LF

- Feed back transistor
  - Linear transistor (Norm)
  - Long linear transistor
  - ELT
- 2 pixels from each flavor
- Bias voltage: -100V

- Gain degradation: 60% - 90%
- Noise increase: 50%

The degradation of “Long” is smallest (but its size is largest)

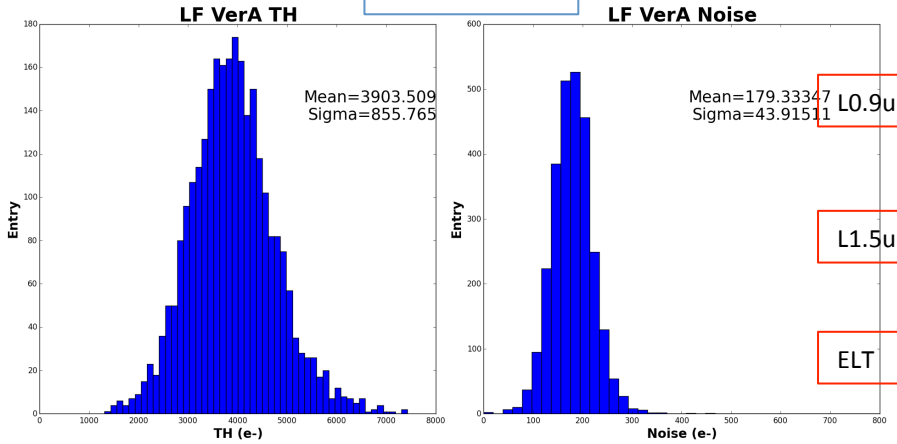
Difference between pixels in the same flavor is not small



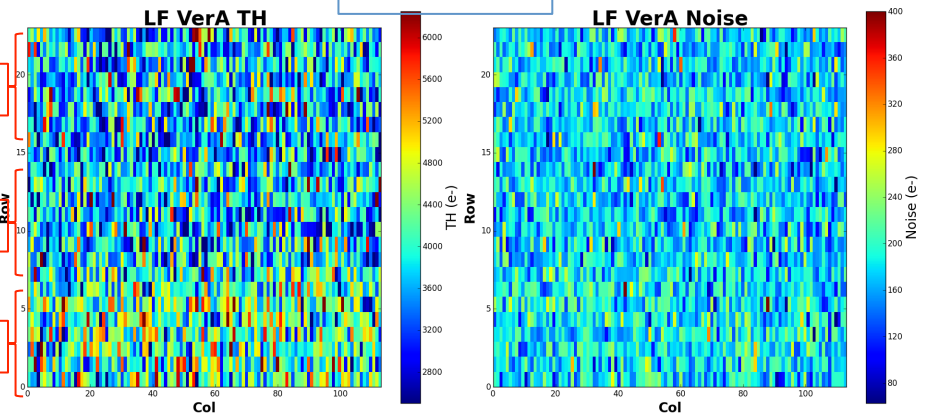
T.Hirono (Bonn)

CCPD_LF VA under protons: analog scan at -20 ℃

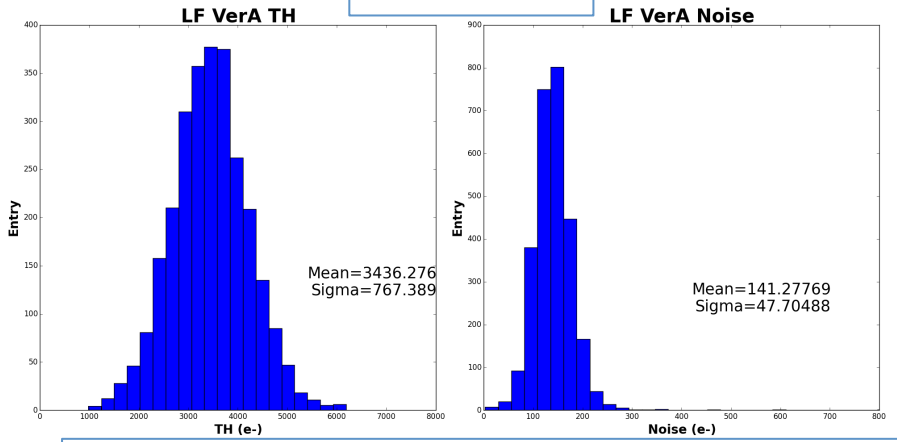
5 MRads



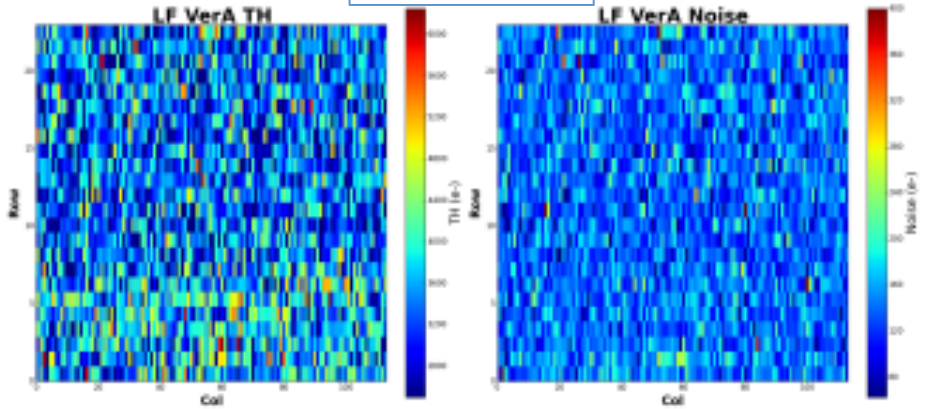
5 MRads



100 MRads

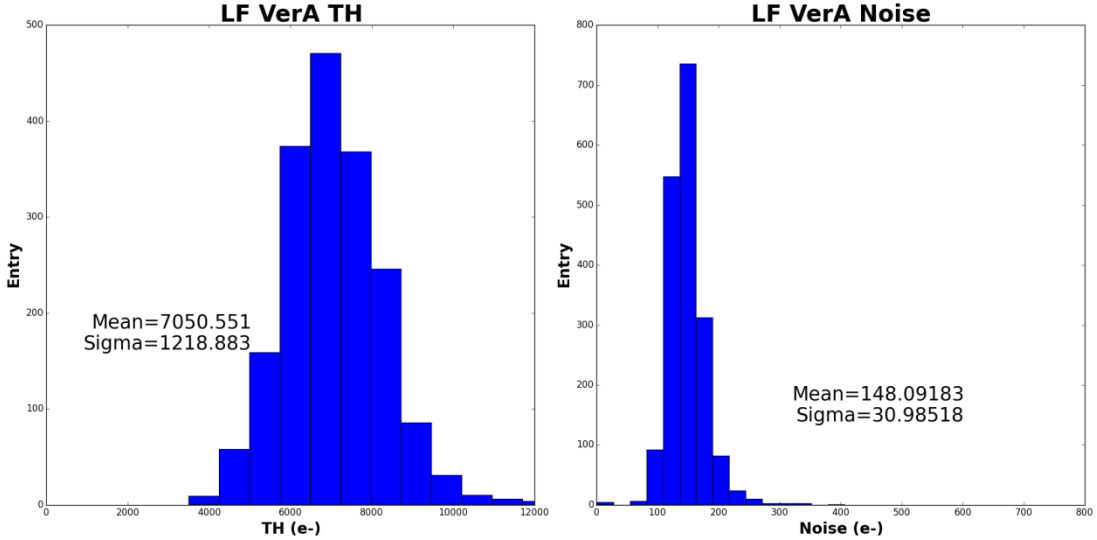


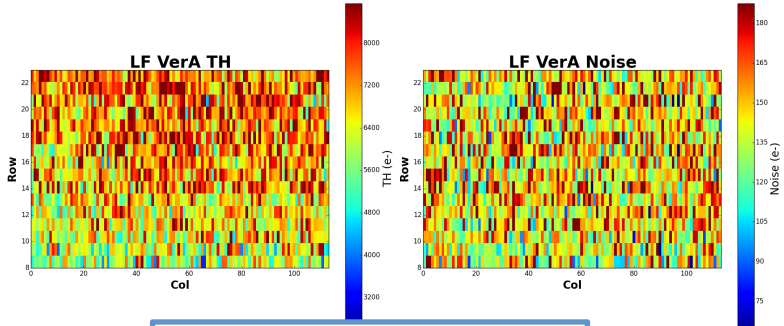
100 MRads



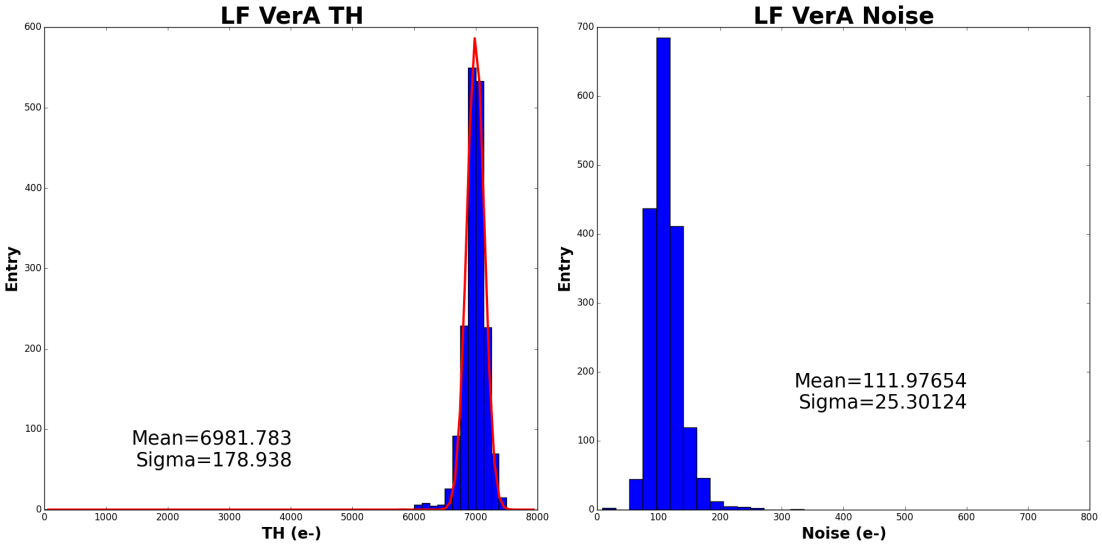
Both the threshold and noise reduced after 100 MRad. The ELT pixels have bigger threshold level than linear feedback pixels.

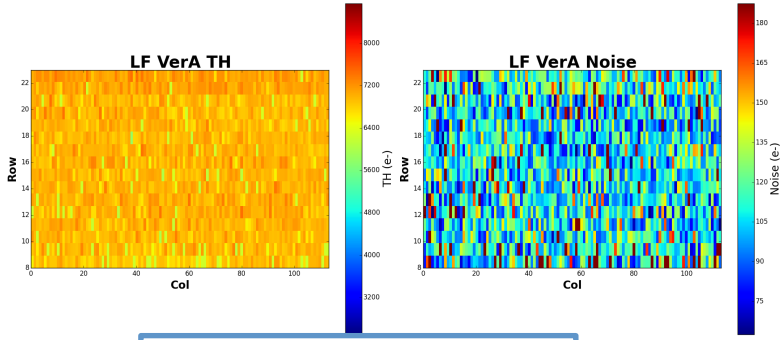
CCPD_LF VA: tuning of LIN feedback pixels





Scan
LSBdacL=63, TDAC=7
TH=0.80V, BL=0.75V

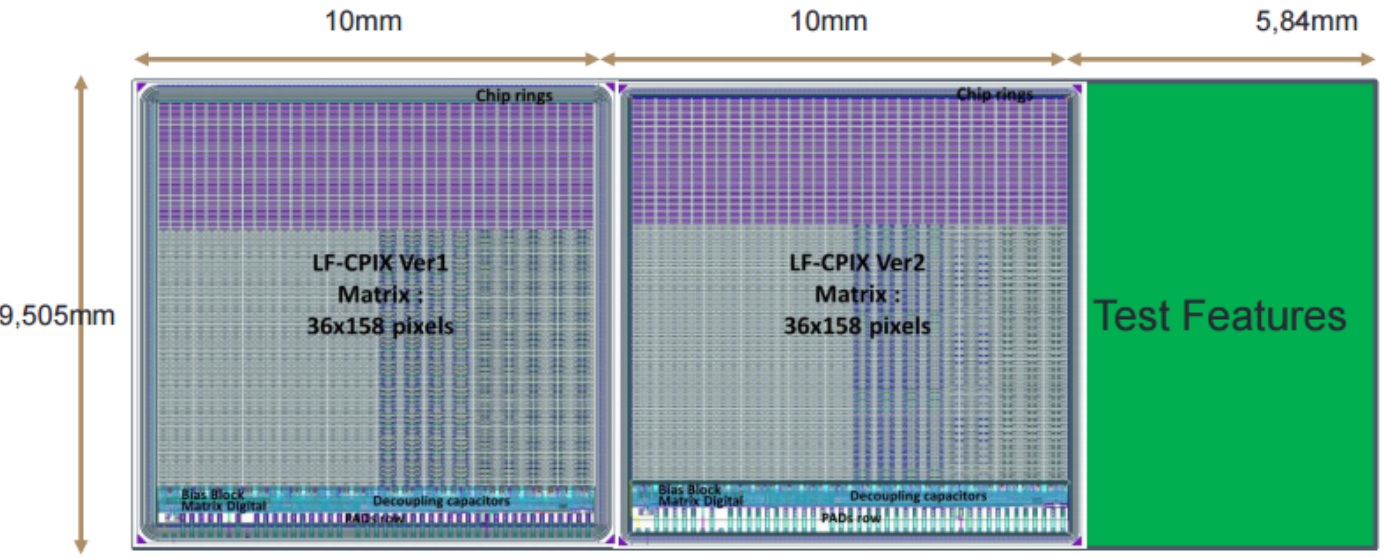


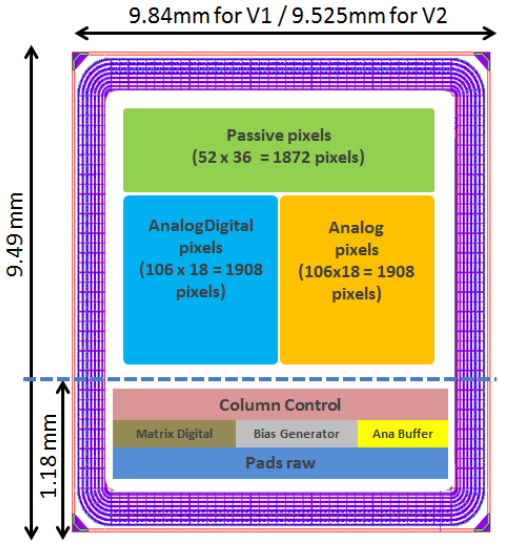


Tuning
LSBdacL=63
TH=0.80V, BL=0.75V

56 pixels (3.1%) were masked.

LF CPIX demonstrator





Designed by

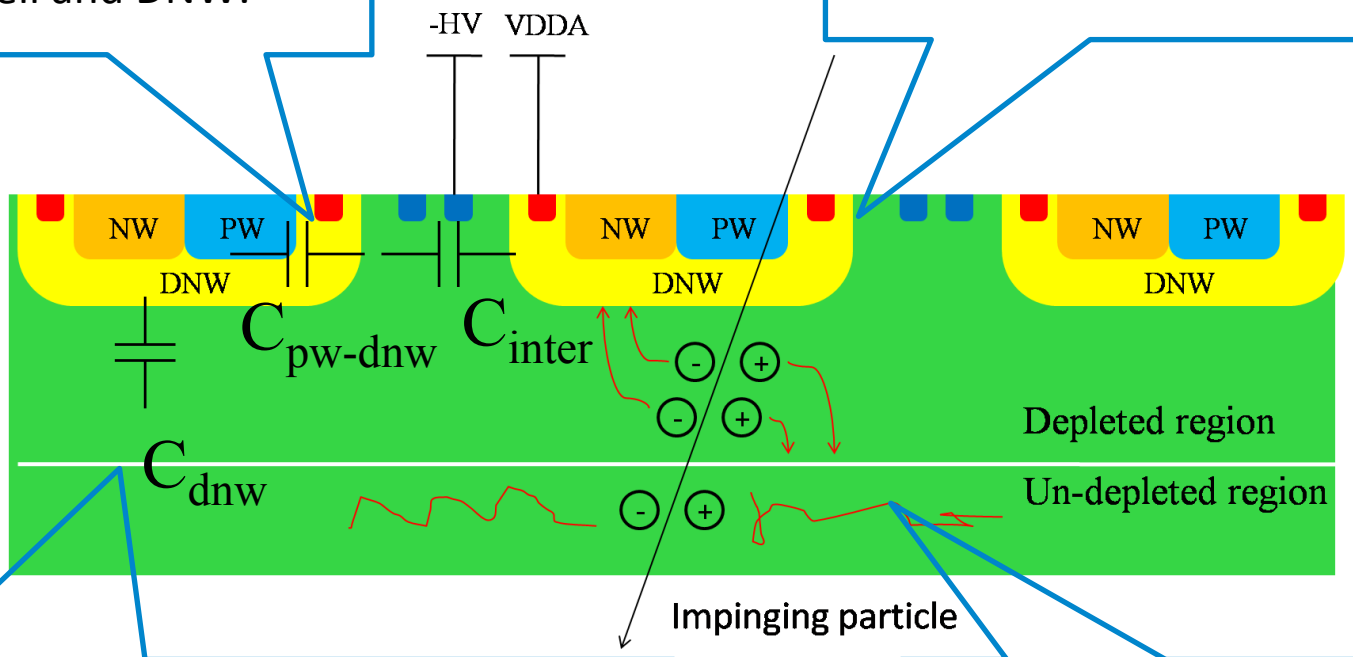
Y. Degerli, S. Godiot, T. Hemperek, H. Krueger, J. Liu, P. Pangaud, P. Rymaszewski, T.Wang

- New large demonstrator LF CPIX was submitted on March 2016:
  - Pixel size 250 µm × 50 µm (FE-I4 like).
  - Consists of three pixel flavors: passive, digital and analog pixel. Some improvements have been brought to them with respect to the characterizations of the LF CCPD prototypes.
  - New guard-ring strategy in LF CPIX Ver2 to increase the breakdown voltage and reduce the inactive region.

What we have done by using TCAD

AC: Input capacitance from the Pwell and DNW.

DC: Breakdown voltage in the critical region.



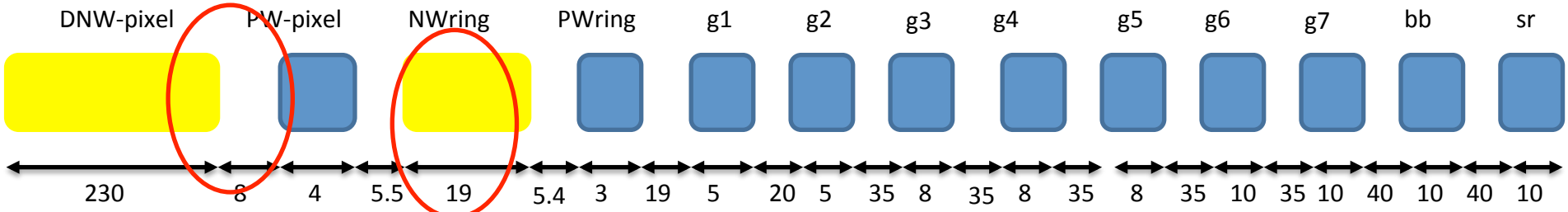
DC: Depletion evaluation depending on the biasing voltage and the resistivity.

DC: Leakage current.

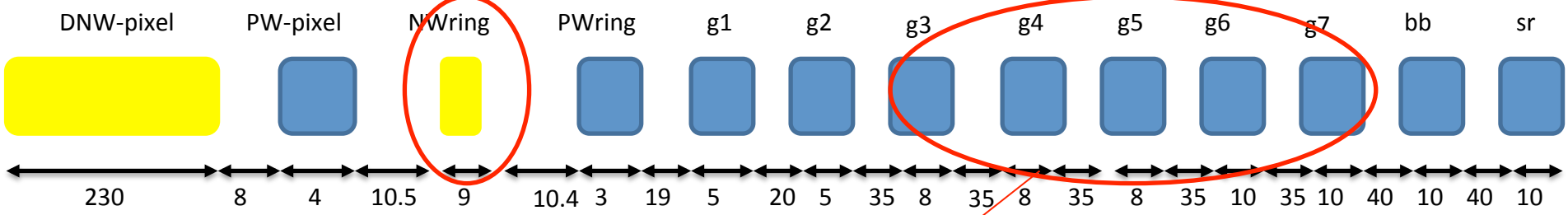
Transient: Charge collection behavior.

Guard-ring strategy of LF CPIX V2

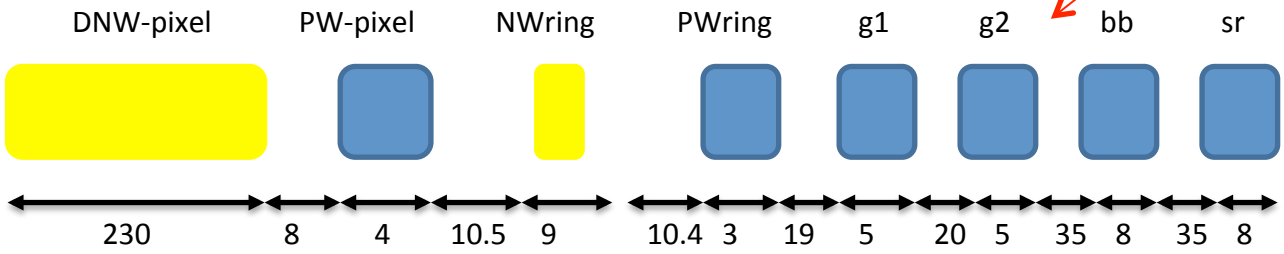
(A) Default: The same size as LF CPIX V1 except for the distance between DNW-pixel and PW-pixel.



(B) Shrunk Nwellring: increase the distance between Nwellring and its neighbor PWs to improve breakdown voltage.



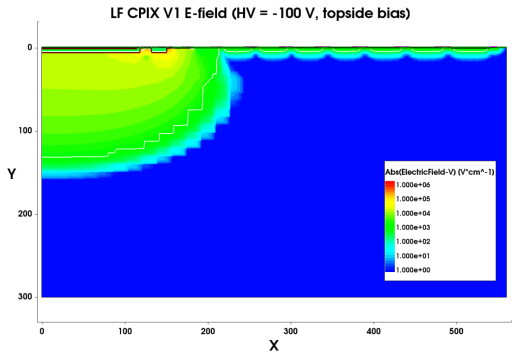
(C) Shrunk Nwellring + reduced guardrings: has enough space to avoid the depleted region touching the cutting edge.

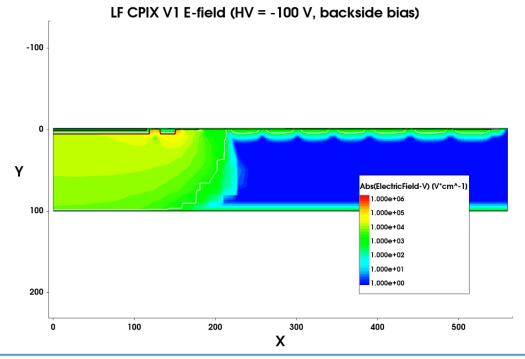


3 scenarios were under simulating. Top side bias with 300um thickness. Backside bias with 100um thickness.
Topside bias: PW-pixel, bb and sr connected to –HV, DNW-pixel and NWring to VDDA, others floating.
Backside bias: backplane connected to –HV, DNW-pixel and NWring to VDDA, others floating.

Depletion and e-field of LF CPIX V1 and V2

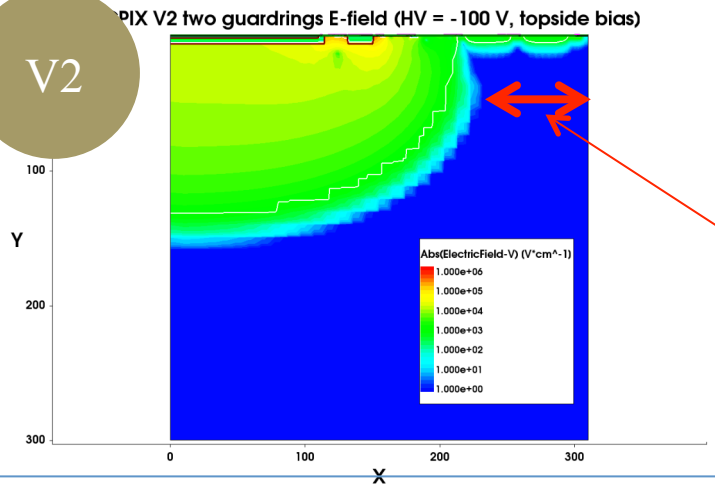
V1

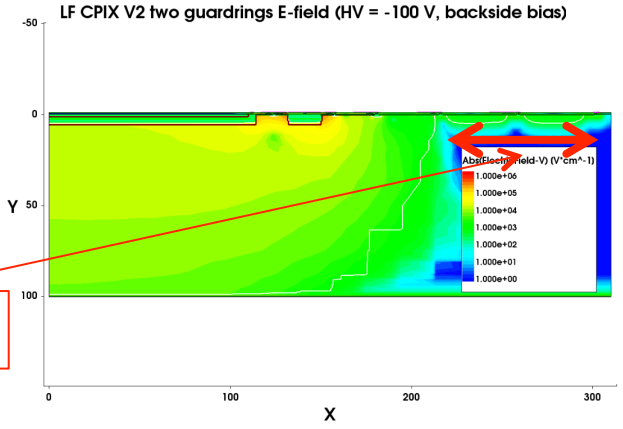




Big un-depleted area between depleted edge and cutting edge → guard-ring reducing is possible → reduced dead region.

V2



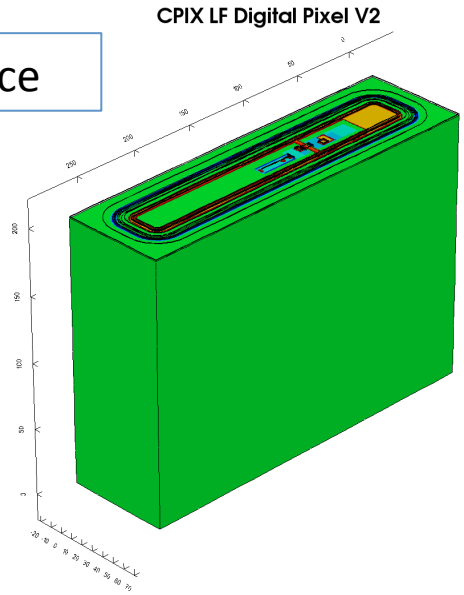


~100 µm

Pwellring + 2 floating guard-rings + backbias + seal-ring.
The depleted region can not reach the chip edge even with removed 5 outer guard-rings.
Break down voltage changed from 90 to 170 V.

AC simulation for LF CPIX

3D device

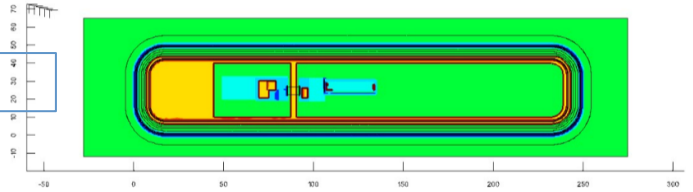


LF 150 nm technology
Pixel size: 50 µm x 250 µm
Substrate resistivity: $2k\Omega \cdot cm$
Substrate thickness: 200 µm

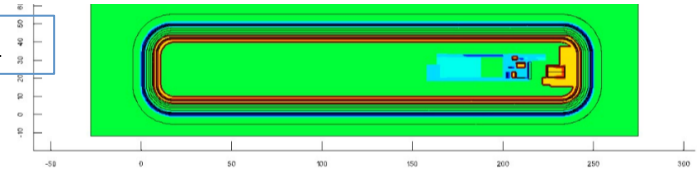
Distance between DNW and guard-ring of V1: 4.86 µm.
DNW size of V1: 237 µm x 37 µm

Distance between DNW and guard-ring of V2: 8 µm.
DNW size of V2: 230 µm x 30 µm

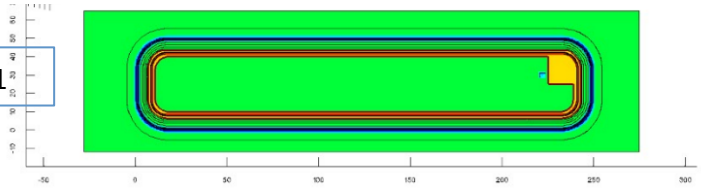
Digital pixel V1



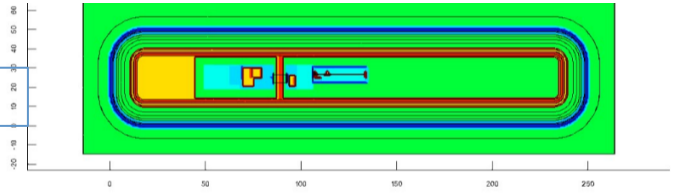
Analog pixel V1



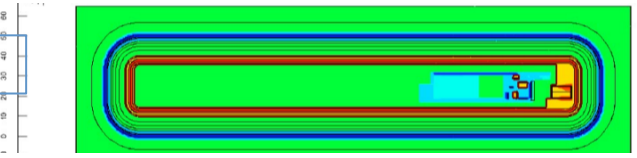
Passive pixel V1



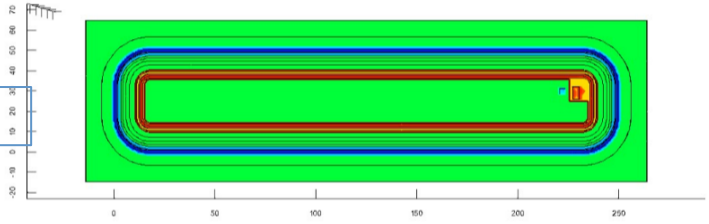
Digital pixel V2



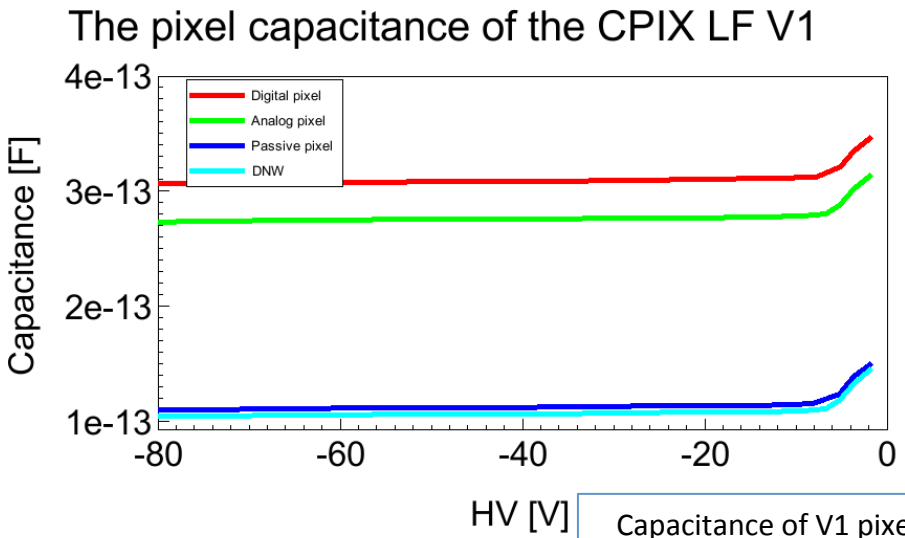
Analog pixel V2

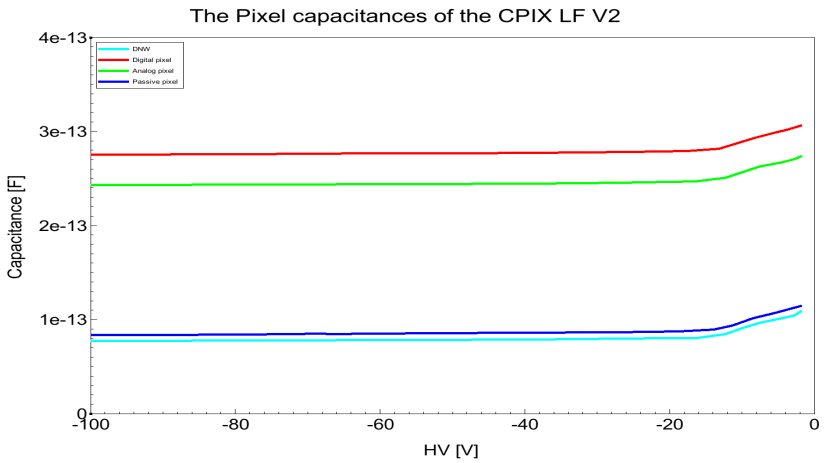


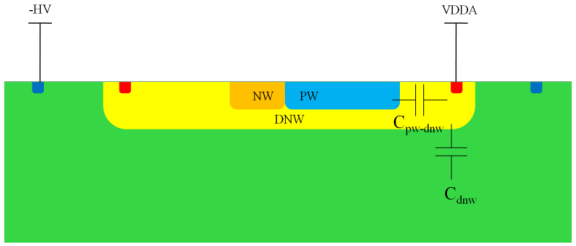
Passive pixel V2



AC simulation for V1 and V2







Capacitance of V1 pixels:

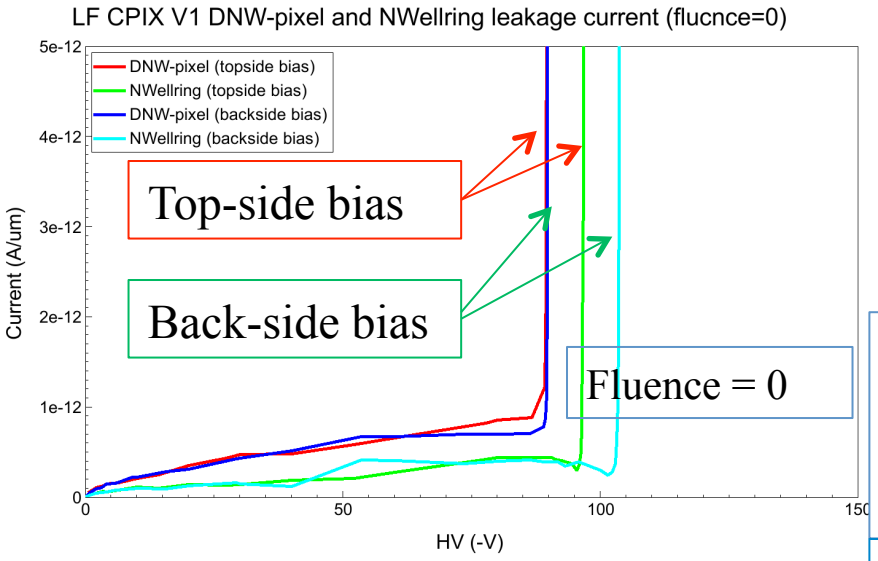
Pixel flavor	Digital	Analog	Passive
C_{dnw} @ - 50 V (fF)	107	107	107
C_{total} @ - 50 V (fF)	308	279	113

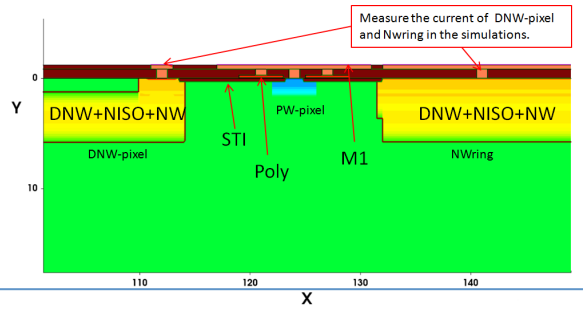
The capacitances of V2 pixels reduced due to the smaller DNW size (larger distance between the DNW and the pixel guard-ring).

Capacitance of V2 pixels:

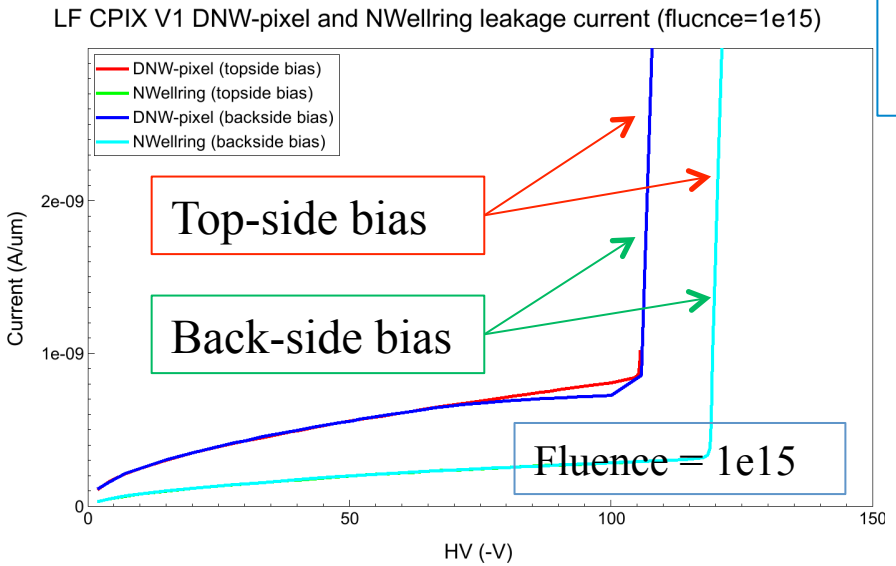
Pixel flavor	Digital	Analog	Passive
C_{dnw} @ - 50 V (fF)	79	79	79
C_{total} @ - 50 V (fF)	277	245	86

Leakage current of LF CPIX V1

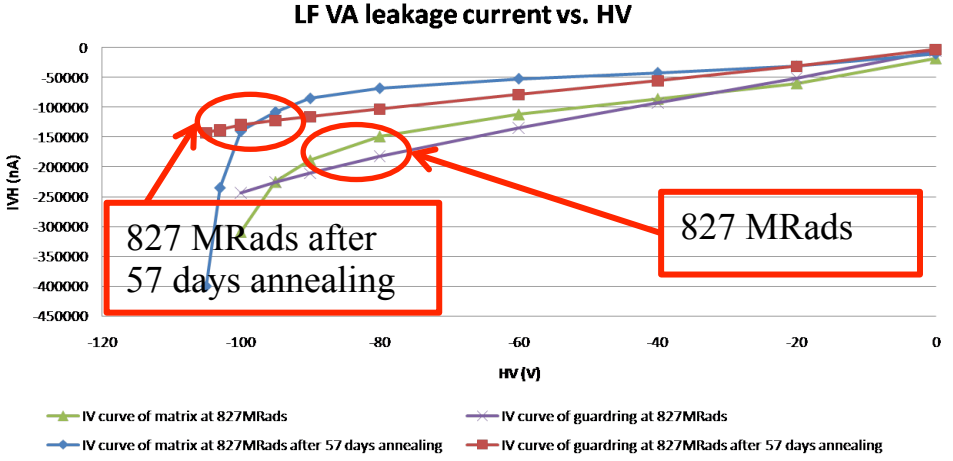




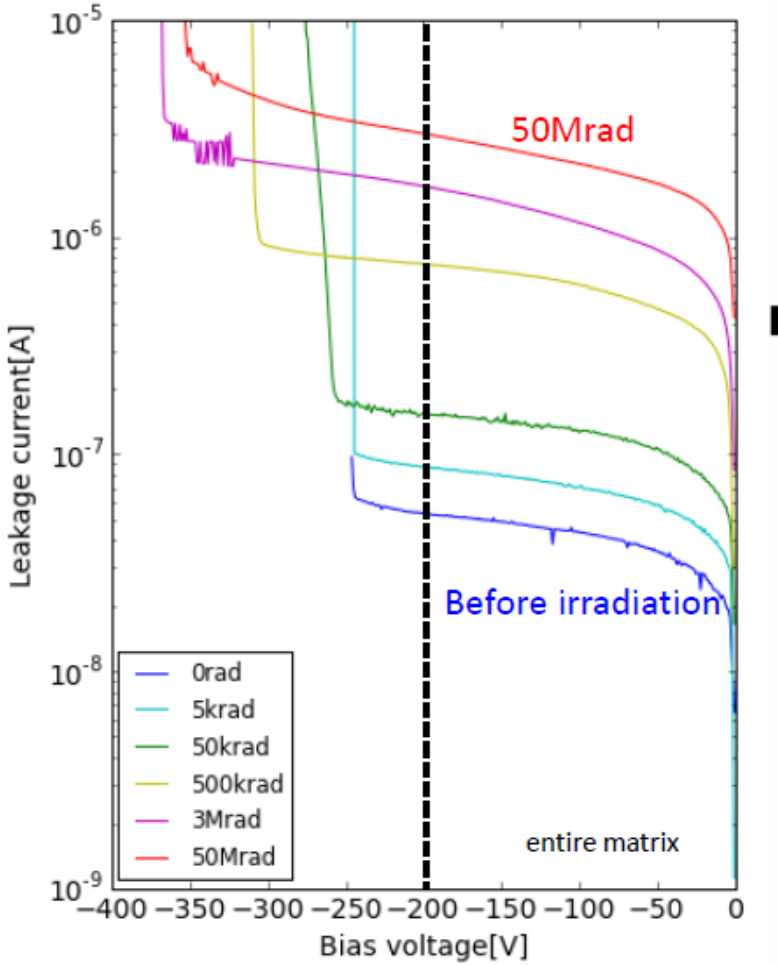
The DNW-pixel dominates the breakdown for both before and after irradiation.
After irradiation, the BV increases from 90 V to 105 V by simulation.

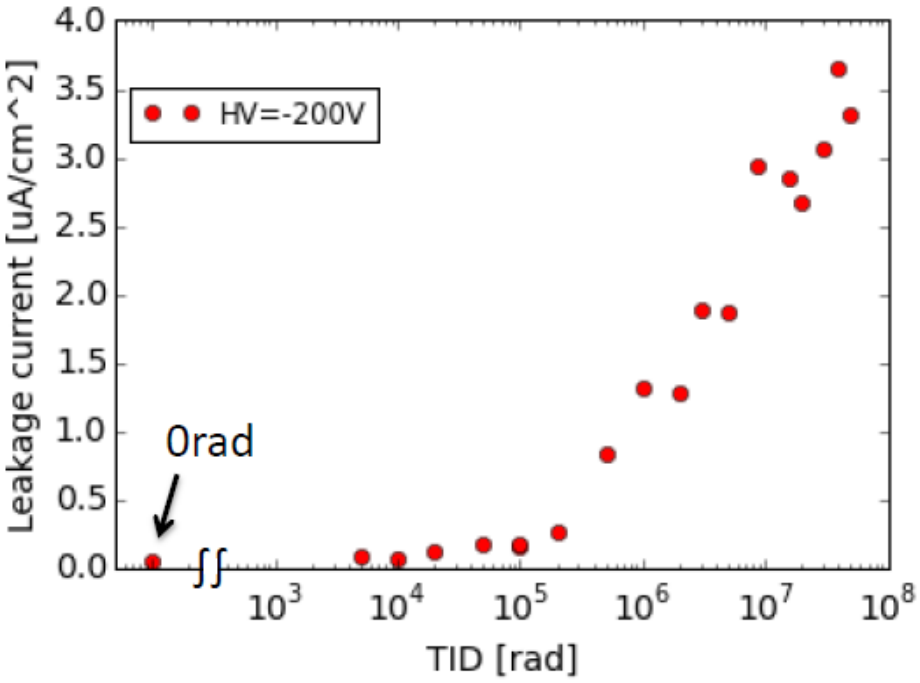


The matrix BV is ~76V before irradiation.
The matrix BV is ~100V at 827MRads.



Leakage current (LF_CPIX) –full matrix





Increase of the leakage current:

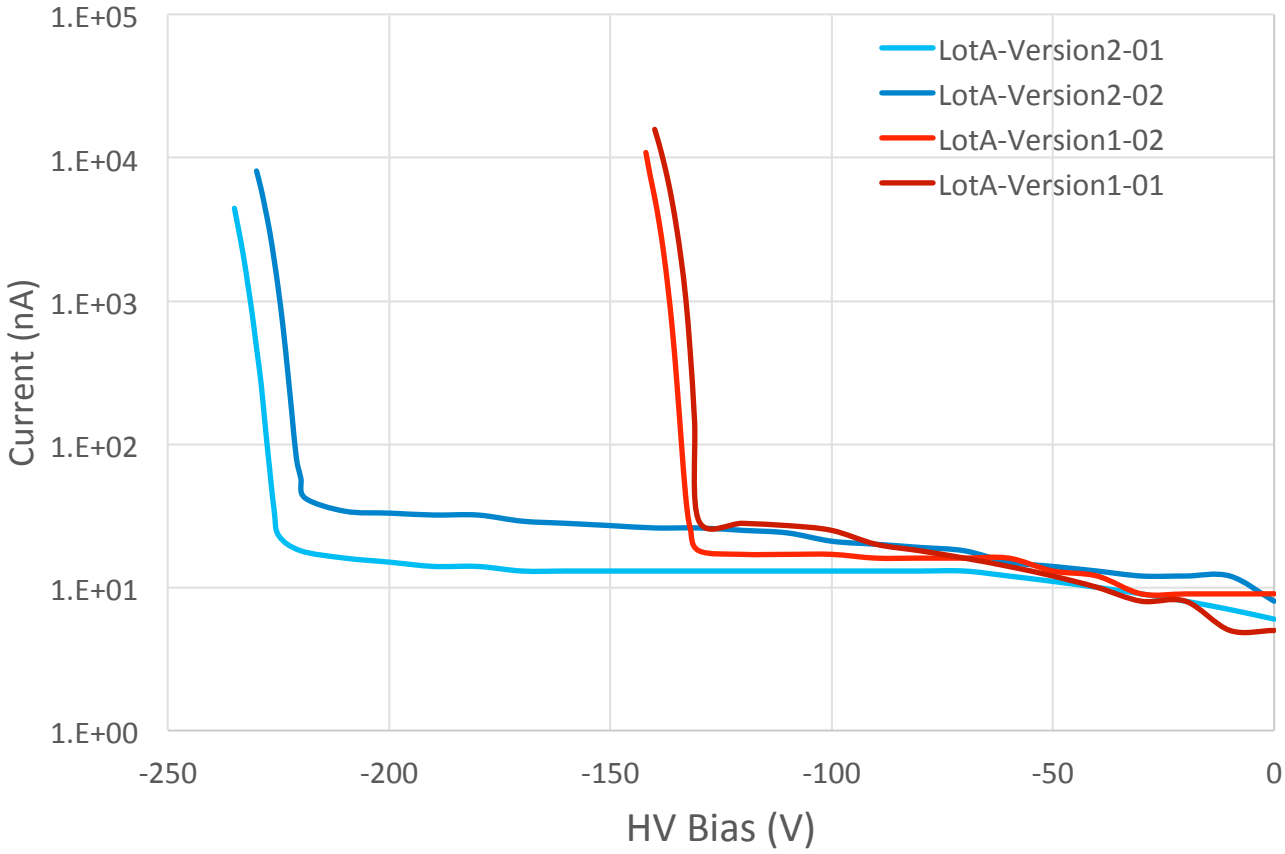
- small < 100krad
- after >100krad => logarithmic increase

0.4 nA/pixel at 50Mrad

=> $ENC_{leak} < 35$ e *cf.* $ENC_{total} \sim 150$ e (for 1 µs shaping time)

T.Hirono (Bonn)

I-V curve of LFCPIX



The breakdown voltage of LFCPIX version1 is about 130V.
The breakdown voltage of LFCPIX version2 is about 220V.
As expected

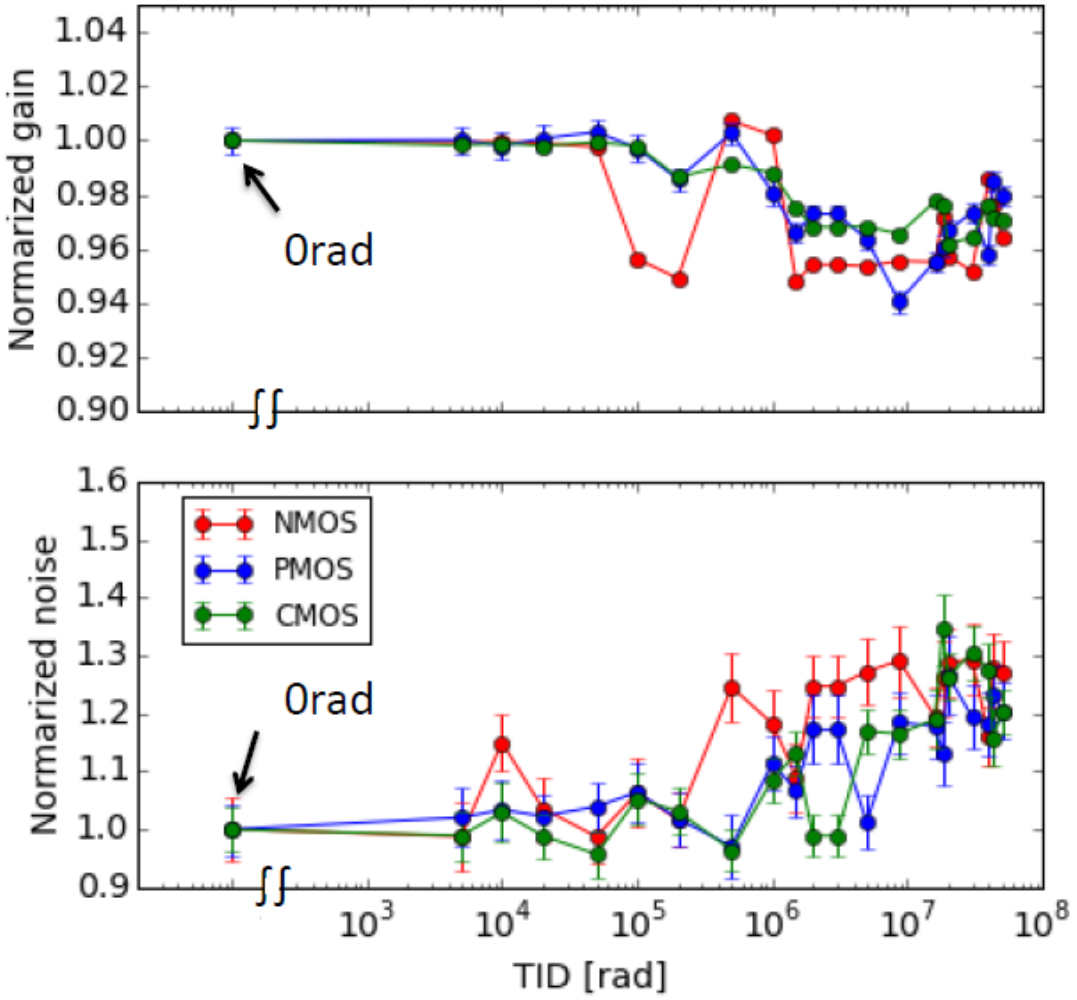
LF_CPIX : Gain and noise under radiation level

LF_CPIX

- Input transistor of CSA
  - NMOS
  - PMOS
  - CMOS
- Bias voltage: -100V

- Gain degradation: >95%
- Noise increase: ~30%

- No significant difference between the 3 flavors

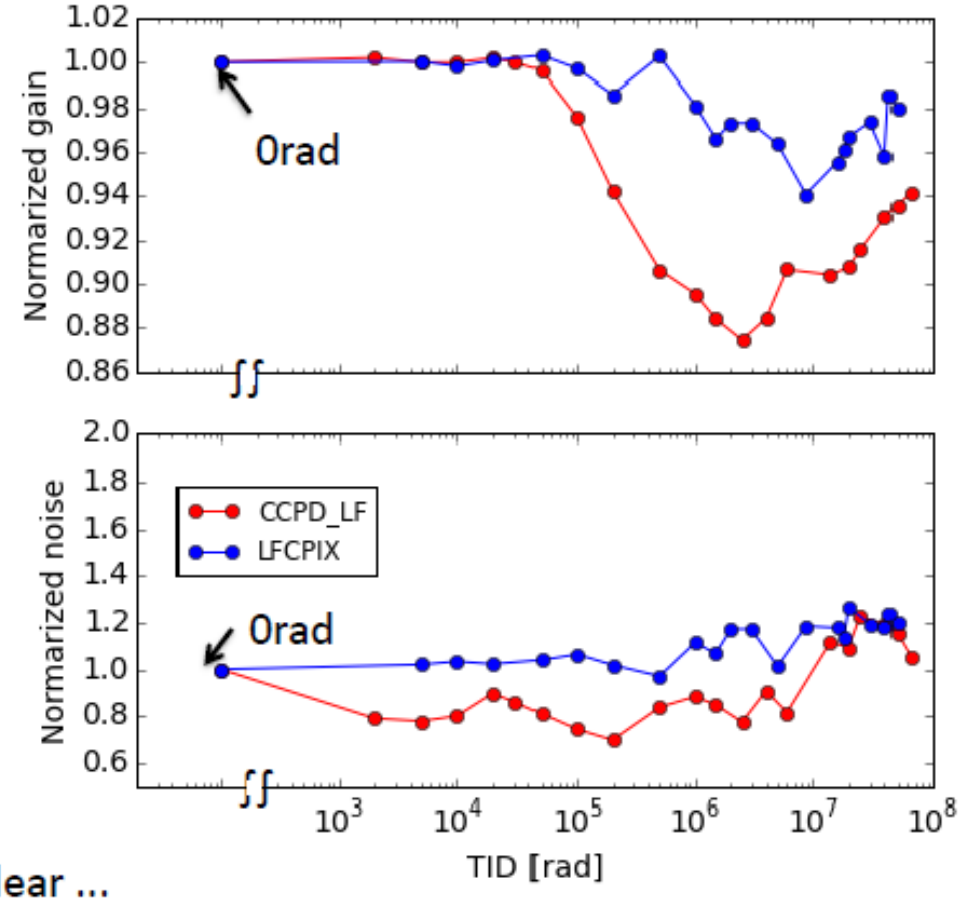


T.Hirono (Bonn)

Comparing CCPD-LF/LF-CPIX

- both have
  - PMOS input transistor
  - Long FB transistor
- pixel size 3x larger for LF-CPIX
  => more relaxed cell layout
- Bias voltage: -100V

Gain degradation:
LF-CPIX < CCPD_LF ☺
Noise increase:
LF-CPIX ≈ CCPD_LF 😐

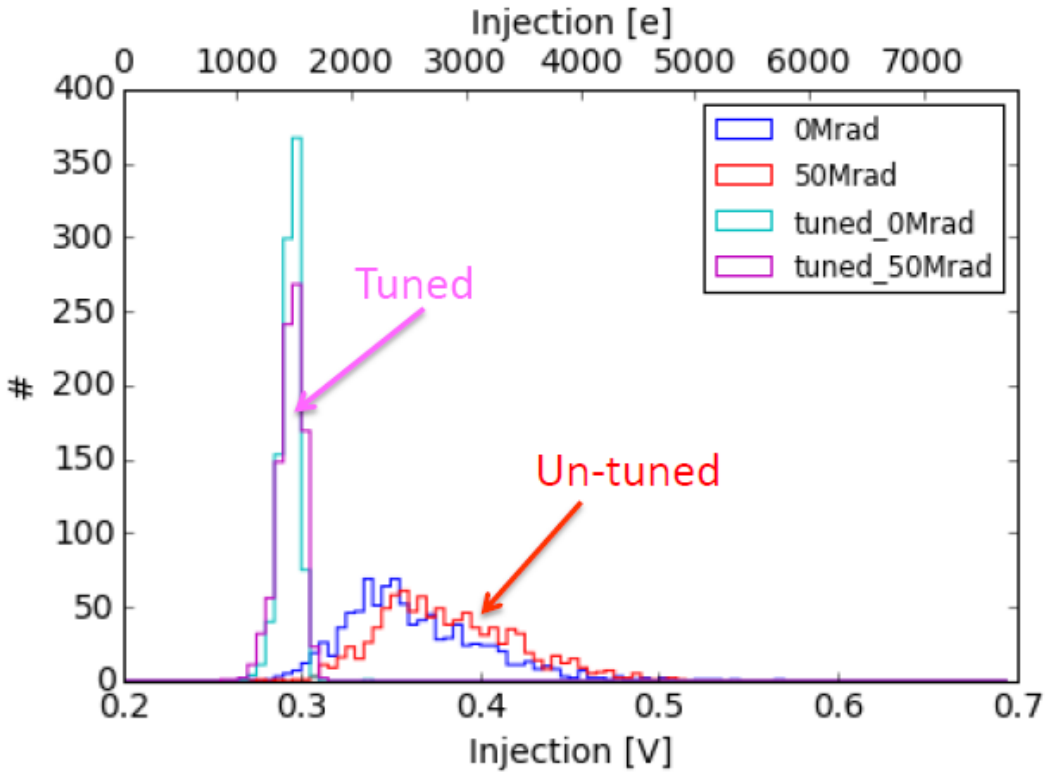


What makes the difference? not 100% clear ...
Pixel size, small changes in MOS size, global DAC of the chip, wafer, process...

Hirono, Bonn

LF_CPIX : Threshold dispersion under radiation level

Un-tuned and tuned threshold dispersions of LF_CPIX (PMOS)



Increase of the initial dispersion is ~10%, and the threshold is still tunable after TID=50Mrad

T.Hirono (Bonn)

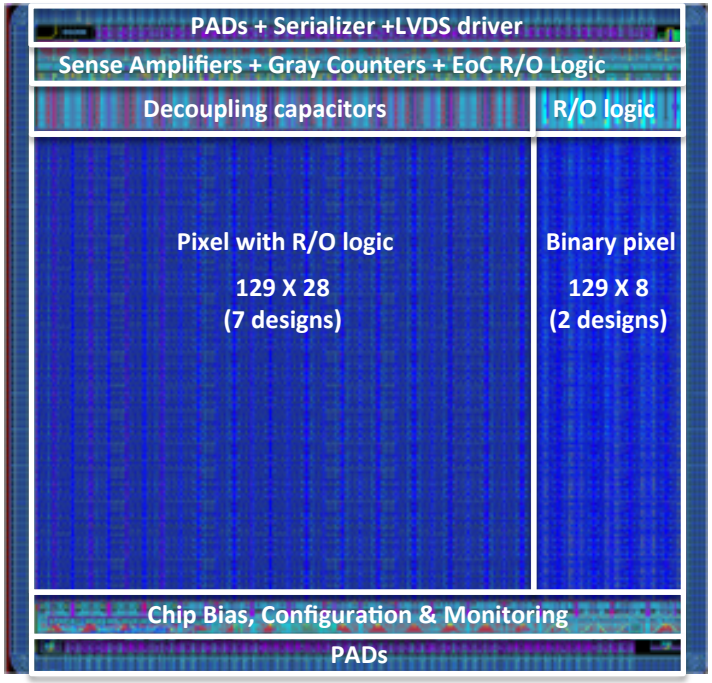
Specification of CMOS SENSOR for the ATLAS ITK upgrade

- A monolithic depleted CMOS sensor may be able to replace the diode sensor +FEIx of a hybrid module by incorporating this function in a single die CMOS monolithic chip. This replacement could offer several advantages, including finer pixel granularity, thinner charge collection layer for better 2- track separation, lower production cost and time, including savings by avoiding traditional bump bonding.

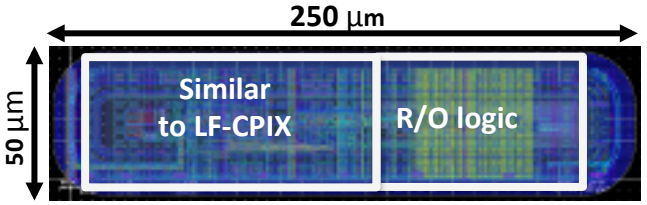
- Chip size = RD53 equivalent
- Pixel size < 50µm²
- Min. stable threshold setting <1000 e-
- Monolithic chip : digital bandwidth 160Mbps
  (number of bits transmitted per hit)
- Radiation level = 80 Mrad TID, and $1.5E^{15}$ n_{eq}/cm^2 NIEL at 4000 fb^{-1}

LF-Monopix demonstrator

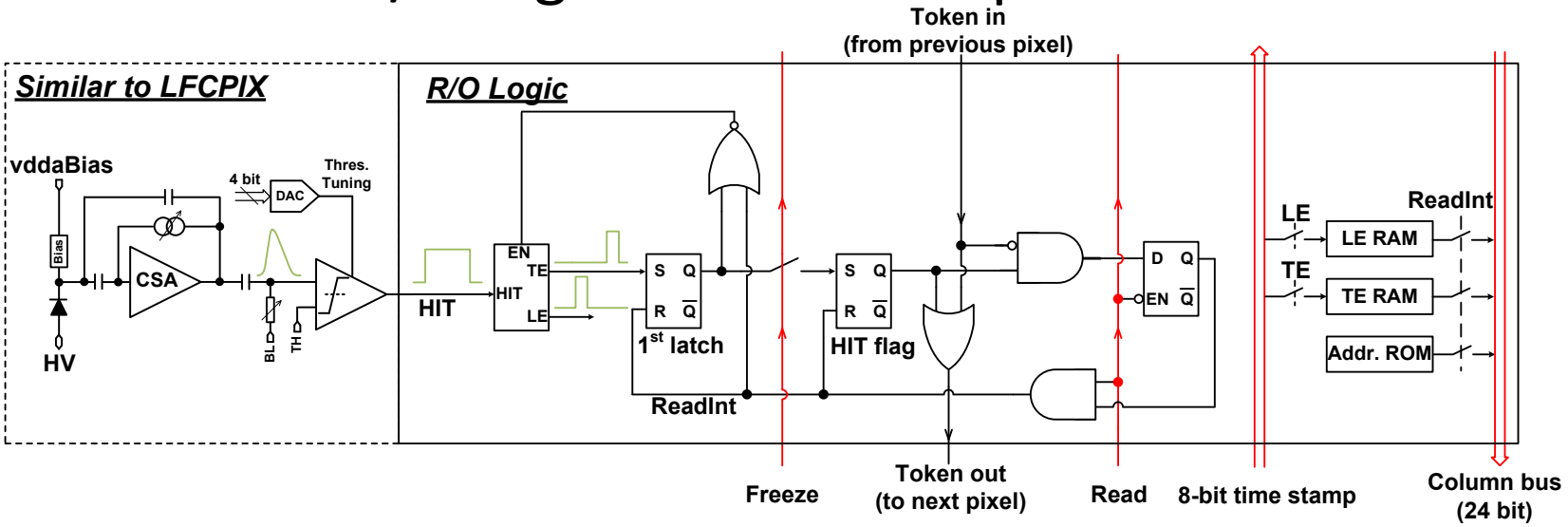
- 129x35 pixel array
- 40 MHz matrix readout FEI3like
- 9 flavours, each 4 col
- 160 Mhz LVDS serial output
- 8 bit LE/TE/ToT
- full custom digital: low noise and fit into pixel



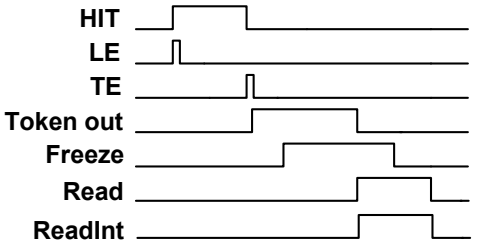
LF-Monopix: key design ingredients



- Pixel analog design a la LFCPIX
- Pixel with R/O logic => FE-I3 like pixel

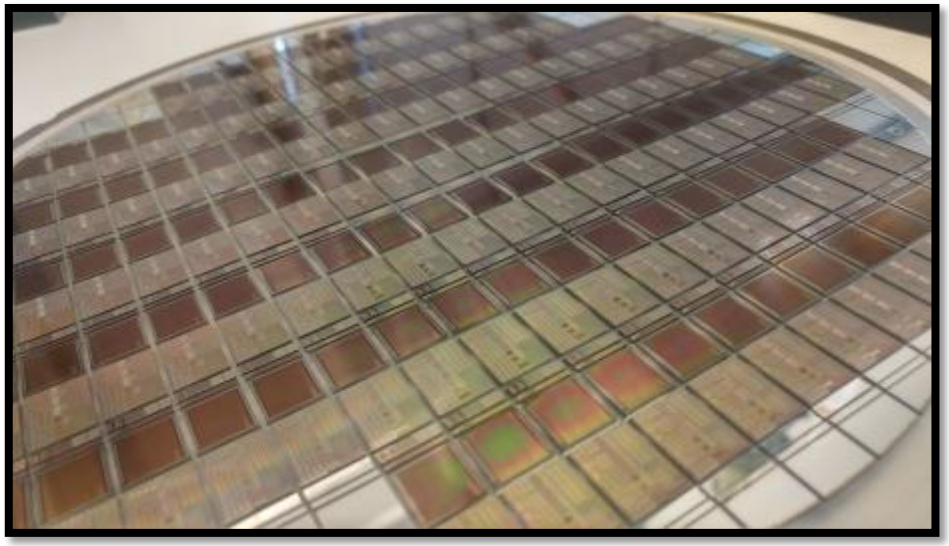


- R/O logic fitted inside the LF-CPIX pixel
- Larger detector capacitance & More cross talk
  - **=> full-custom dig. circuit**
  - **=> low noise circuit for critical dig. Blocks**
  - **=> Very careful layout needed**

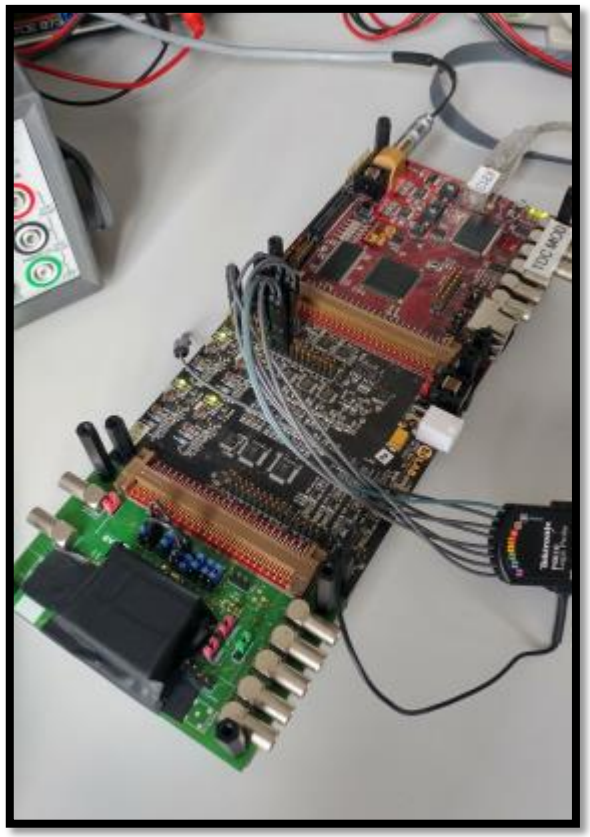


LF Monopix wafer received February

- Diced in March, wire bonded and tested at Bonn

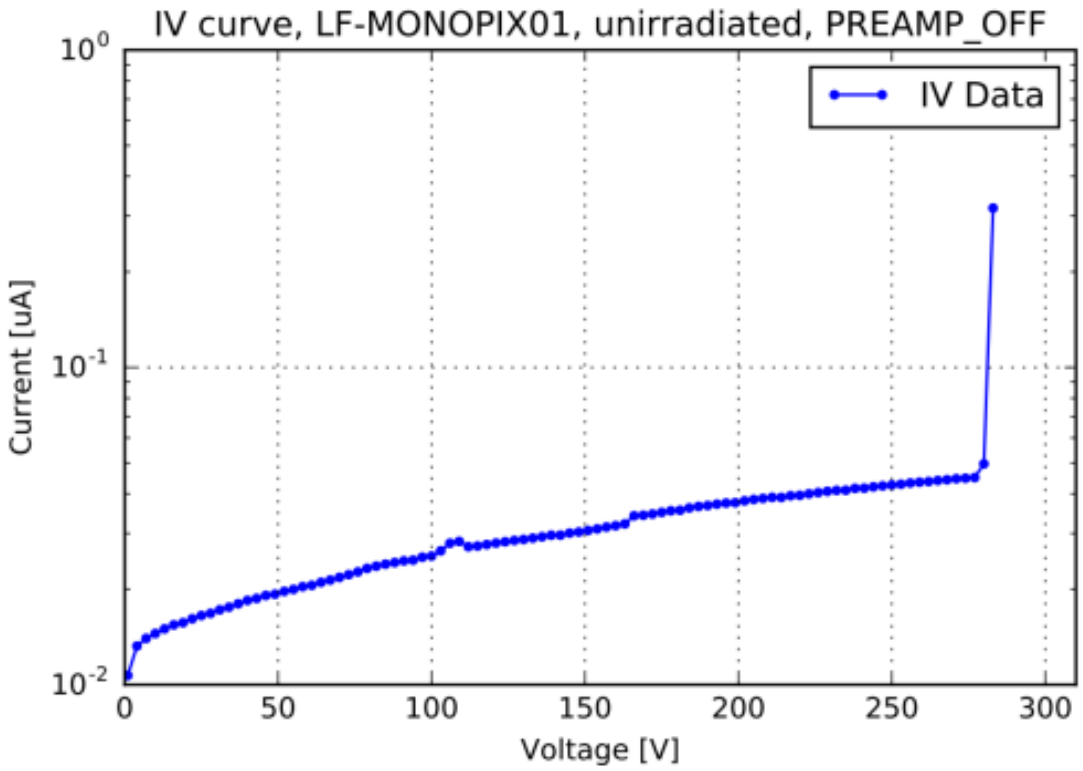


Received
2017 Q1

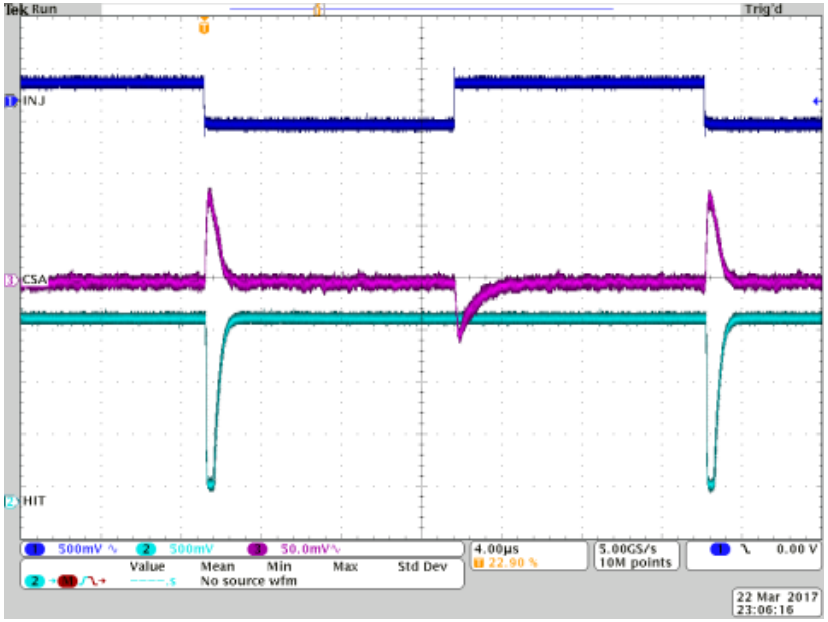


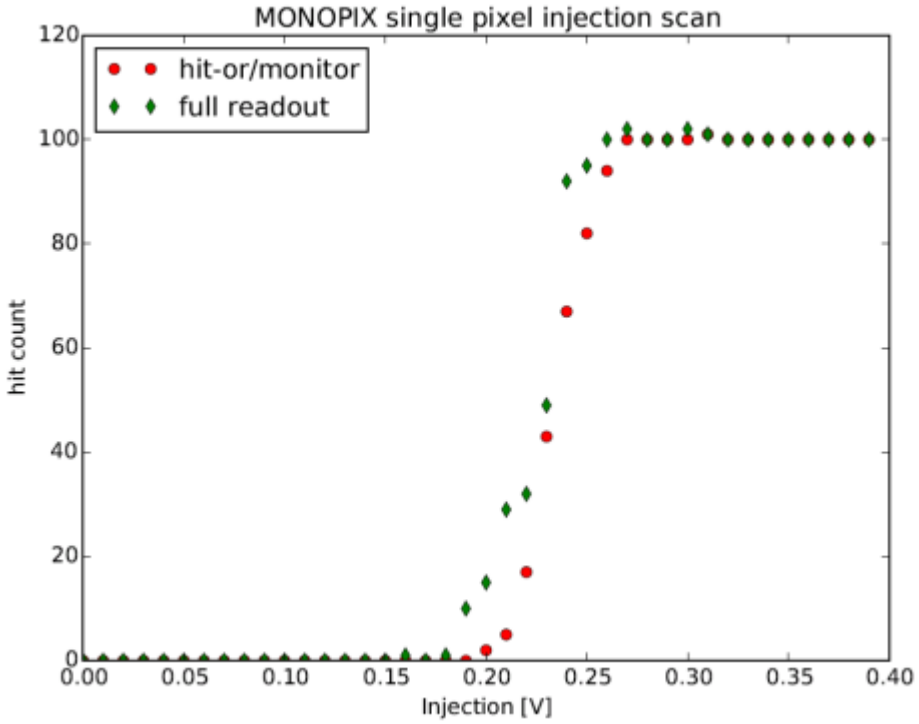
LF-Monopix IV curve

- HV breakdown at 280 V



LF_MONOPix - Readout - First results





https://github.com/SiLab-Bonn/monopix_daq

Conclusions

- Three generations of active CMOS sensors were designed and fabricated in LFoundry 150nm technology
- **CCPD-LF** fully characterized under X-ray, neutron and proton irradiations. At TID=50 MRad the increase of leakage current, gain decrease, noise increase and threshold tunability are acceptable
- **LF-CPIX "Demonstrator"** – design and optimization with TCAD tools, better breakdown voltage, after TID=50 MRad better gain degradation (~10%), good threshold tunability
- **LF-Monopix** delivered and fully functional, to be characterized and irradiated

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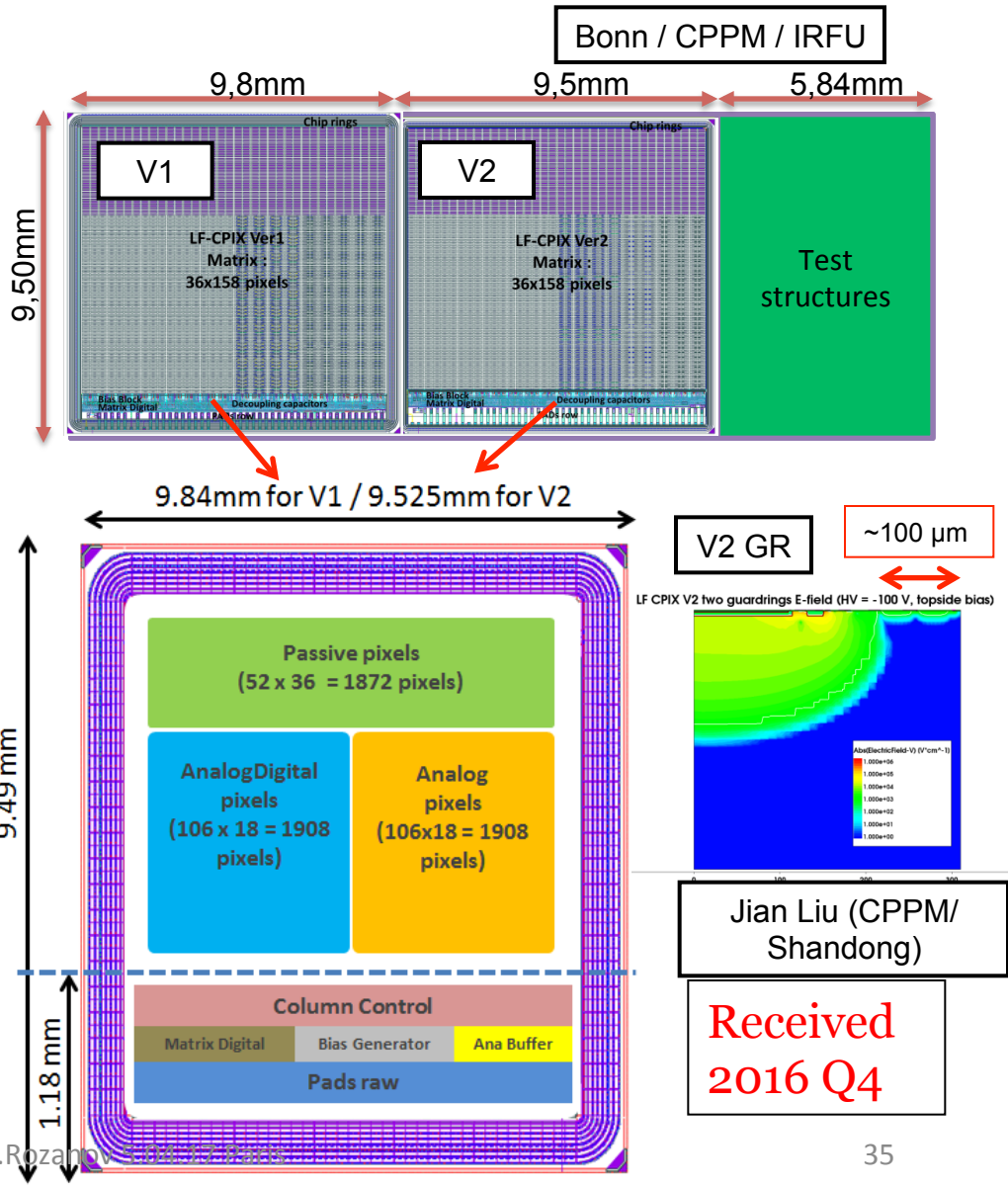
Backup material

LFOUNDRY: LF-CPIX demonstrator

- Feb. 2016: 10×10 mm^2 chip size
- V2 = V1 + new guard ring strategy.

Pixel Matrix :

- Pixel 250µm×50µm (FEI4-like)
- All pixels have bond pad to FEI4
- 3 sub-matrices :
  - **Passive**: only DNwell sense diode
  - **AnalogDigital**: à la LF VA, 4 flavors (different diode bias, diff. input transistors NMOS and PMOS).
  - **Analog**: preamp with complementary input CMOS, and 8 flavors (diode polarization, outputs “linear”, “saturated” or “digital”…).
  - Preamp out / hitOR available for all pix!



LFOUNDRY: MONOPIX demonstrator

– Chip overview

– Large input from LF-CPIX: pixel, floor plan…

– 9 flavors for comparative studies => each 4 col.

- Pixel with R/O logic (FE-I3 like pixel)

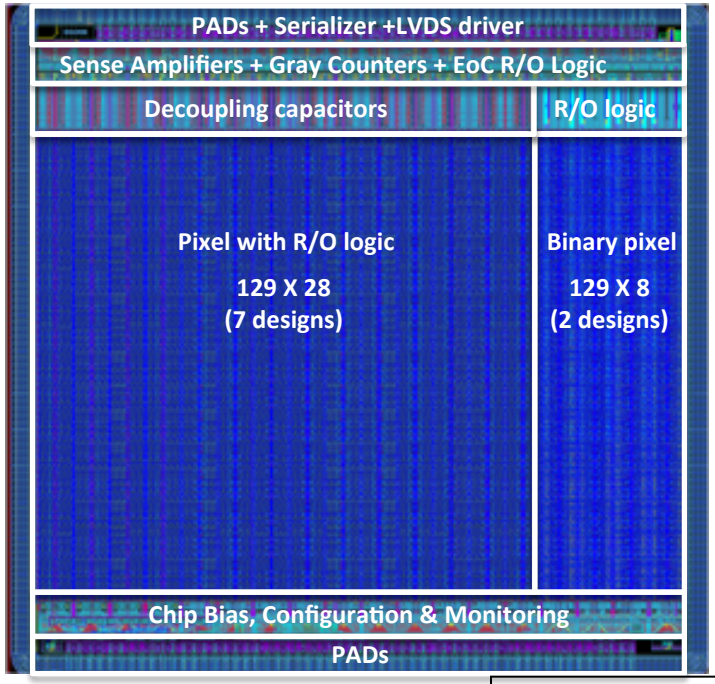
❑ NMOS/CMOS pre-amp. ❑ Old/new discriminator

❑ Different power domains for discriminator.

❑ CS /CMOS token transmission

- Binary pixel with R/O logic at column end

❑ NMOS /PMOS source follower for “HIT” R/O



Received 2017 Q1

– Many design efforts to meet the challenges in terms of noise and timing

❑ faster pre-amp. & discriminator ❑ careful layout and post layout sim.

❑ full-custom in-pixel digital circuit & low noise digital block