Status of WP6 activities in Liverpool

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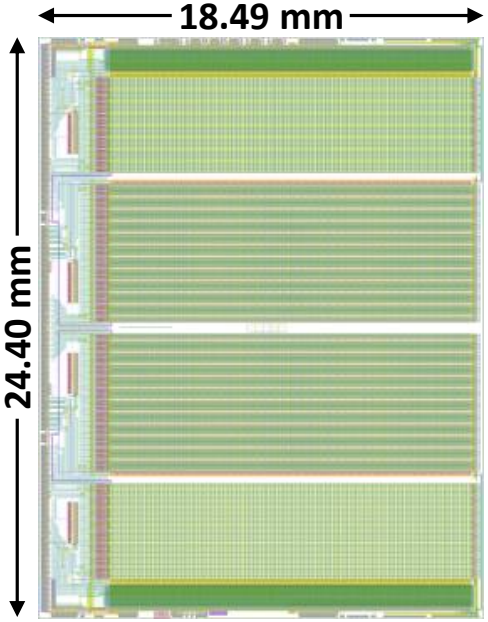
Outline

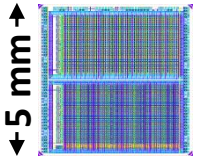
1. HV-CMOS chips
2. Test structures in HV-CMOS chips
3. H35DEMO
4. RD50 HV-CMOS submission
5. Accµra100 flip-chip bonder and test kit
6. Summary

HV-CMOS chips



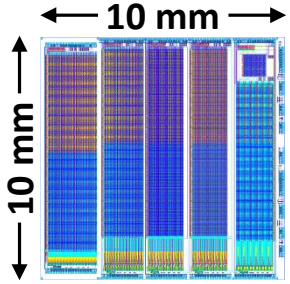
H35DEMO - Features:

- ams 0.35 µm HV-CMOS (H35)
- Contributions from CERN, IFAE, KIT, Uni. Bern, Uni. Geneva and Uni. Liverpool
- Different matrices (2 CCPD and 2 monolithic) and test structures
- Pixel size is 50 µm x 250 µm (for compatibility with FE-I4)
- Resistivities: 20 Ω·cm, 80 Ω·cm, 200 Ω·cm and 1k Ω·cm
- Delivered in December 2015 (eng. run)



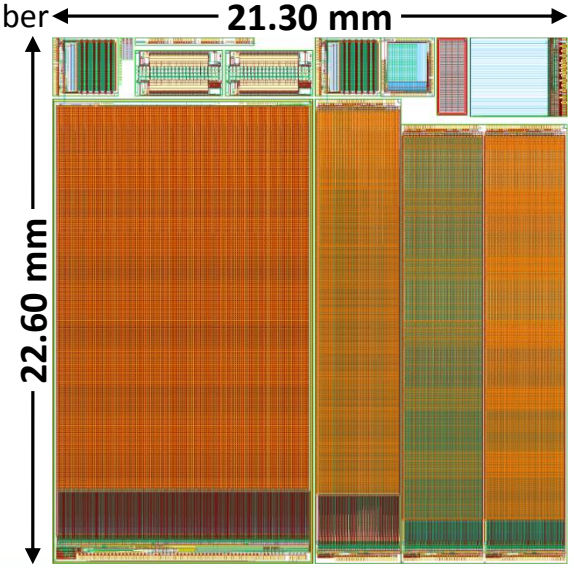
Features:

- LFoundry 150 nm HV-CMOS
- Contributions from IFAE, Uni. Geneva and Uni. Liverpool
- Different matrices (2 monolithic) and test structures
- Resistivities: 500 Ω·cm and 1.9k Ω·cm
- Submitted in November 2016 (MPW)
- ASICs will be delivered in April 2017



Features:

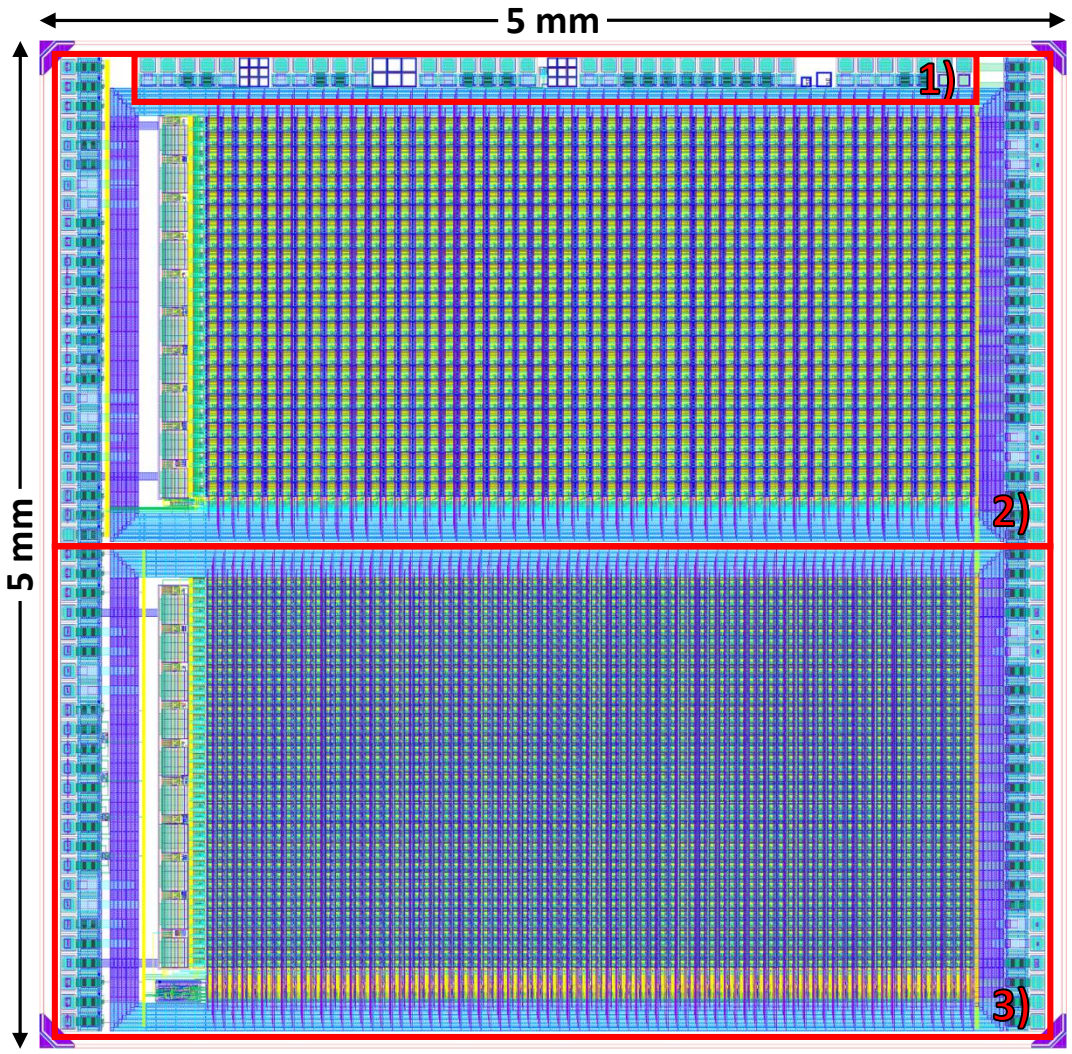
- LFoundry 150 nm HV-CMOS
- Contributions from BNL, IFAE, KIT, Uni. Bern, Uni. Geneva, Uni. Heidelberg and Uni. Liverpool
- Different matrices (1 CCPD and 5 monolithic) and test structures
- Resistivities: 100 Ω·cm, 500-1.3k Ω·cm, 2k-2.5k Ω·cm and 3.6k-3.9k Ω·cm
- Submitted in August 2016 (MPW)
- Delivered in March 2017



Features:

- ams 180 nm HV-CMOS (H18)
- Contributions from CERN, KIT, Uni. Geneva, Uni. Heidelberg and Uni. Liverpool
- Different matrices (1 CCPD and 3 monolithic, it includes MuPix8), CLICpix and test structures
- Submitted in January 2017 (eng. run)
- ASICs will be delivered in ~April 2017

LFoundry HV-MAPS chip



Areas from top to bottom (see R. Casanova's talk):

1) Test structures

- TCT/e-TCT
- sensor capacitance measurement
- very fast measurements

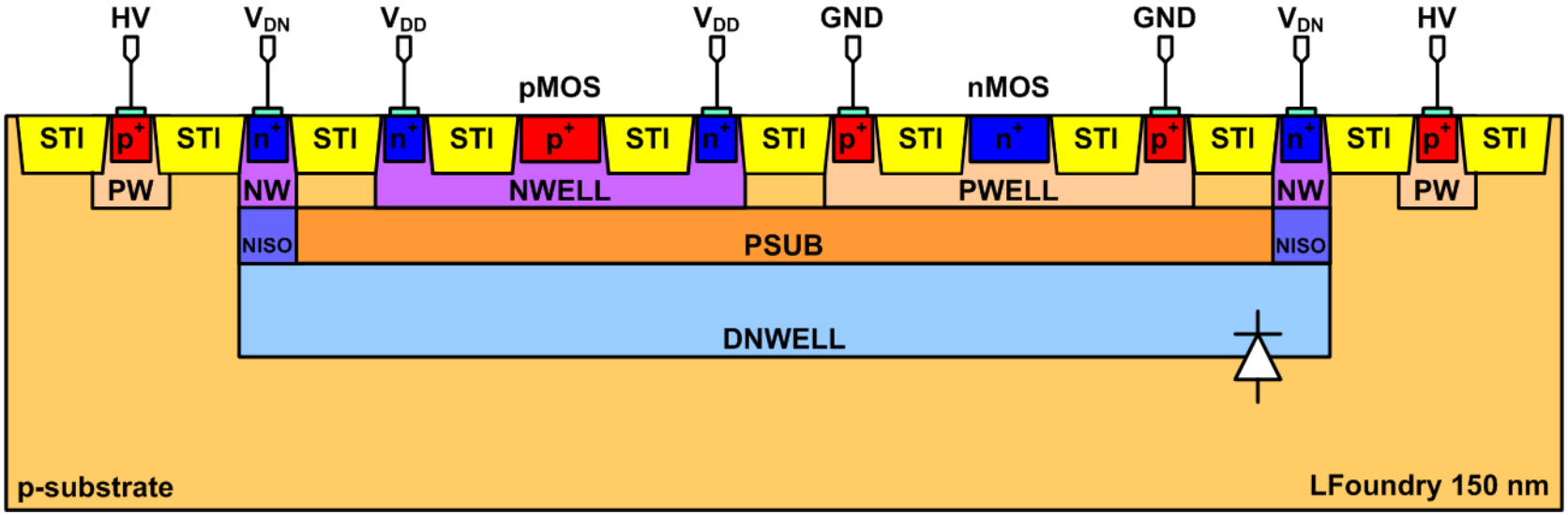
2) Non-ATLAS matrix

3) Matrix of HV-MAPS pixels with FEI3-like readout

- 40 rows x 78 columns of pixels
- pixel area is 50 µm x 50 µm
- analog and digital readout electronics are embedded inside the pixel area
- analog readout electronics → preamplifier, shaper and discriminator
- digital readout electronics → electronics to process the output of the discriminator, 2 8-bit DRAM memories to store the TS and 1 8-bit DROM memory to store the pixel address
- This matrix was designed to study very small pixels with all the readout electronics integrated inside the pixel area and to qualify this technology for the HL-LHC upgrade

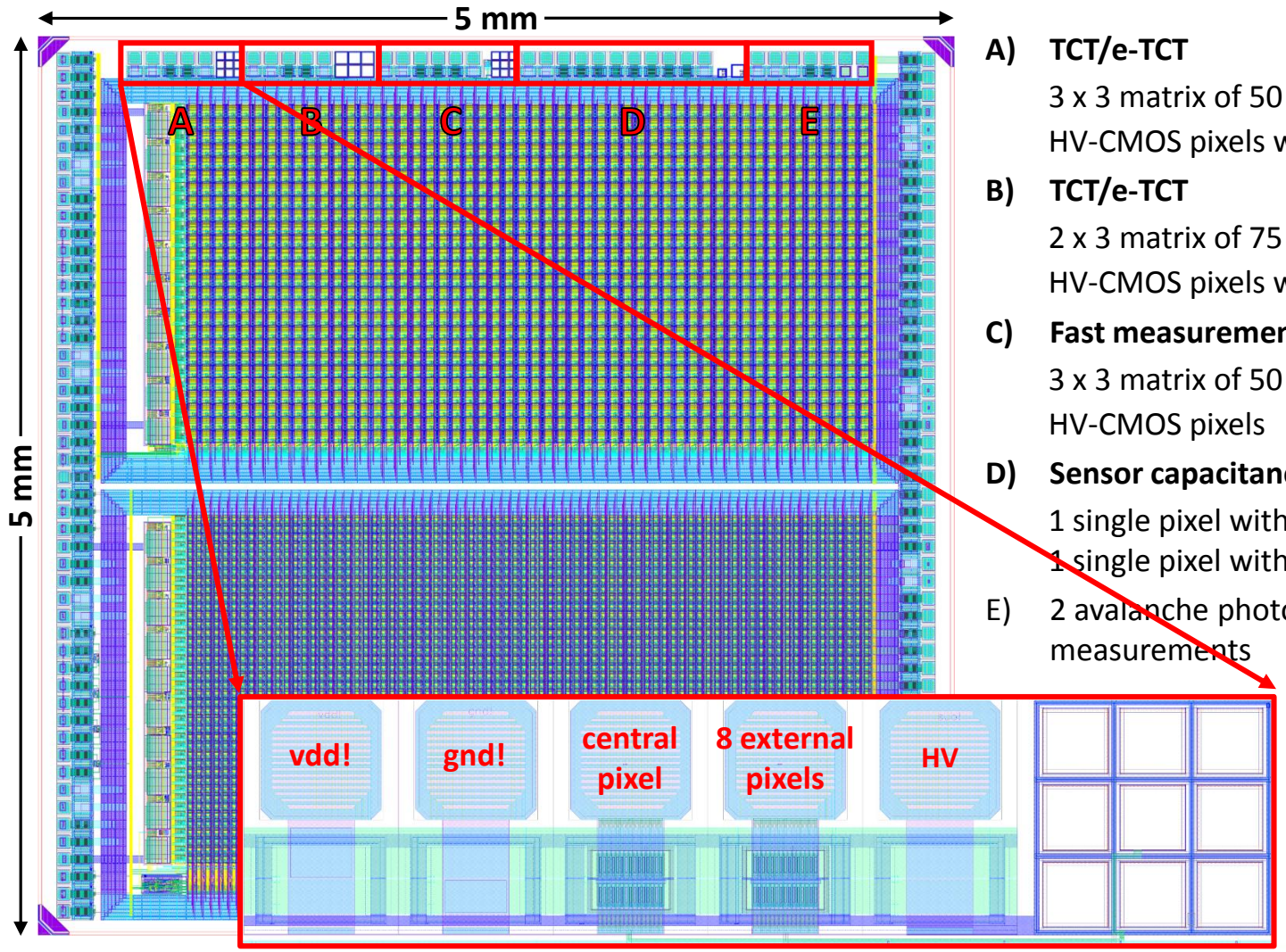
- No backside biasing option
- Detector thickness is 280 µm

LF2 - Pixel cross-section



- The sensing diode is a p-substrate/DNWELL junction
- The DNWELL can be isolated from NWELLs/PWELLs thanks to the PSUB layer
- **Therefore, it is possible to have fully CMOS electronics inside the pixel area**
- In our case, we have multiple NWELLs and PWELLs:
  - 1 NWELL/PWELL for the CSA and the shaper
  - 1 NWELL/PWELL for the CMOS discriminator
  - 1 NWELL/PWELL for the digital readout
  - 1 NWELL for the pMOS transistors of the sensor bias circuit (this NWELL is connected to the DNWELL)
- The DNWELL is biased through an n^+/NWELL/NISO structure

LF2 - Test structures



A) TCT/e-TCT

3 x 3 matrix of 50 µm x 50 µm
HV-CMOS pixels without electronics

B) TCT/e-TCT

2 x 3 matrix of 75 µm x 75 µm
HV-CMOS pixels without electronics

C) Fast measurements (with a laser)

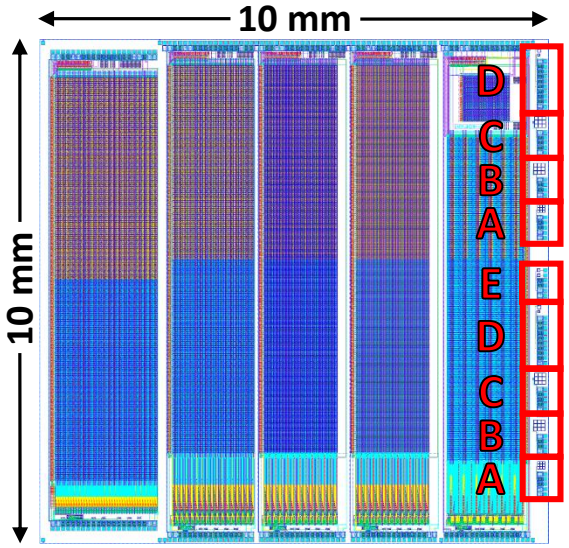
3 x 3 matrix of 50 µm x 50 µm
HV-CMOS pixels

D) Sensor capacitance measurement

1 single pixel with 50 µm x 50 µm
1 single pixel with 75 µm x 75 µm

E) 2 avalanche photodiodes for I-V measurements

LF1 and ams 180 nm - Test structures



A) **TCT/e-TCT →** 3 x 3 matrix of 50 µm x 50 µm HV-CMOS pixels without readout electronics

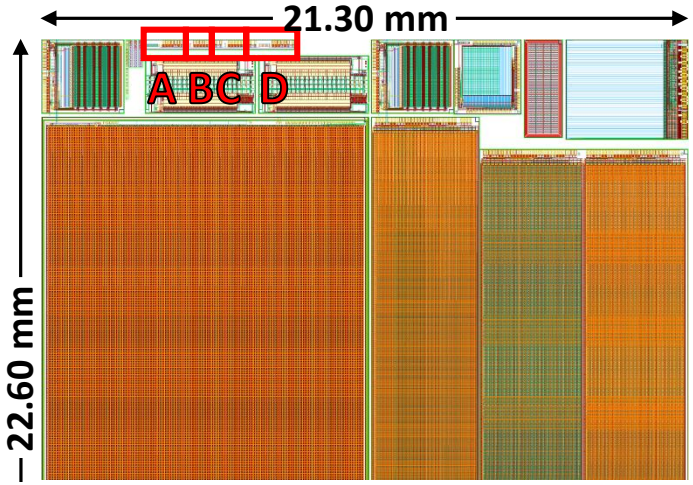
B) **TCT/e-TCT →** 3 x 3 matrix of 75 µm x 75 µm HV-CMOS pixels without readout electronics

C) **Fast measurements →** 3 x 3 matrix of 50 µm x 50 µm HV-CMOS pixels

D) **Sensor capacitance measurement**

1 single pixel with 50 µm x 50 µm
1 single pixel with 75 µm x 75 µm

E) 2 avalanche photodiodes for I-V measurements



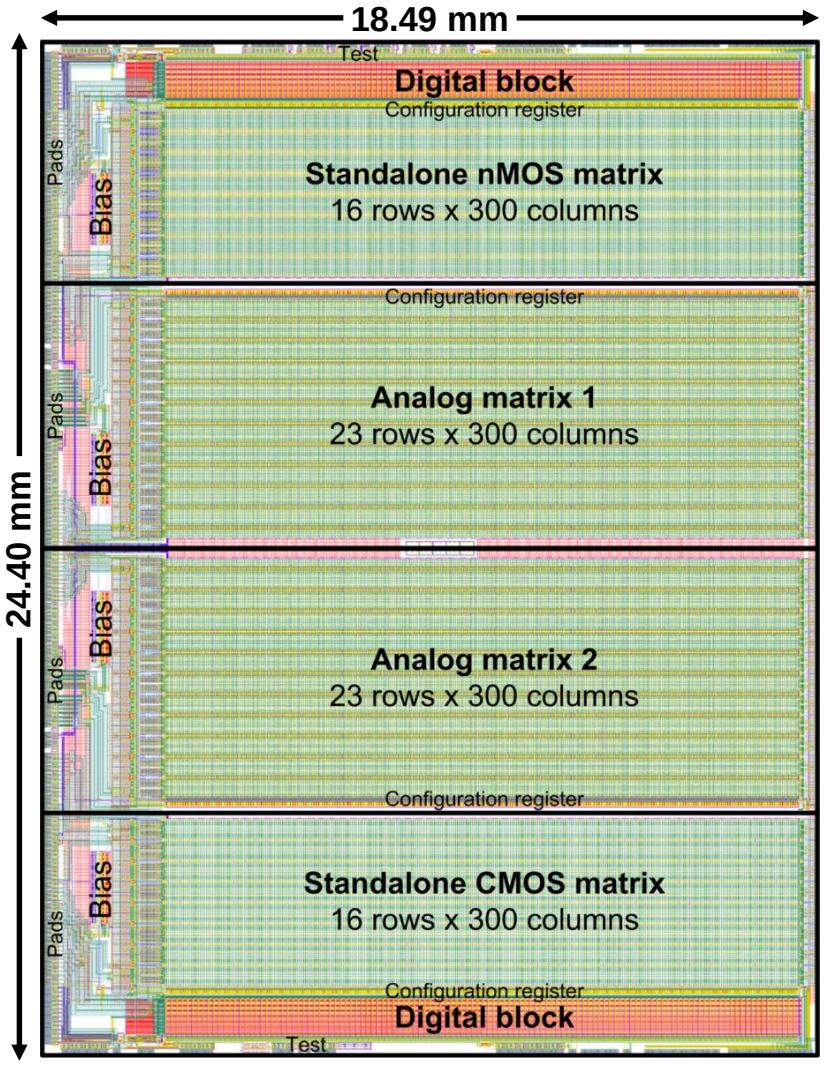
A) **TCT/e-TCT →** 3 x 3 matrix of 33 µm x 125 µm HV-CMOS pixels without readout electronics

B) **Sensor capacitance measurement →** 1 single pixel with 33 µm x 125 µm (simple pixel)

C) **Sensor capacitance measurement →** 1 single pixel with 33 µm x 125 µm (pixel with TW compensation)

D) **Fast measurements →** 3 x 3 matrix of 33 µm x 125 µm HV-CMOS pixels

H35DEMO - Design aspects reminder



Main features:

- ams 0.35 µm HV-CMOS (H35)
- submission through an engineering run
  - submission in October 2015
  - wafer production finished in December 2015
- different substrate resistivities to improve SNR
  - 20 Ω·cm (standard), 80 Ω·cm, 200 Ω·cm, 1k Ω·cm

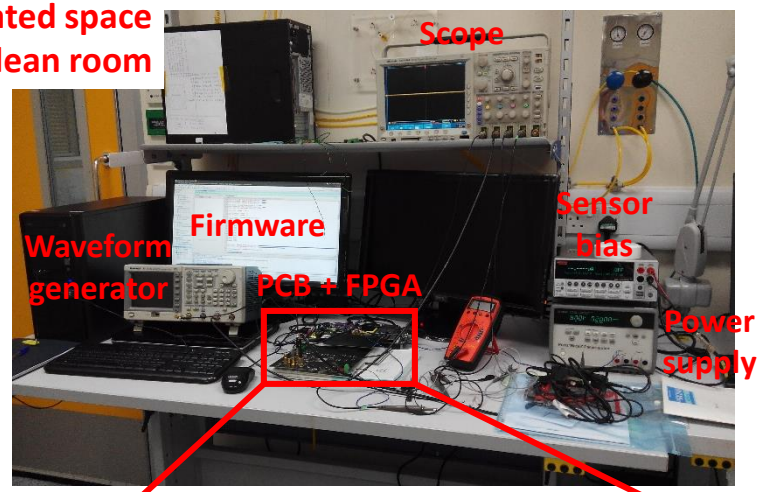
Areas (from top to bottom):

- standalone nMOS matrix
  - digital pixels with in-pixel nMOS comparator
  - standalone readout
- analog matrix (2 identical arrays)
  - different flavours
- standalone CMOS matrix
  - analog pixels with off-pixel CMOS comparator
  - standalone readout
- All pixels are 50 µm x 250 µm for compatibility with FEI4

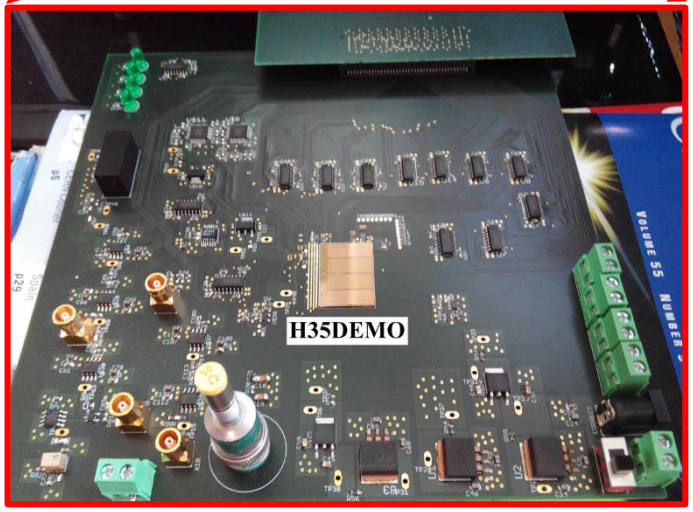
CERN KIT Karlsruhe Institute of Technology UNIVERSITÉ DE GENÈVE IFAE UNIVERSITÄT BERN UNIVERSITY OF LIVERPOOL

H35DEMO - Measurements with Sr90

Allocated space in clean room



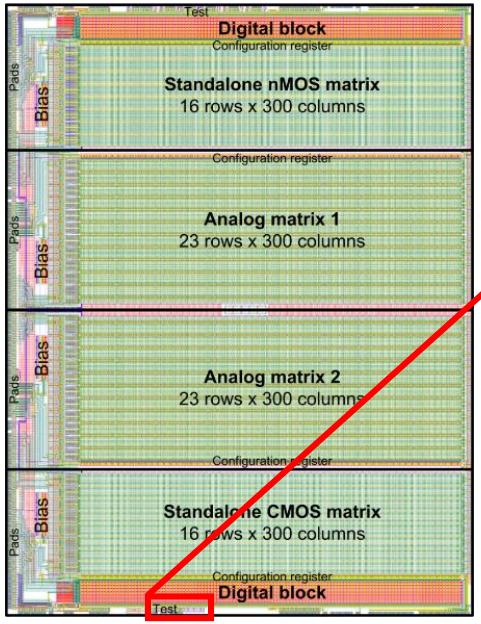
Custom made PCB designed at UoL



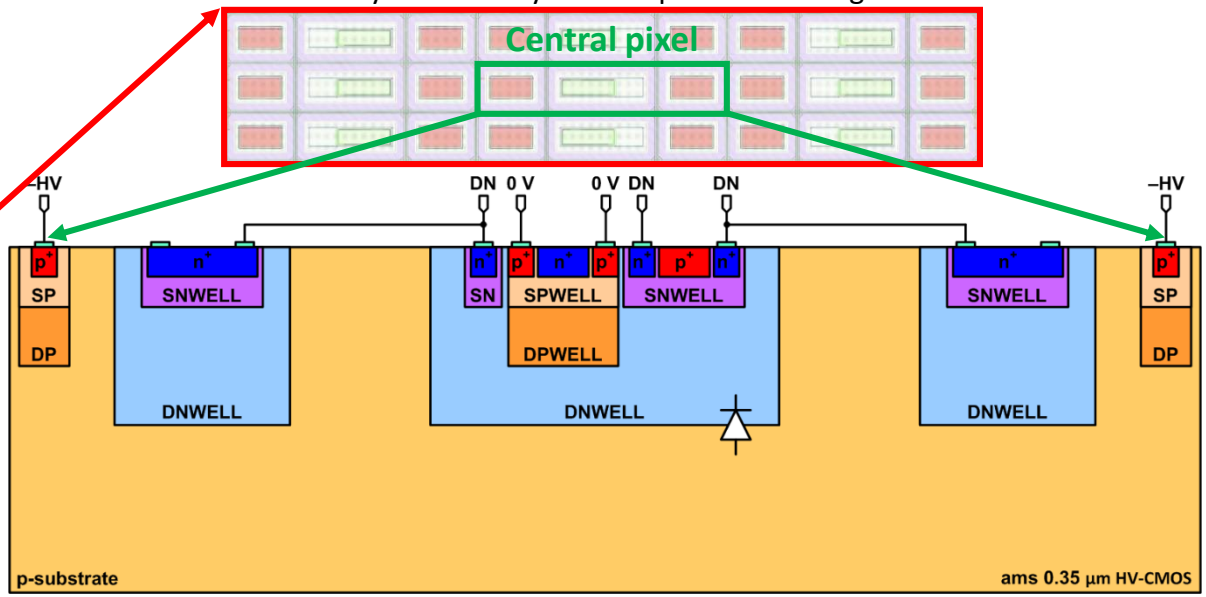
CSA output when the ASIC is irradiated with a Sr90 source (standalone nMOS matrix)

Amplitude = 342 mV
Rise time = 105 ns
Fall time = 1.35 µs

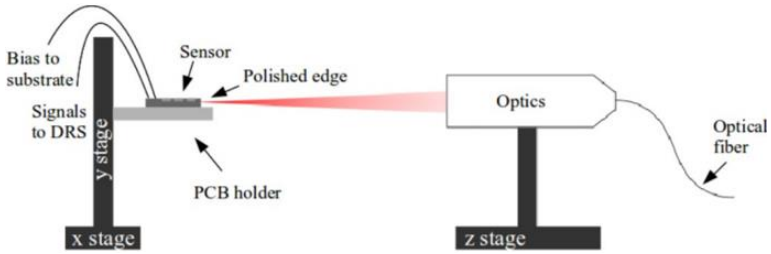
H35DEMO - e-TCT measurements



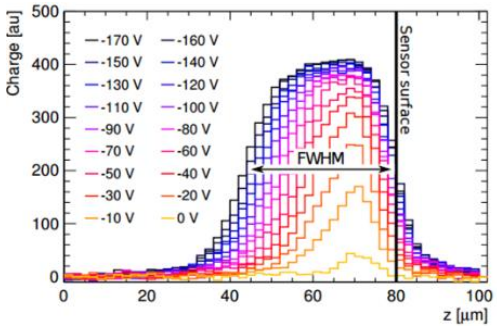
No circuitry or metal layers on top of the sensing diodes



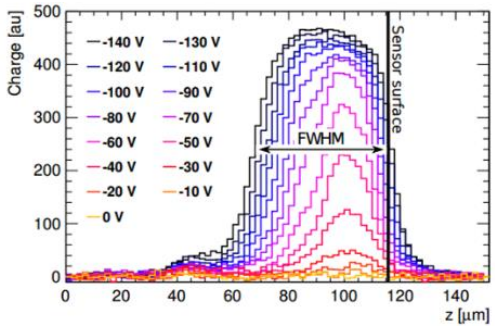
e-TCT set-up:



Measured results:



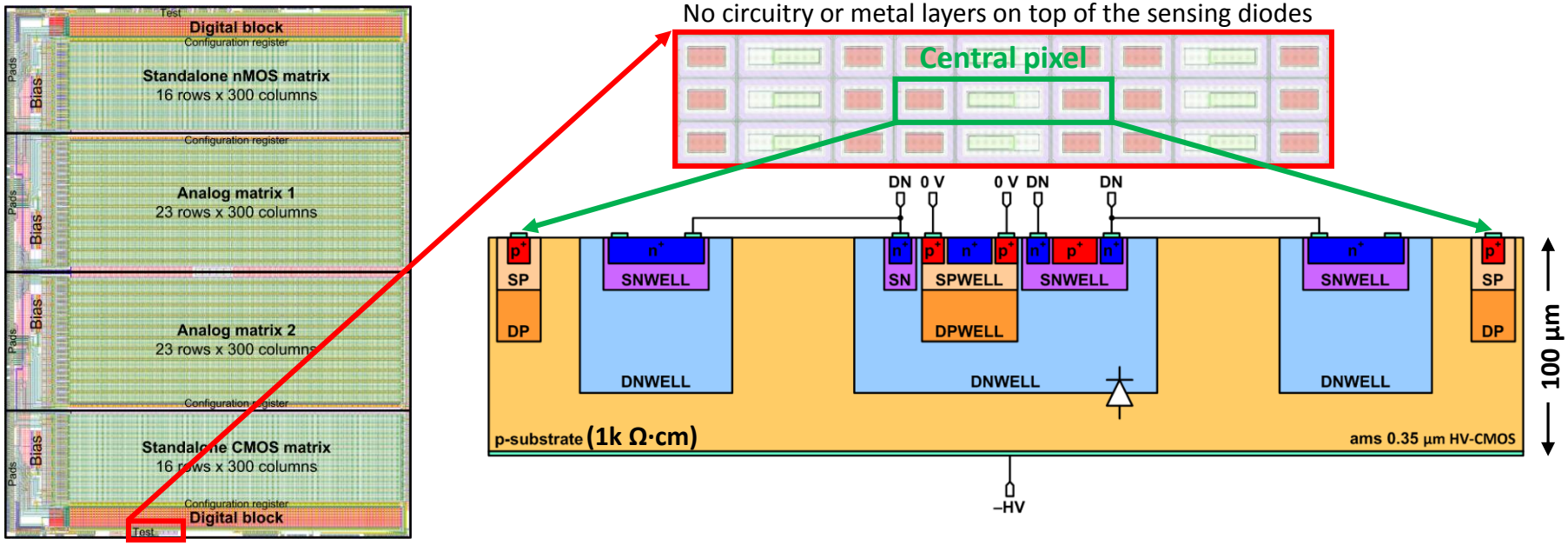
ρ=80 Ω·cm, d~35 µm @ -170 V



ρ=200 Ω·cm, d~45 µm @ -140 V

E. Cavallaro, arXiv:1611.04970v2

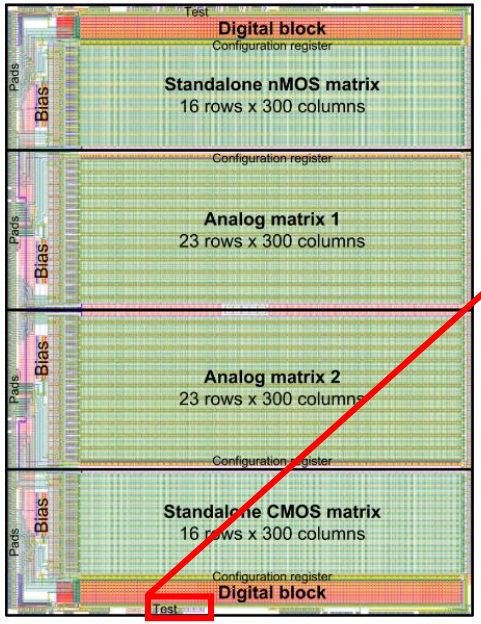
H35DEMO - e-TCT measurements



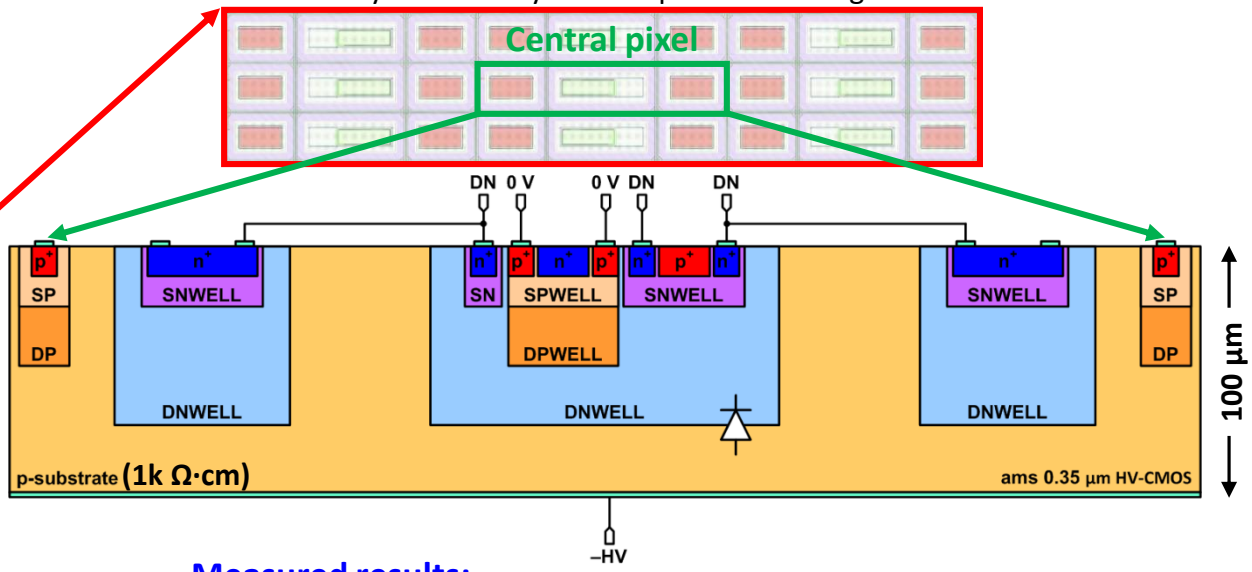
- Samples of the **H35DEMO in the 1k Ω·cm resistivity** were **backside processed**:
  - thinning to 100 µm
  - backside p^+ implantation with boron
  - thermal annealing
  - backside metallization

  to allow backside biasing and achieve a **stronger, more uniform electric field in the sensing volume**

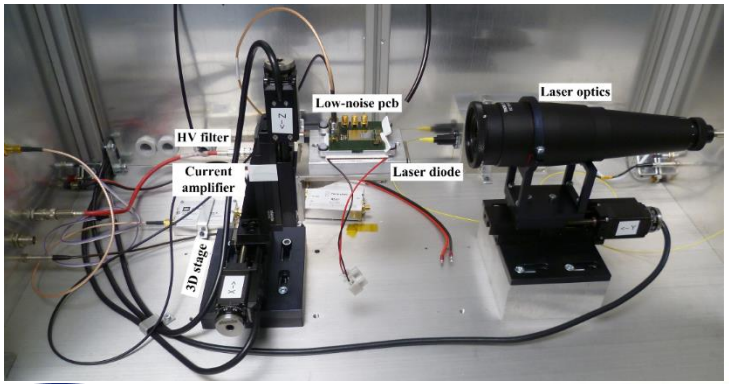
H35DEMO - e-TCT measurements



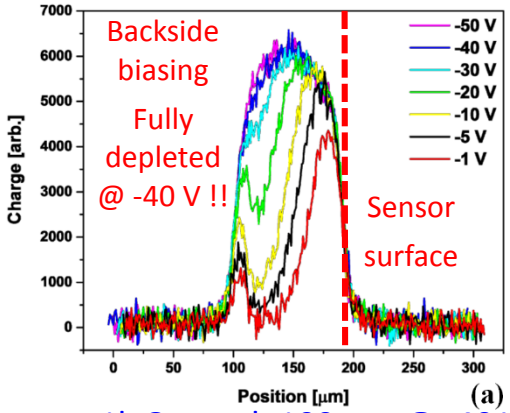
No circuitry or metal layers on top of the sensing diodes



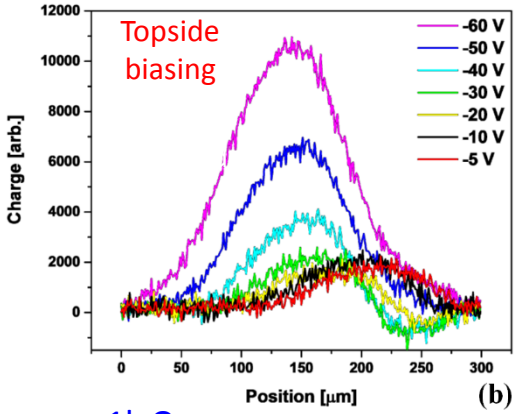
e-TCT set-up:



Measured results:

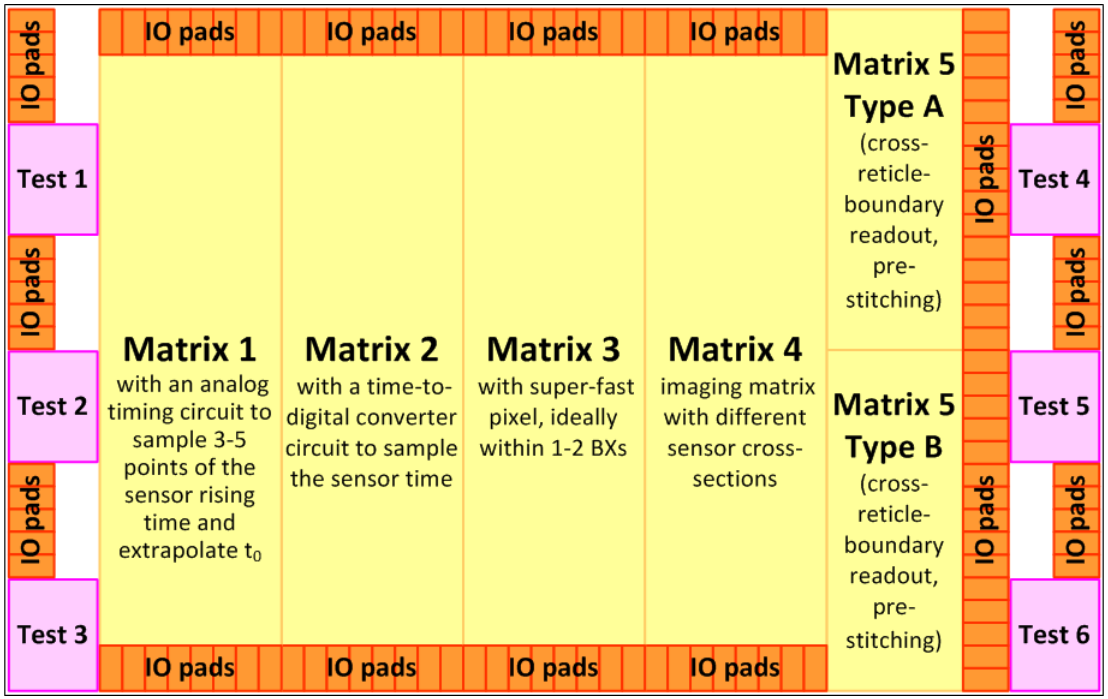


ρ=1k Ω·cm, d~100 µm @ -40 V



ρ=1k Ω·cm

HV-CMOS submission within RD50 collaboration



RD50

Design effort:

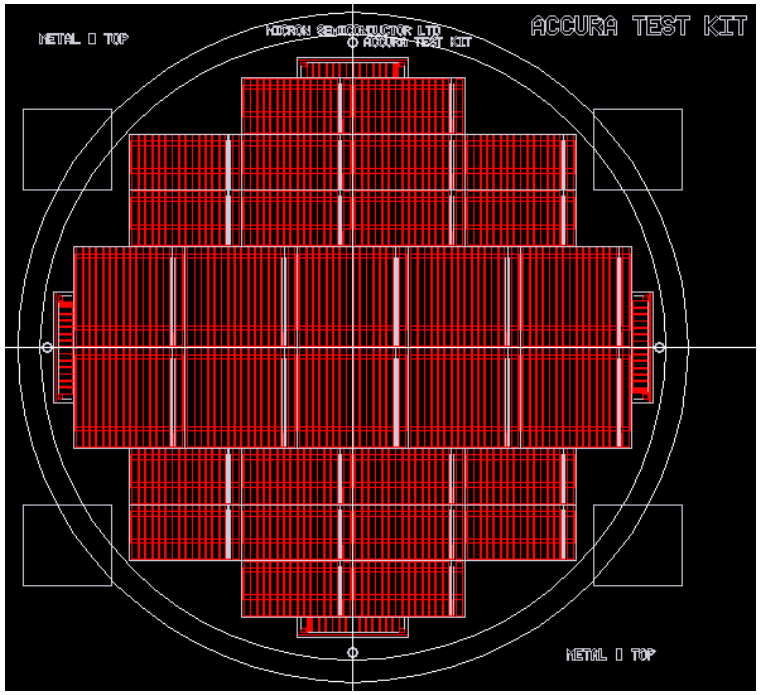
IFAE
R. Casanova
Uni. Barcelona
O. Alonso
Uni. Liverpool
S. Powell
E. Vilella
C. Zhang

Scope for further design contributions…

Test structure 1	Simple CMOS capacitors to study oxide thickness
Test structure 2	10 x 10 matrix of very small pixels with passive readout
Test structure 3	10 x 10 matrix of very small pixels with 3T-like readout
Test structure 4	Small matrix of pixels for TCT, e-TCT and TPA-TCT measurements
Test structure 5	Single pixels for sensor capacitance measurements
Test structure 6	…

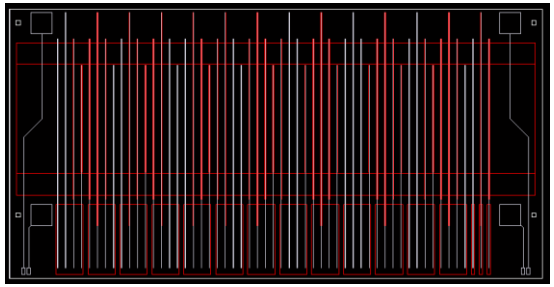
Accµra100 flip-chip bonder and test kit

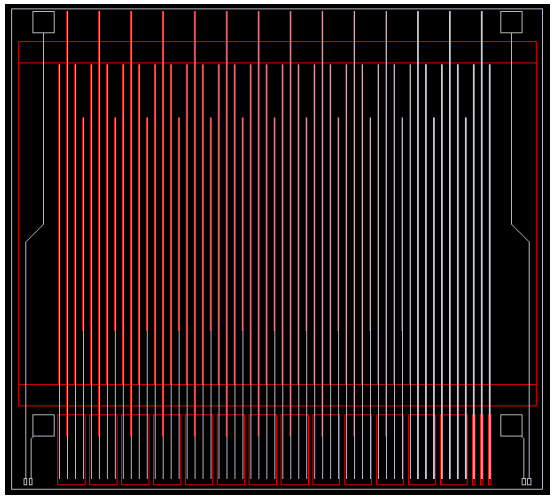
Accµra100 flip-chip bonder



Metal-on-Glass process
6-inch wafer submitted to Micron Semiconductor Ltd (March 2017)

20x test structures (RD53 chip size) for 10 trials of flip chip bonding



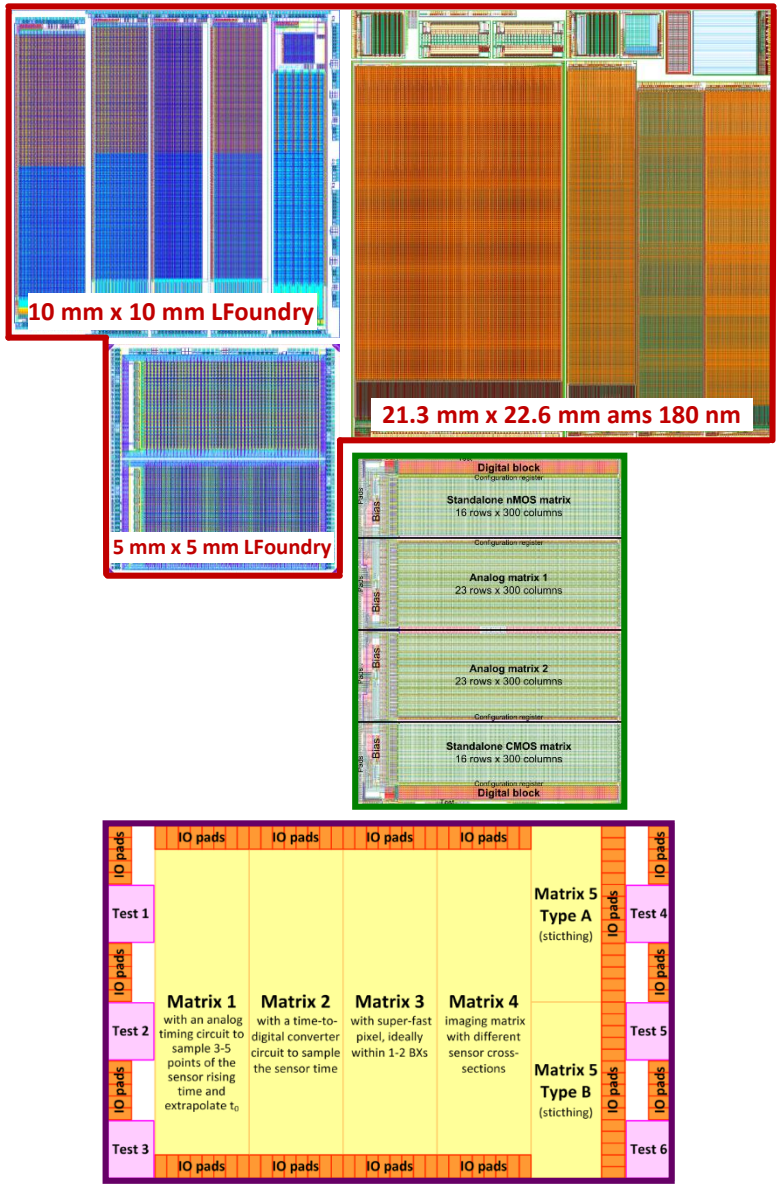


10x test structures (FE-I4 chip size) for 5 trials of flip chip bonding

- The original plan is to align and glue 2 parts together and to characterise their coupling by accurate capacitance measurements.

Summary

- **Several HV-CMOS submissions in 2016:**
  - 10 mm x 10 mm HV-MAPS ASIC in LFoundry 150 nm via MPW
  - 5 mm x 5 mm HV-MAPS ASIC in LFoundry 150 nm via MPW
  - 21.3 mm x 22.6 mm HV-MAPS ASIC in ams 180 nm via engineering run
- The fabricated ASICs are expected during **the first quarter of 2017**
  - PCBs to design
  - Firmware to write
  - Many many measurements to be done
- **H35DEMO measurements** are on-going
- Working towards a **new HV-MAPS submission** within the RD50 collaboration
- New **Accura100 flip-chip bonder** and test kit



Thank you for your attention !