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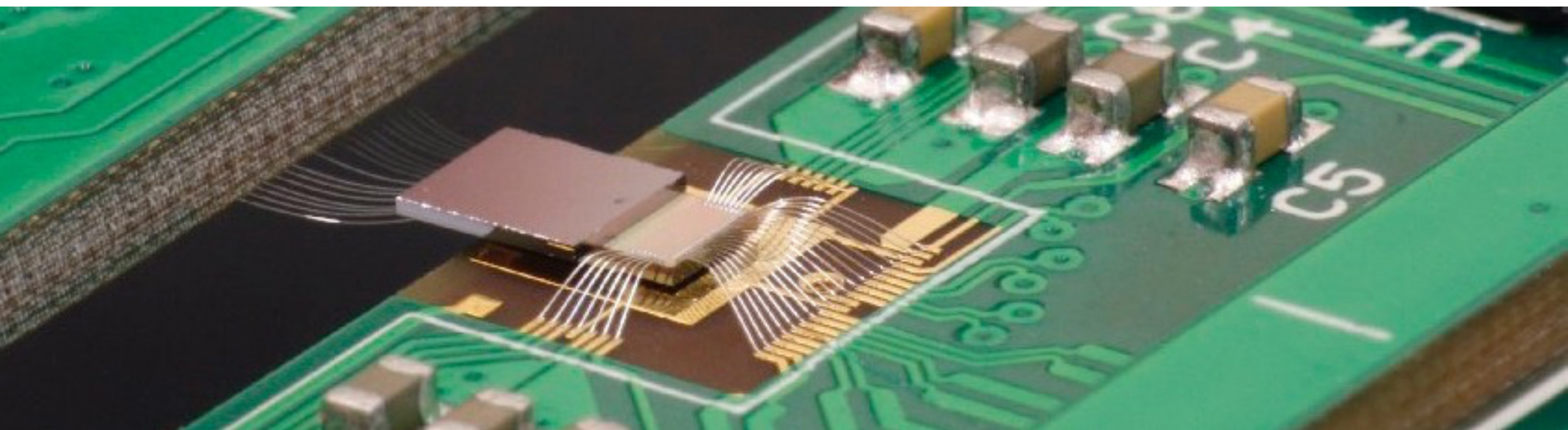
Status of HV-CMOS developments
for the CLIC vertex detector



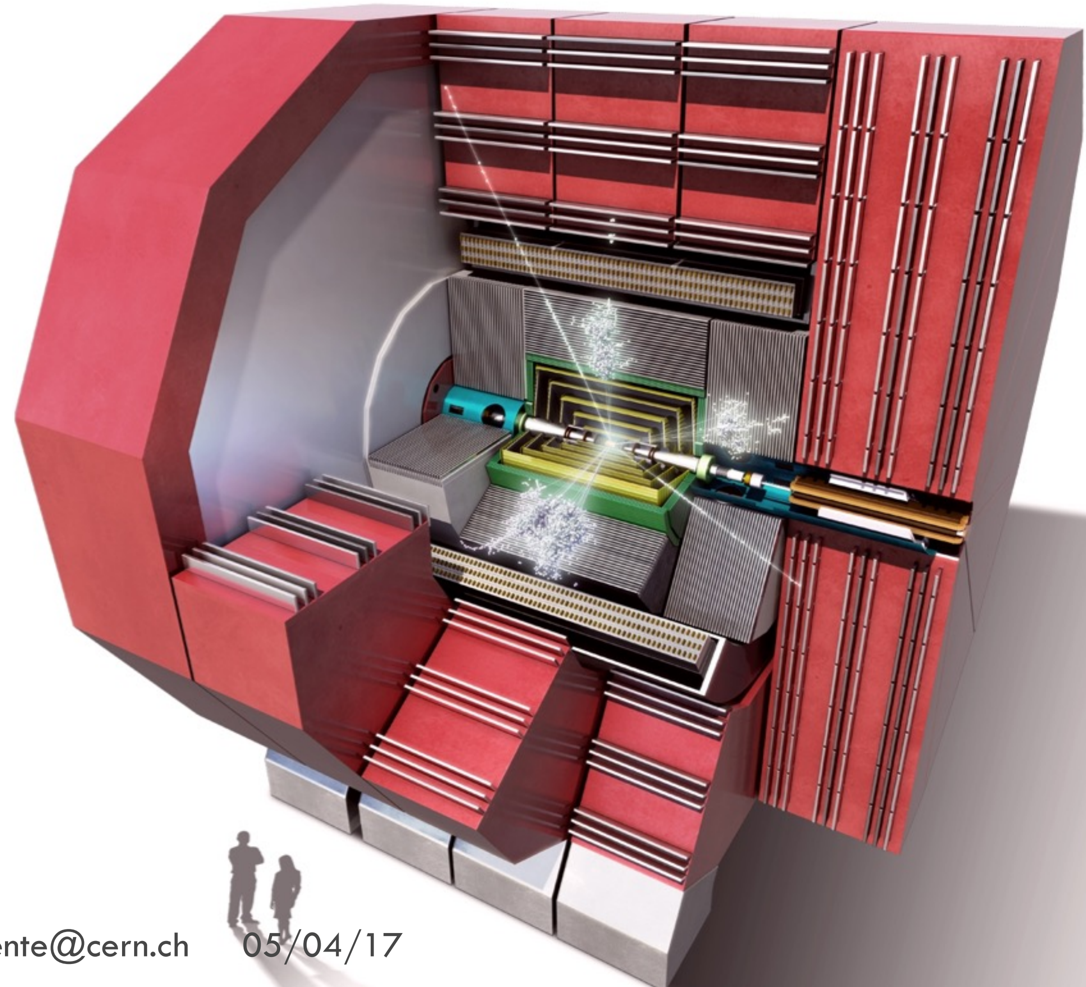
CLICpix + CCPDv3. Szymon Kulis - http://skulis.web.cern.ch/skulis/clicpix/

AIDA2020 – WP6
05/04/2017

Mateus Vicente (UniGE/CERN)
on behalf of the CLICdp collaboration

Outline

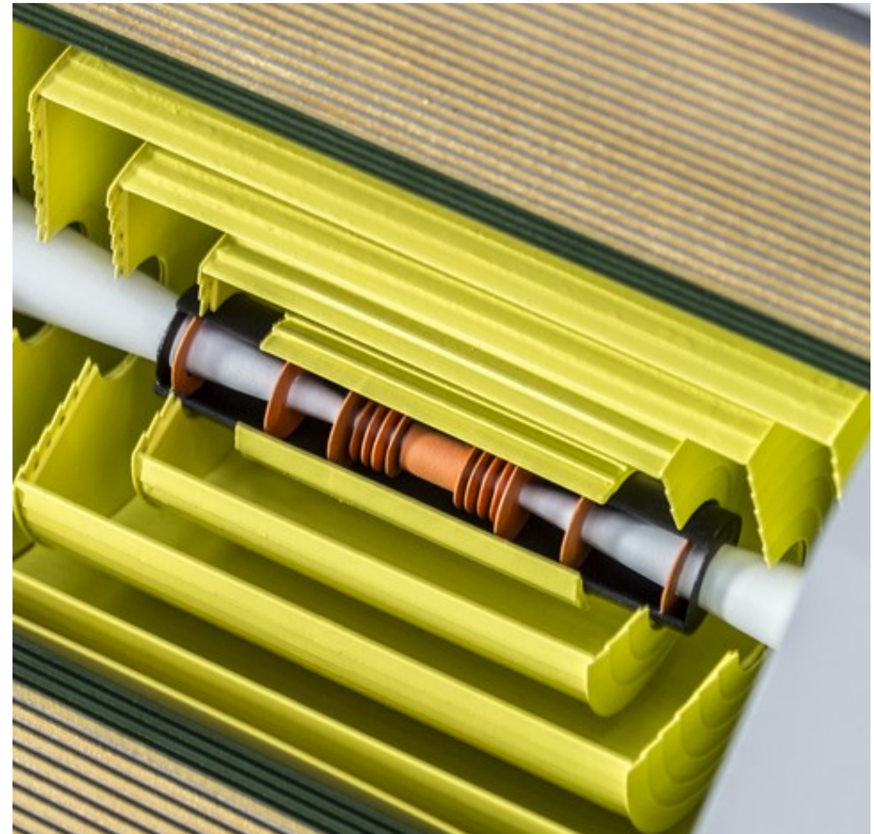
- CLIC Vertex Detector
- 1st Generation chips
  - CLICpix + CCPDv3
  - Designs and simulations
  - Assembly and testbeam
- 2nd Generation chips
  - CLICpix2
  - C3PD
- New Caribou DAQ system
- Summary and Conclusions



CLIC Vertex Detector

and requirements

- All-silicon vertex and tracking detector
- Demanding performance requirements for the vertex detector
  - Ultra low mass, **0.2% X0** per layer
  - Single hit resolution of ~**3 µm**
  - Time-stamping of **10 ns**
  - Power consumption of **50 mW/cm2**
    - + **0.2% X0** requirement = **Forced air cooling**
- R&D aimed in hybrid pixel detectors
  - Thin planar or capacitively coupled **HV-CMOS**
  - Pixel size of **25 µm × 25 µm**
  - ASIC and sensor thickness of **50 µm** (each)

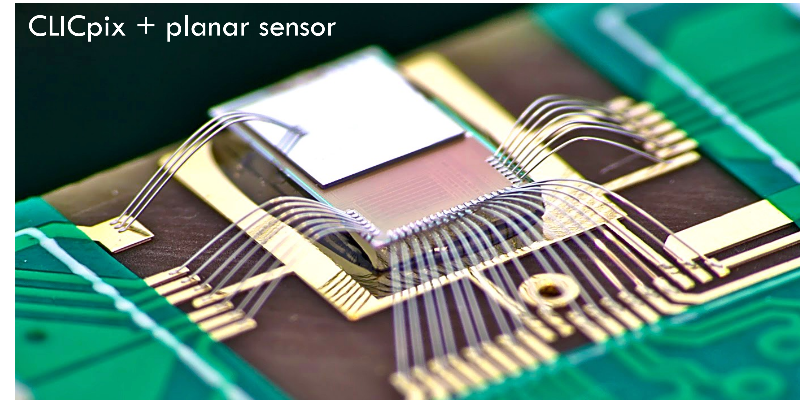


CLICpix Readout ASIC

for planar and HV-CMOS sensors

- Implemented in a 65 nm CMOS process
  - Based on the Timepix/Medipix chip family
- Demonstrator chip with 64×64 Pixel matrix
- Pixel size is 25×25 µm
  - Total active area is 1.6×1.6 mm^2
- 4-bit ToA and ToT measurements
  - Per pixel, simultaneously
- Time stamping < 10 ns
  - Full readout in < 800 µs
    - for 10% occupancy @ 320 MHz readout clock
- Power pulsing scheme

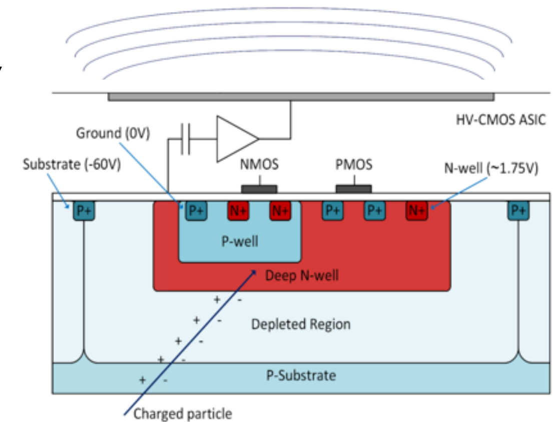
Parameter	Simulated Value	Measured Value
ToA Accuracy	< 10 ns	< 10 ns
Gain	44 mV/ke$^-$	40 mV/ke$^-$
Dynamic Range	up to 40 ke$^-$	up to 45 ke$^-$
Equivalent Noise (bare chip)	$\sigma = 60e^-$	$\sigma = 51e^-$ (average)
DC Spread (uncalibrated)	$\sigma = 160e^-$	$\sigma = 128e^-$
DC Spread (calibrated)	$\sigma = 24e^-$	$\sigma = 22e^-$
Minimum threshold	388 e^-	417 e^-
Power consumption per pixel	6.5 μW	7 μW

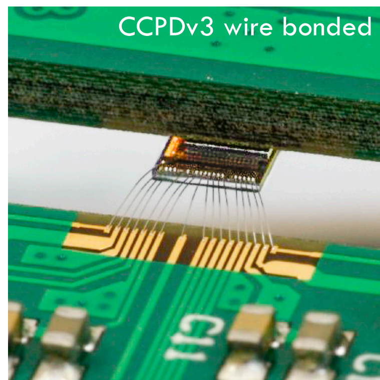


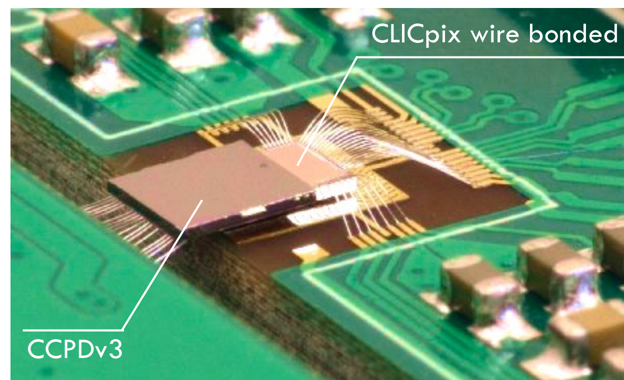
CCPDv3 Sensor ASIC

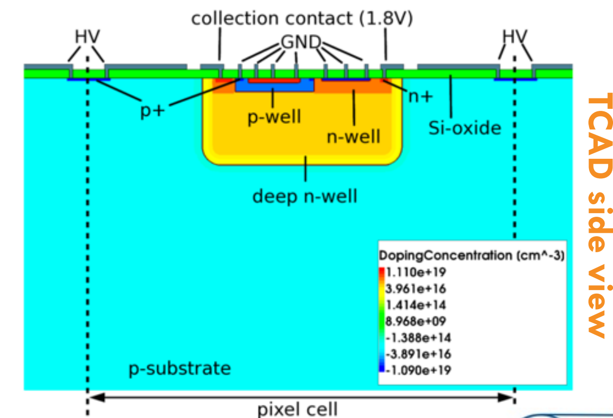
HV-CMOS sensor

- Fabricated in a 180 nm commercial HV-CMOS technology
- Matching the CLICpix 64×64 pixel matrix
  - Pixel size also is 25×25 µm
- Two stages amplifier on each pixel
- Capacitively coupled (glued) to the CLICpix chip
  - Flip-chip with Epoxy glue instead of bump-bonds







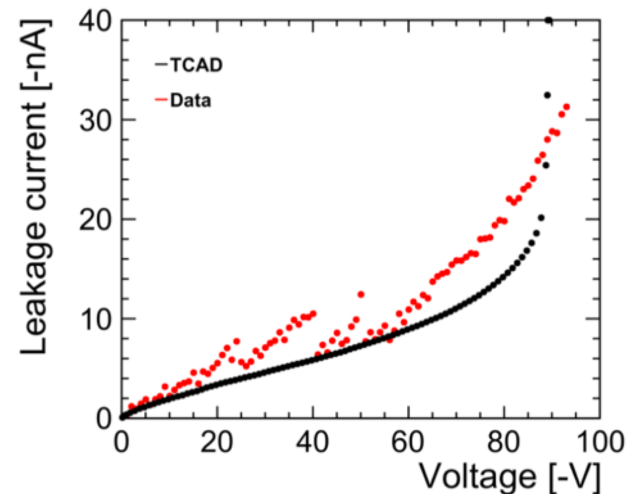


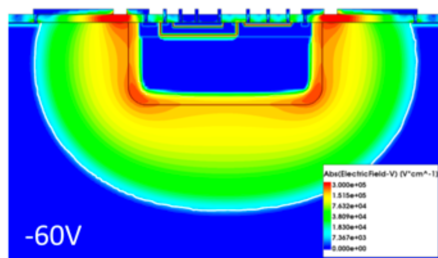
TCAD side view

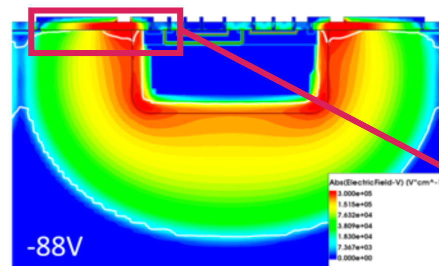
CCPDv3 TCAD Simulations

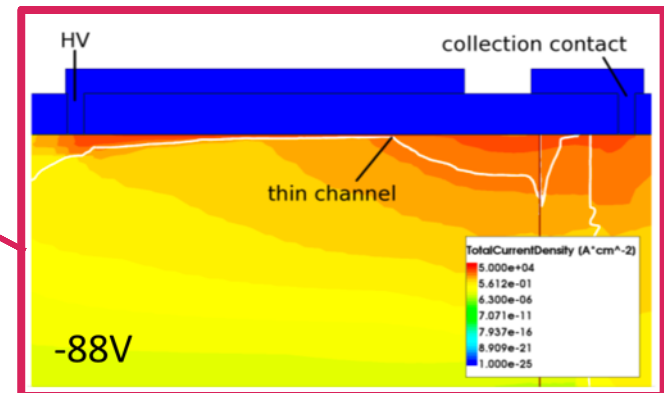
Sensor IV

- Possibility to study pixel design and resulting breakdown
  - Both current and breakdown reproduced well in simulations
    - Breakdown: Data -93V vs TCAD -88V
  - At high enough bias distortion of depletion region, allows thin channel to short HV and deep n-well





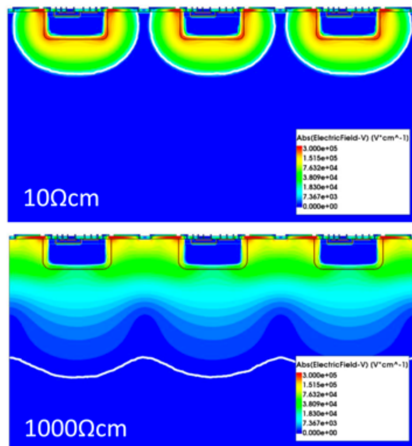


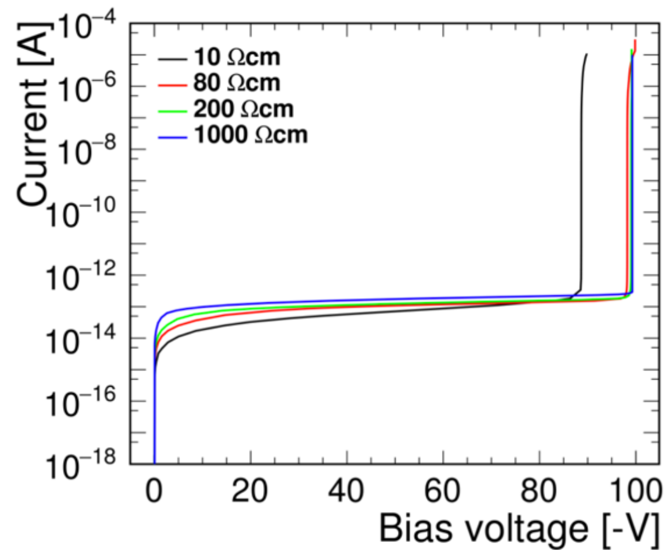


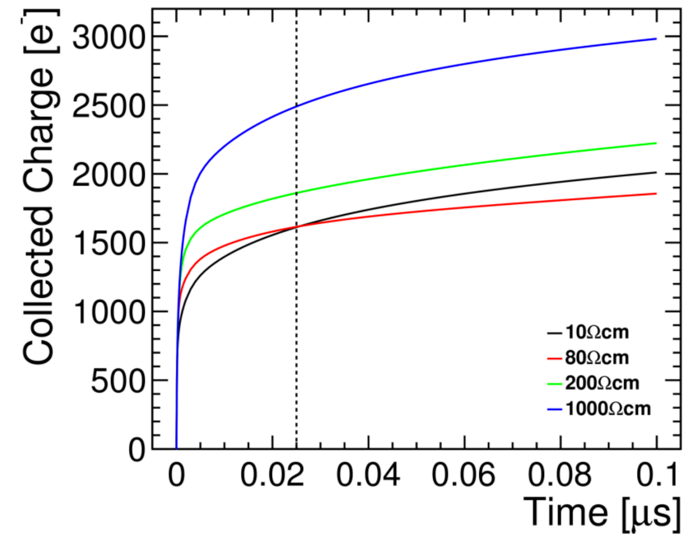
CCPDv3 TCAD Simulations

Sensor Possible Improvements - Resistivity

- Change the resistivity of the substrate
  - Increase in the depletion depth
  - Larger breakdown voltage and Faster and more charge collection
    - 1000 Ohm*cm model collecting around 50% more than the 10 Ohm*cm model after 100 ns.



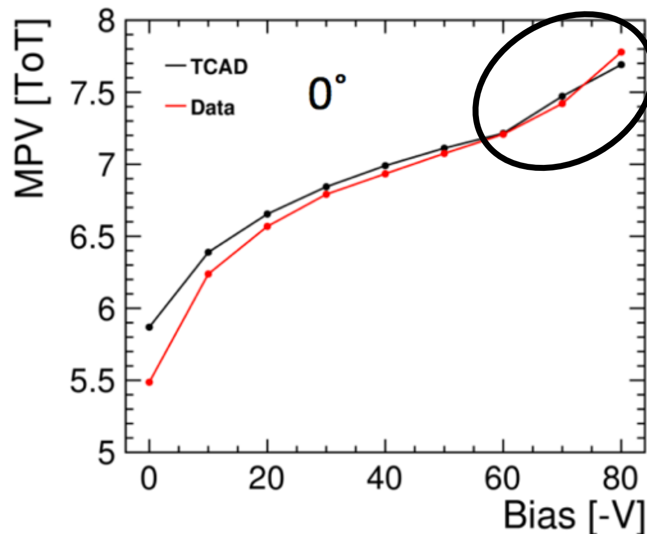


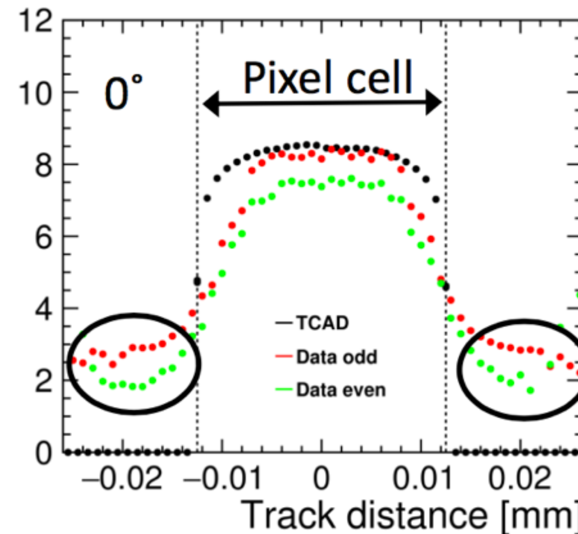


CCPDv3 TCAD Simulations

VS test-beam data – Charge collection

- Comparison between simulation and test beam data
  - Calibrations of the device are used to convert TCAD output to ToT
  - MPV for single pixel clusters
  - Increase in gradient for voltages > 60 V due to **avalanche multiplication**
  - ToT of ~3 at sides due to **cross-coupling** (not included on TCAD simulations)



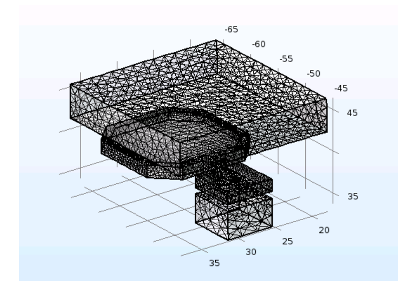


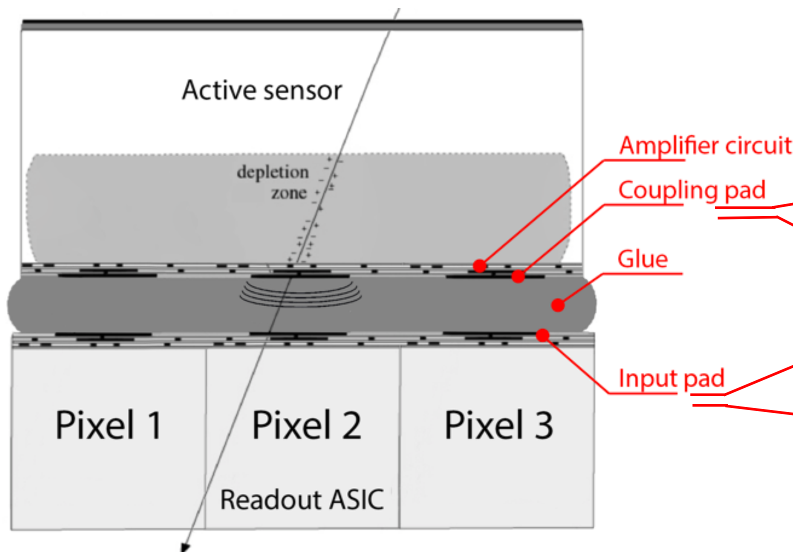
CCPDv3 FEM Simulations

Coupling with CLICpix

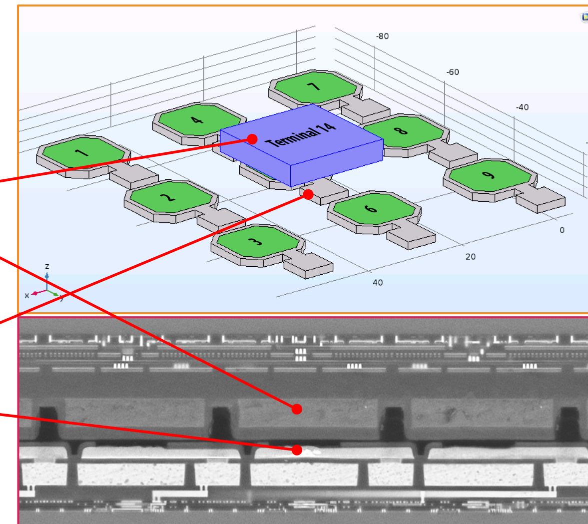
- Signal transfer from the sensor to the ROC via a capacitive injection
  - Issue of cross talk/coupling to neighbouring pixels must be considered
  - 3D simulation, using the *Finite Element Analysis* method (with COMSOL)
    - Effect of different glue layer thickness, pixels misalignment and different pixel pads design

Mesh of pixel pads





CLICpix+CCPDv3 pixel pads



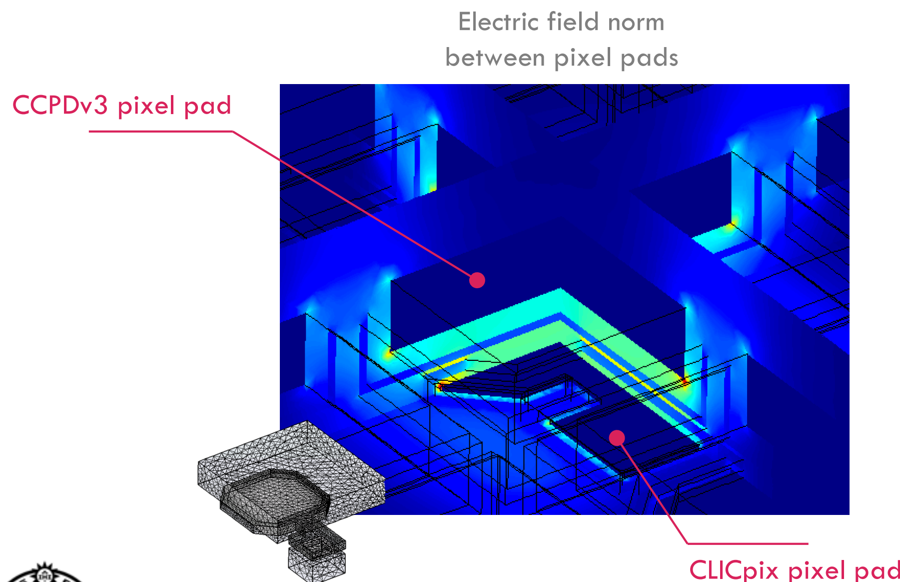
Scanning Electron Microscope picture of CLICpix+CCPDv3 assembly cross section

CCPDv3 FEM Simulations

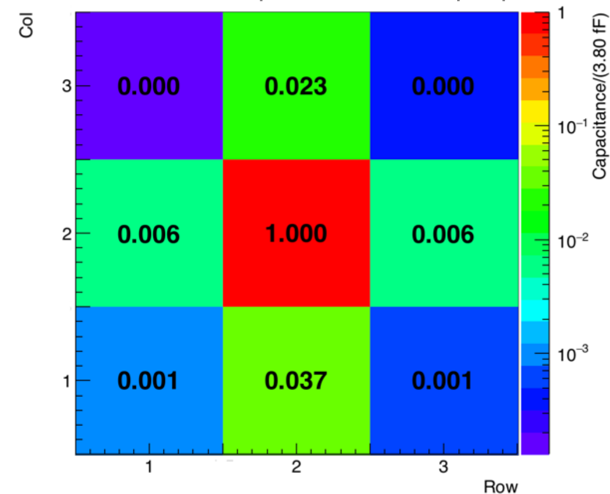
Coupling with CLICpix

- Capacitance calculated from the Electric energy density between pixel pads
  - Capacitance to closest pixel: 3.8 fF
    - For a gap of 0.22 um (measured from the SEM pictures) between the chips
  - Cross capacitance < 4% to neighboring pixels
  - Asymmetric cross capacitance due to pixel pads geometry

Electric field norm between pixel pads

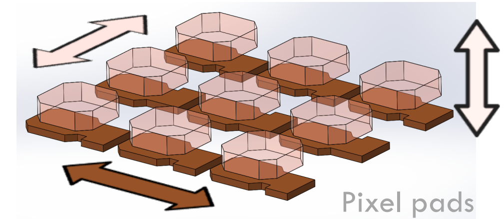


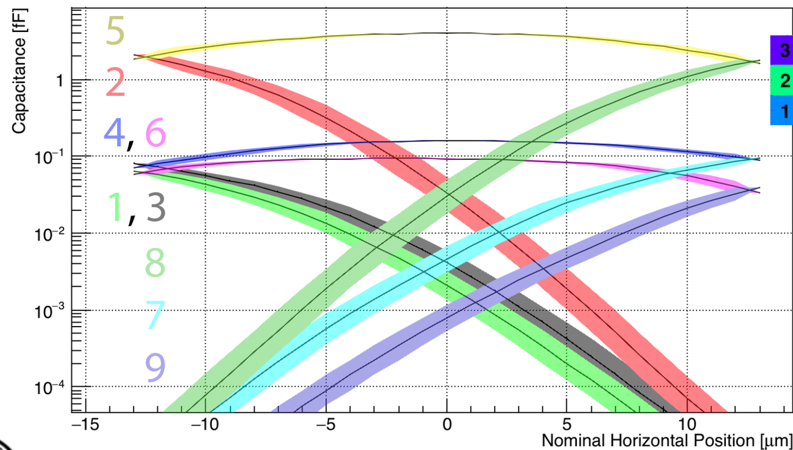
(Normalized (to 3.8 fF)) Capacitance between CCPDv3 central pixel and 9 CLICpix pixels

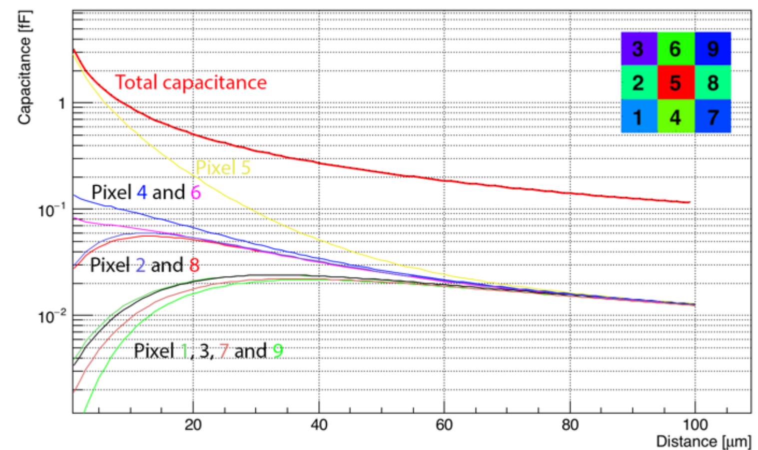


CCPDv3 FEM Simulations
Cross-coupling with CLICpix - Misalignment

- Possibility of study alignment effects on the capacitances
  - Simulations with planar misalignment or different glue thickness
    - Possibility to study and improve charge sharing on the signal transmission
  - Comparison with test beam data on going
    - As expected, assemblies with half pixel misalignment has two pixels on the RO chip with same capacitance
      - Uncertainty bands on left plot corresponds to the assumed alignment precision of +- 1 um
    - Typical gap between chips bump-bonded (~20um) would result in a coupling capacitance about 10x smaller for the closest pixel







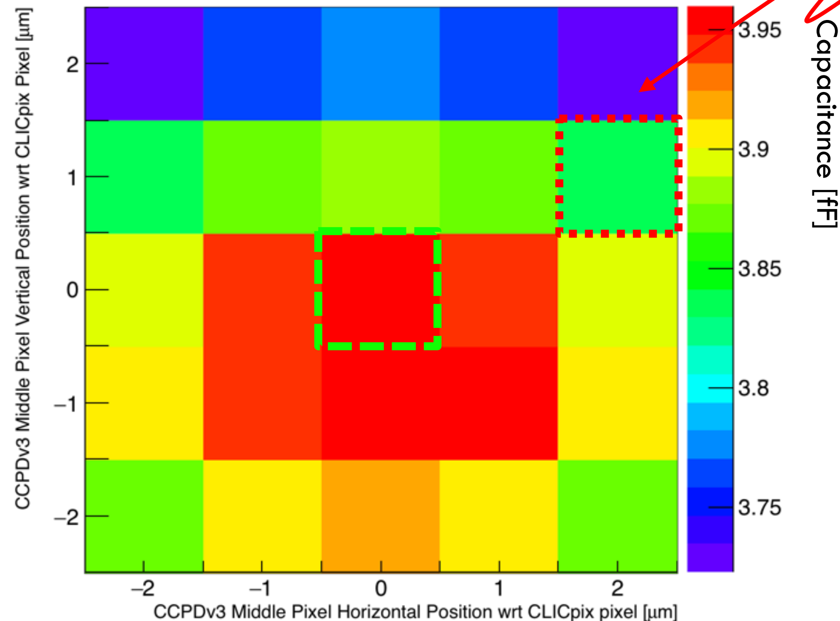
CCPDv3 FEM Simulations

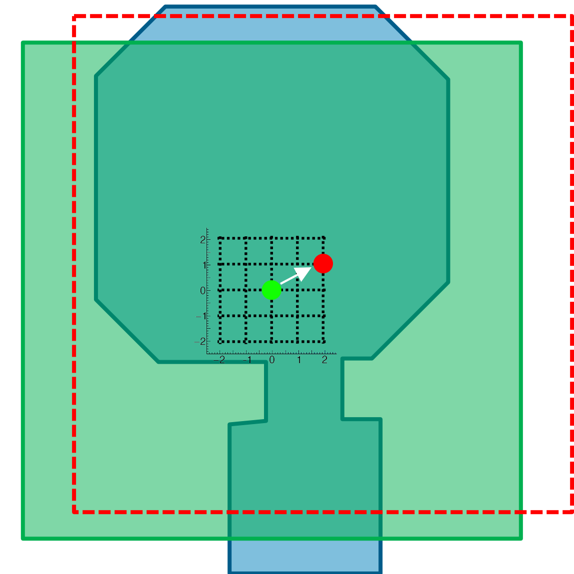
Cross-coupling with CLICpix - Misalignment

- 2D alignment scan - Simulate the effect of the precision on the flip-chip process
  - ±2um X and Y uncertainty simulated
    - Capacitance coupling drops by 200 aF (~5%)

Misaligned (+2,+1) CCPDv3 pixel pad

Centered CCPDv3 pixel pad





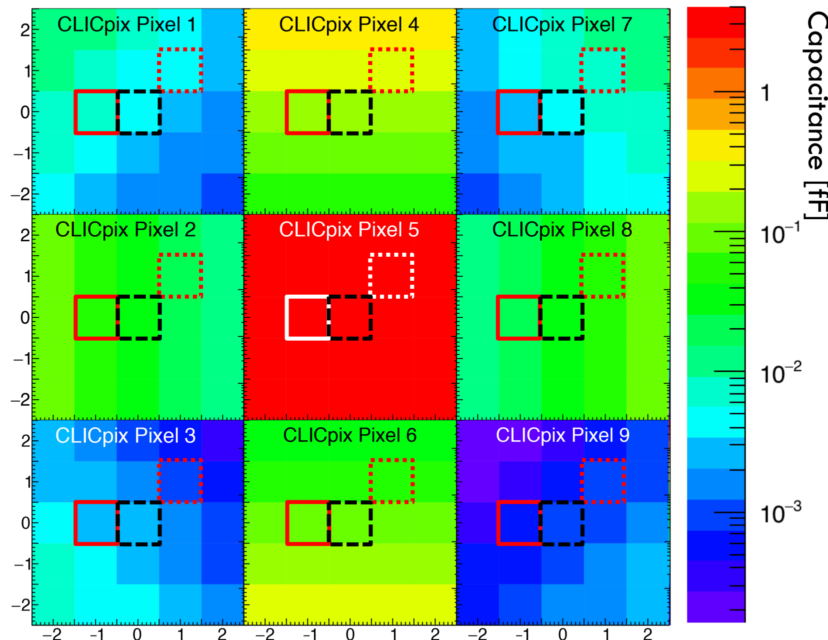
CLICpix pixel pad

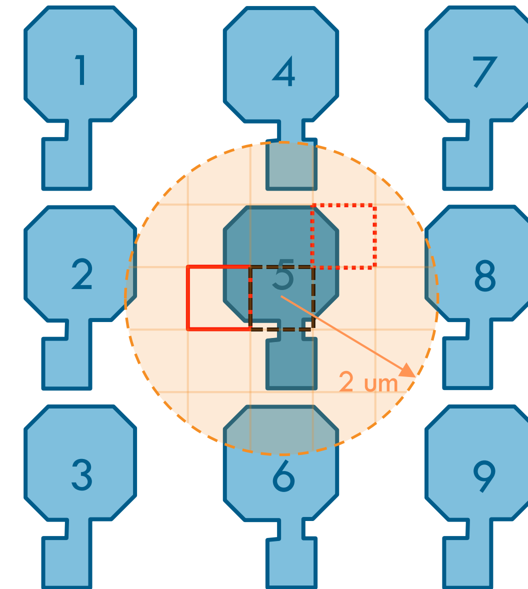
CCPDv3 pixel pad

CCPDv3 FEM Simulations

Cross-coupling with CLICpix - Misalignment

- 2D alignment scan - Simulate the effect of the precision on the flip-chip process
  - ±2um X and Y uncertainty on CCPDv3 pixels position
    - No major effect for CLICpix central pixel
    - Pixels 4 and 6 most affected (effect seen in TB data)
      - Pixel 4 [0.05, **0.15**, 0.36] and Pixel6 [0.23, **0.09**, 0.02] **fF**

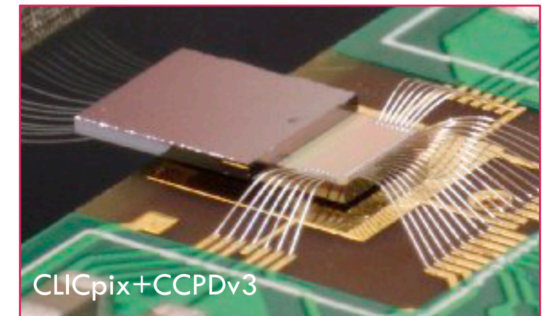




Flip-chip at UniGE

CLICpix + CCPDv3

- Heating up to **400 degC** and force applied by bonding arm up to **100 kg**
  - CLICpix+CCPDv3: **100 degC** (for **6 min**) and **5N bonding force**
    - *Manual glue deposition on CCPDv3
- XY Alignment stage with resolution of **0.015 um**
- Post bonding accuracy **~<1 um** achieved
  - < 0.5 um (theoretically)
  - PixelShop pattern-recognition program to guide alignment



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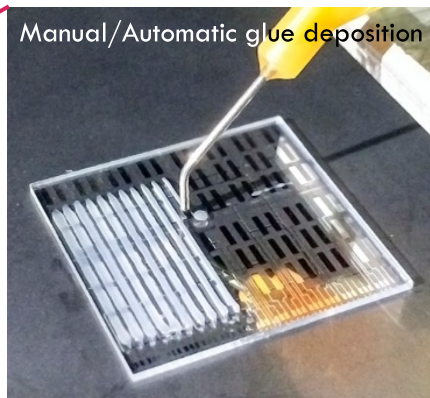
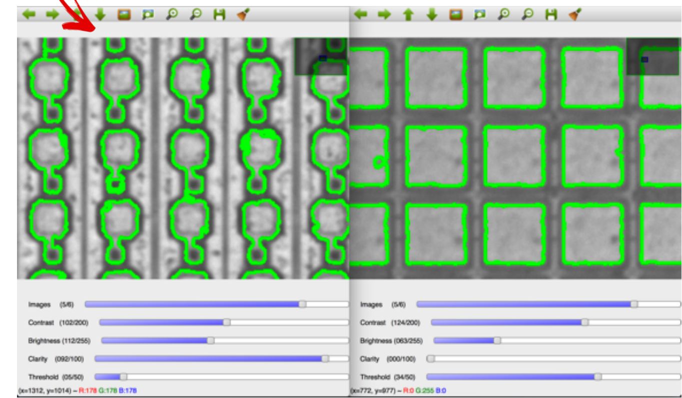


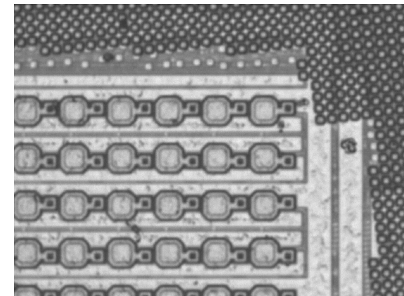


Flip-chip at UniGE

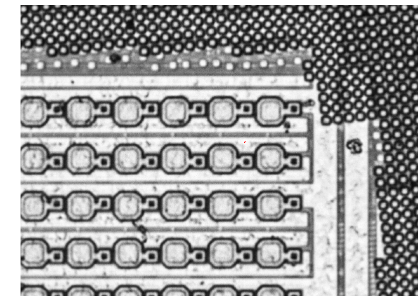
CLICpix + CCPDv3 with PixelShop

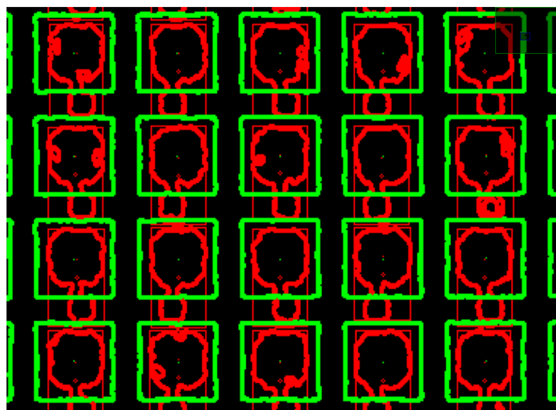
- PixelShop
  - Pictures from flip-chip digital cameras
    - 2 cameras with field of view of 900x700um
      - 0.37 um/pixel
  - C++ and OpenCV framework
    - Enhance pictures contrast for better contour finding
    - Calculate offset between contour geometric center

CLICpix original picure



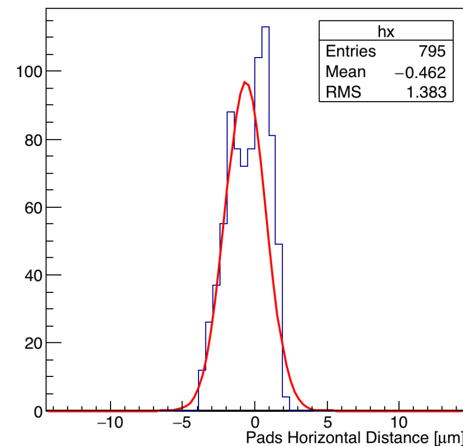
CLICpix edited picure



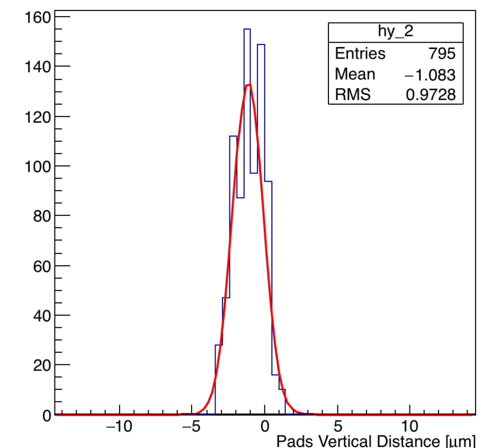


Pixel pads contours
CLICpix and CCPDv3

Horizontal pads offset

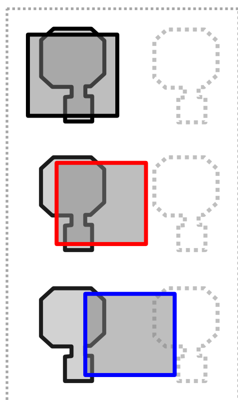


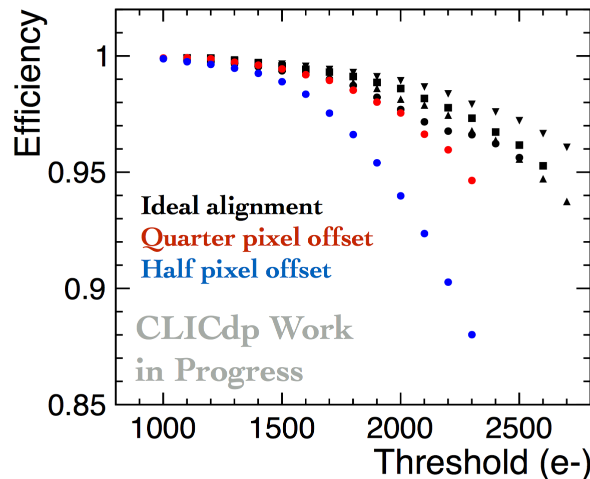
Vertical pads offset

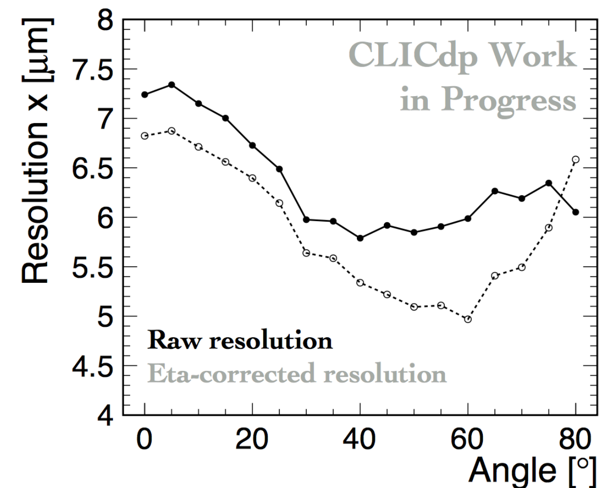


Testbeam Results
with CLICpix + CCPDv3

- Samples produced with different alignment to gauge sensitivity of device performance to glueing precision
  - Performance remains good regardless of misalignment
    - Still efficient at target thresholds
- Beam incidence angle scan to test clustering and resolution in thin sensors
  - Not at the vertex requirement yet. Still some ground to cover



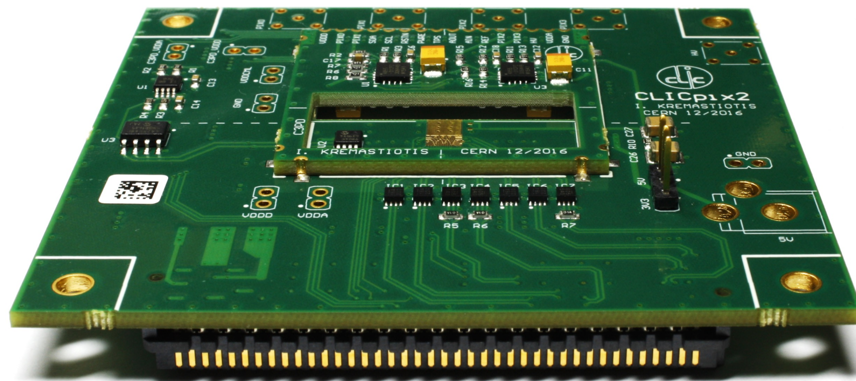


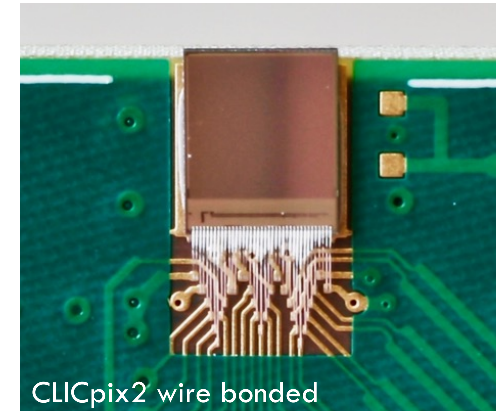


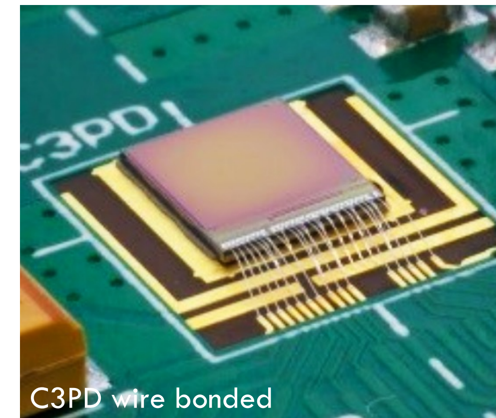
CLICpix2 and C3PD

2nd generation readout and sensor ASIC

- Improved chips based on previous CLICpix and CCPDv3
  - **C**LIC **C**apacitively **C**oupled **P**ixel **D**etector (C3PD) HV-CMOS sensor
  - Bigger pixel matrix
  - Different pixel electronics
  - Guard ring around HV-CMOS pixels pads
  - Measurements done in stand-alone mode
    - CLICpix2+C3PD Caribou chip board already in hands




CLICpix2 wire bonded


C3PD wire bonded

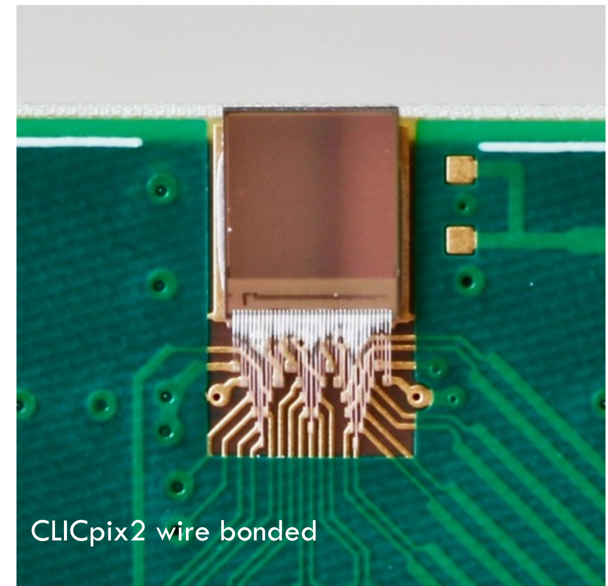
CLICpix2
Readout chip

- CLICpix2 Overview

	CLICpix	**CLICpix2**
Matrix size [pixels]	64 × 64	**128 × 128**
Active area [mm^2]	1.6 × 1.6	**3.2 × 3.2**
ToT counter	4 bits	**5 bits**
ToA counter	4 bits	**8 bits**

- Operation with counters combined, giving 13-bit timing
  - 82 µs depth with 100 MHz clock
- Improved noise isolation and removal of cross-talk issue
- Parallel column readout and 8/10 bit encoding
- Integrated test pulse DACs and band-gap
- First chips received at CERN mid-Feb
  - Comissioning on-going

Power domain	simulation	**measurement**
VDDA *(1.2 V)*	110 mA	**104 mA (-5%)**
VDDD *(1.2 V)*	97 mA	N/A
VDD_CML *(1.2 V)*	31 mA	**33 mA (+6%)**

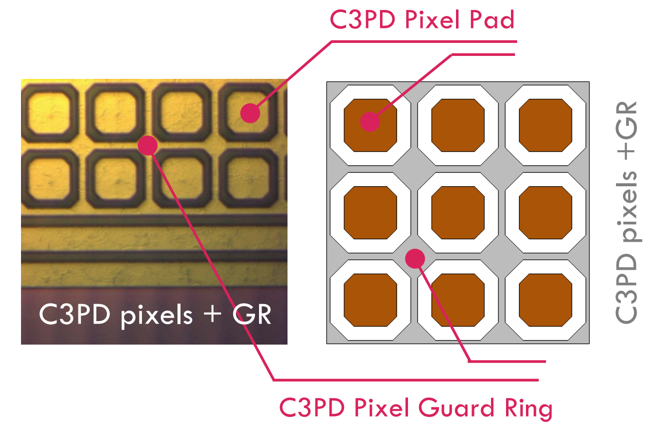

CLICpix2 wire bonded

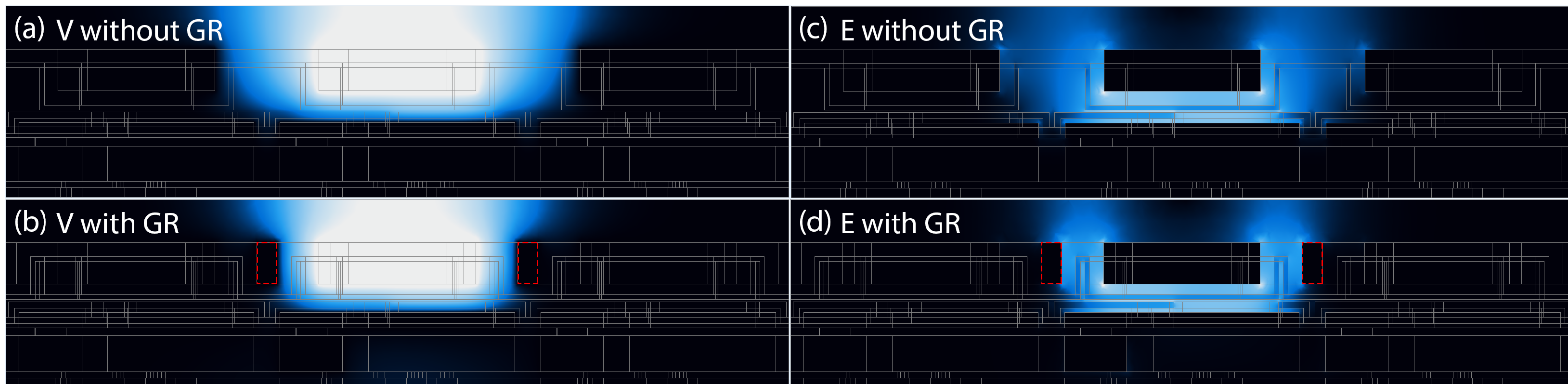
C3PD

New Output Pads Guard Ring

- C3PD Pixel output pads guard ring
  - Shield neighboring CLICpix2/C3PD pixel pads
    - Cross-couplig capacitance ~10X smaller

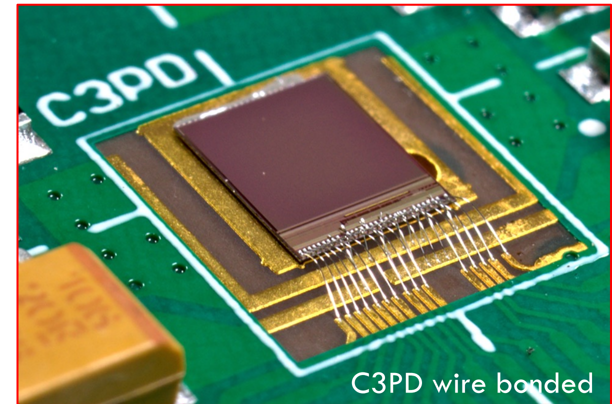
	Pixel 4	Pixel 5	Pixel 6	Metal lines	GR
Without GR	96E-3	3.360	96E-3	854E-3	-x-
With GR	12E-3	3.4839	12E-3	398E-3	3.14



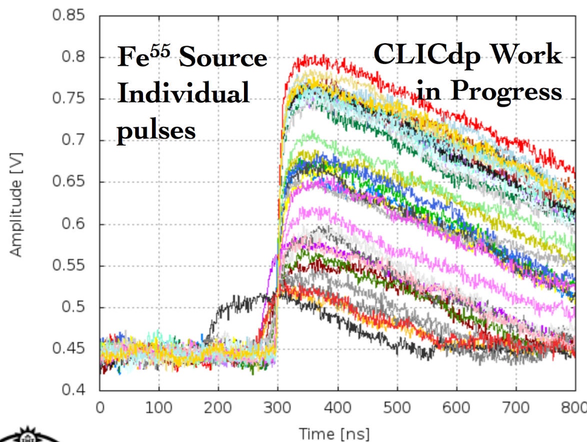


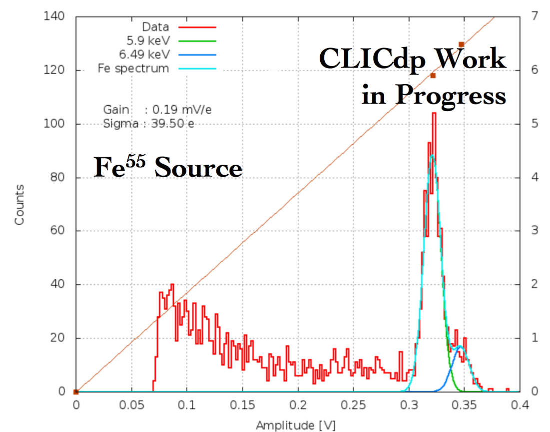
C3PD
Stand Alone measurements

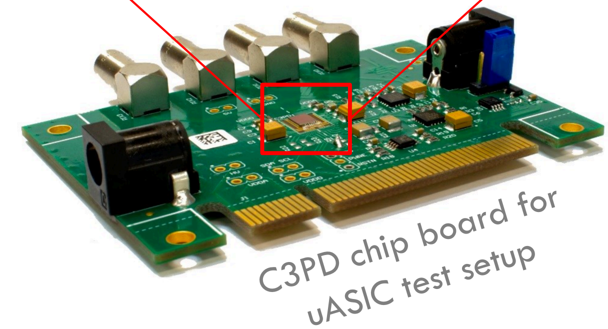
- C3PD Overview
  - 128x128 pixels with 25 µm pitch
  - 3 different flavours of pixels
  - Test 3x3 pixel matrix can be directly readout
  - Alignment marks for precise alignment with CLICpix2
  - Architectural changes to minimize power consumption



C3PD wire bonded





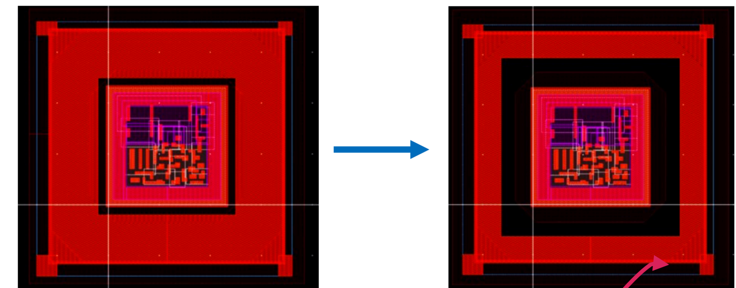

C3PD chip board for uASIC test setup

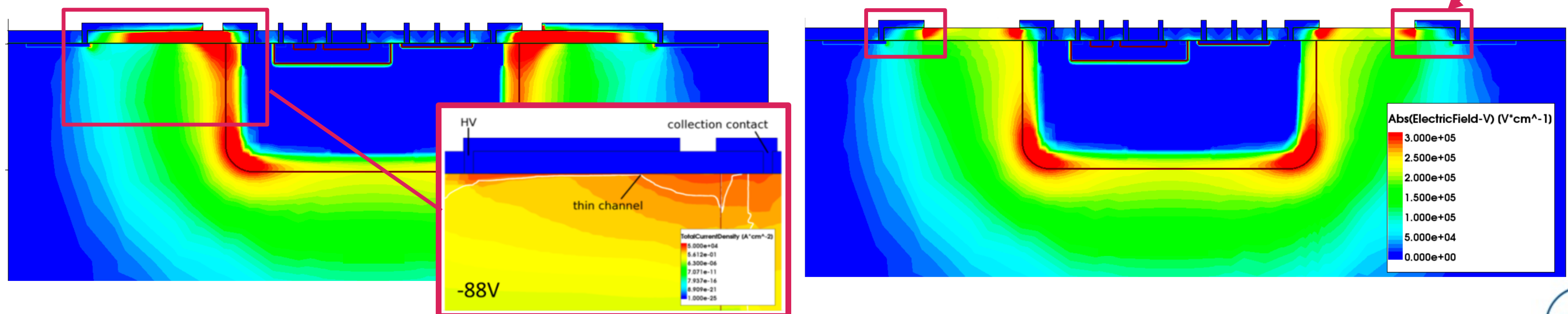
C3PD(v2)

Second submission

- C3PD first submitted in MPW on 20 Ωcm substrate
- New (C3PDv2) engineering run submission
  - 20, 80, 200 and 1kΩcm substrate resistivity
    - Will allow for validation of TCAD results
    - Expected arrival: Beginning of May
  - Thinned pixel HV guard ring ➔ higher breakdown voltage expected from TCAD simulations
    - Down to 2.62 μm from 4.82 μm
  - Higher substrate resistivity and higher biasing voltage will lead to a larger depleted volume and therefore a more efficient charge collection

C3PD pixel guard ring changing





CaRIBOu System

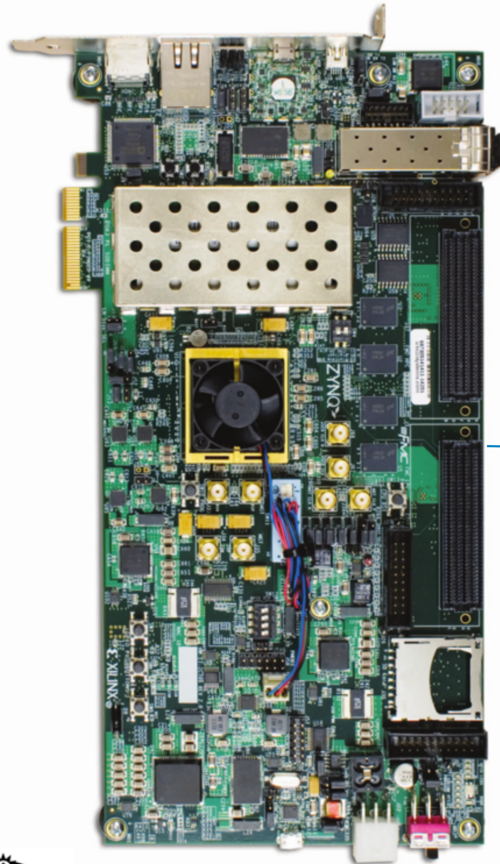
HV-CMOS DAQ – GITLAB LINK

- A modular readout system for pixel detectors
  - Developed at BNL with collaboration from UNIGE and CERN for ATLAS and CLIC
  - Open architecture welcomes contributions from other groups
  - Modular architecture allows for integration of new readout chips and sensors

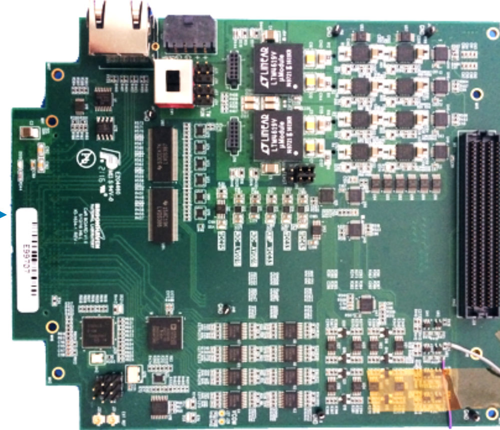
CaRIBOu System

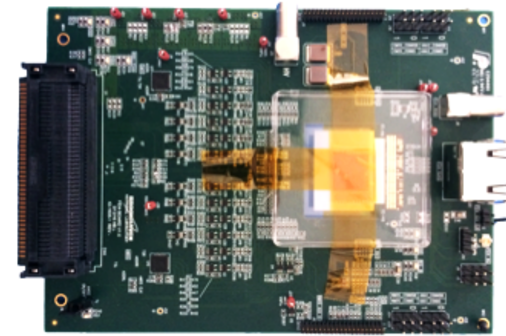
HV-CMOS DAQ – GITLAB LINK

ZC-706 FPGA Evaluation board

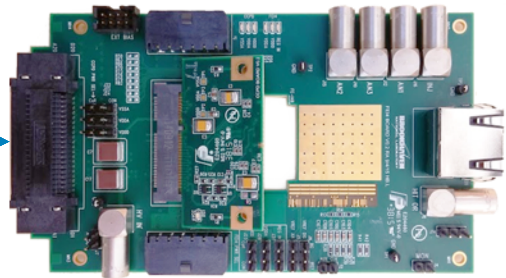


CaR board V1





FEI4 + H35DEMO

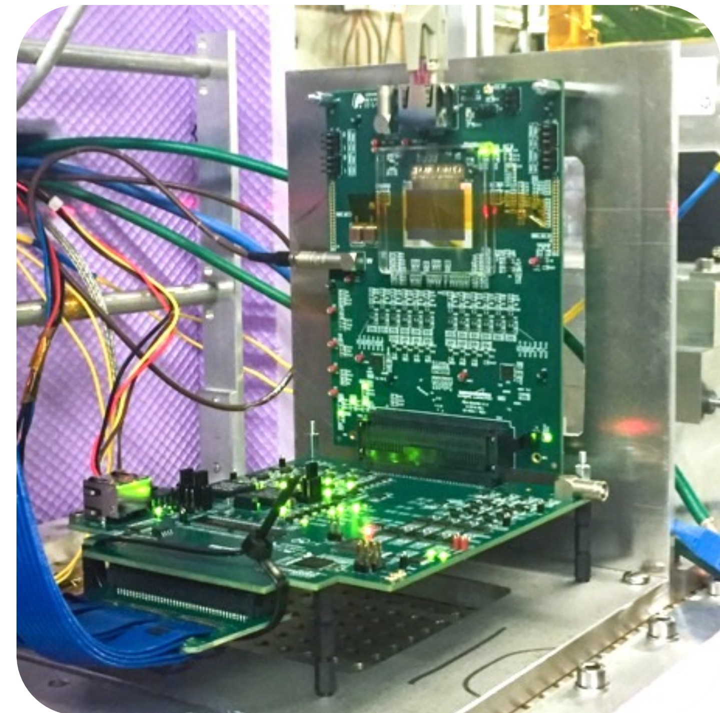


FE-I4 + CCPDv4,5 (CaR V0)

CLICpix2 + C3PD

CaRIBOu System
CaR board ressources

- 8 × general purpose power supplies with monitoring capabilities
- 32 × adjustable voltage output (0 — 4 V)
- 8 × current output (0 — 1 mA)
- 8 × voltage input (0 — 4 V)
- ADC (16 channels, 65 MSPS/14-bit)
- 4 × injection pulser
- I2C bus
- TLU RJ45 input (clock and trigger/shutter)
- general CMOS signals (10 × outputs, 14 × inputs)
  - with adjustable voltage levels (0.8 - 3.6V)
- 17 × LVDS pairs



FE-I4 + H35DEMO @ Fermilab 2017

Conclusions
and overview

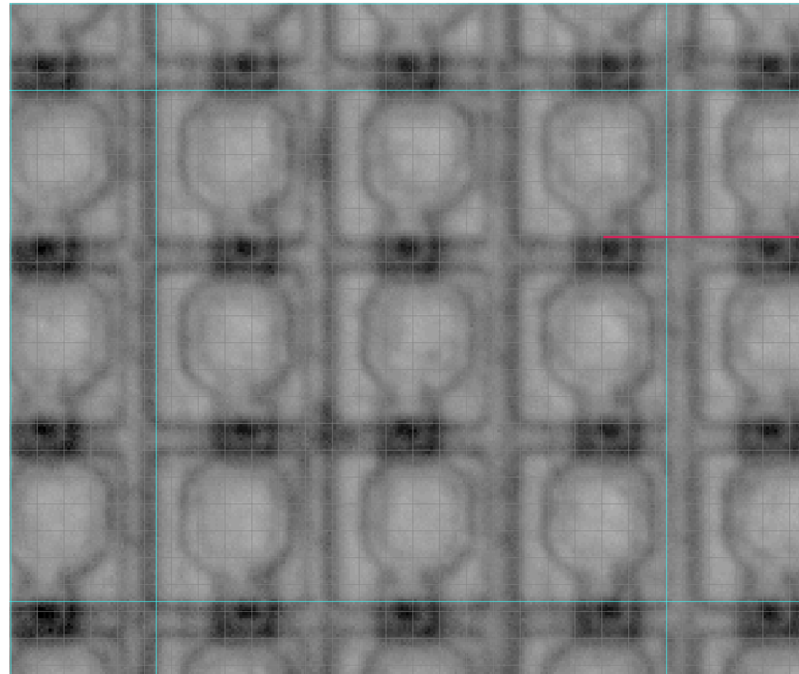
- CLIC vertex strong requirements introduced
  - HV-CMOS being investigated as sensor for the CLIC vertex detector
- CLICpix readout ASIC and CCPDv3 HV-CMOS chip first detector prototypes
  - TCAD simulations to predict sensor features
  - FEM simulations to understand pixels coupling between sensor and readout chips
- Preliminary test beam results
  - Results shows good control on the gluing process
  - Good efficiency at target threshold (even for misaligned samples)
    - Resolution requirement not yet achieved
- On-going work to test CLICpix2+C3PD on the next test beam campaign
  - Clicpix2 under comissioning
  - C3PD received and under test
    - C3PDv2 with new features to arrive in May
  - Caribou DAQ setup being commissioned for use

BACKUP

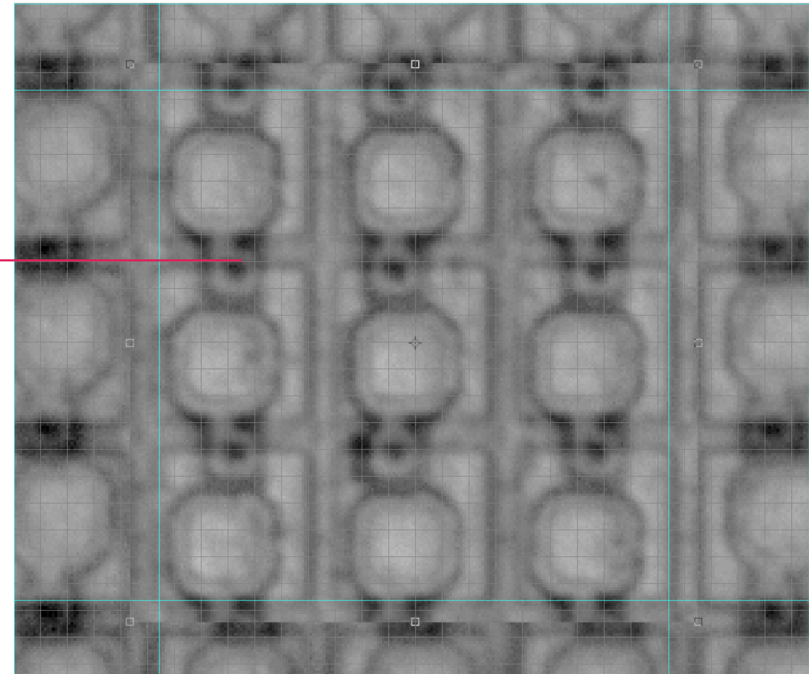
Lens Distortion

Check Superposing the Same Picture

Bottom left part of the picture

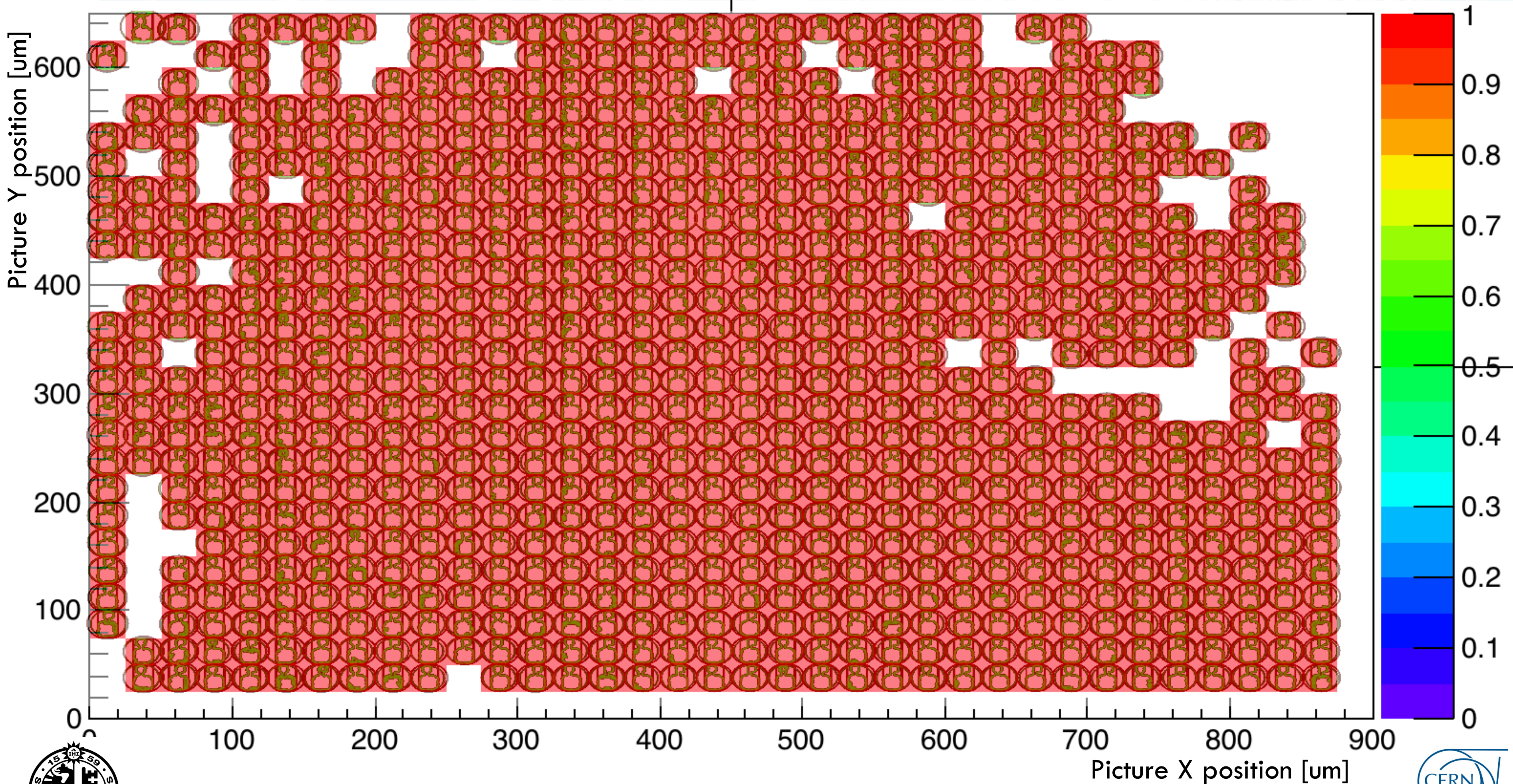


Top right corner pasted on top of bottom left



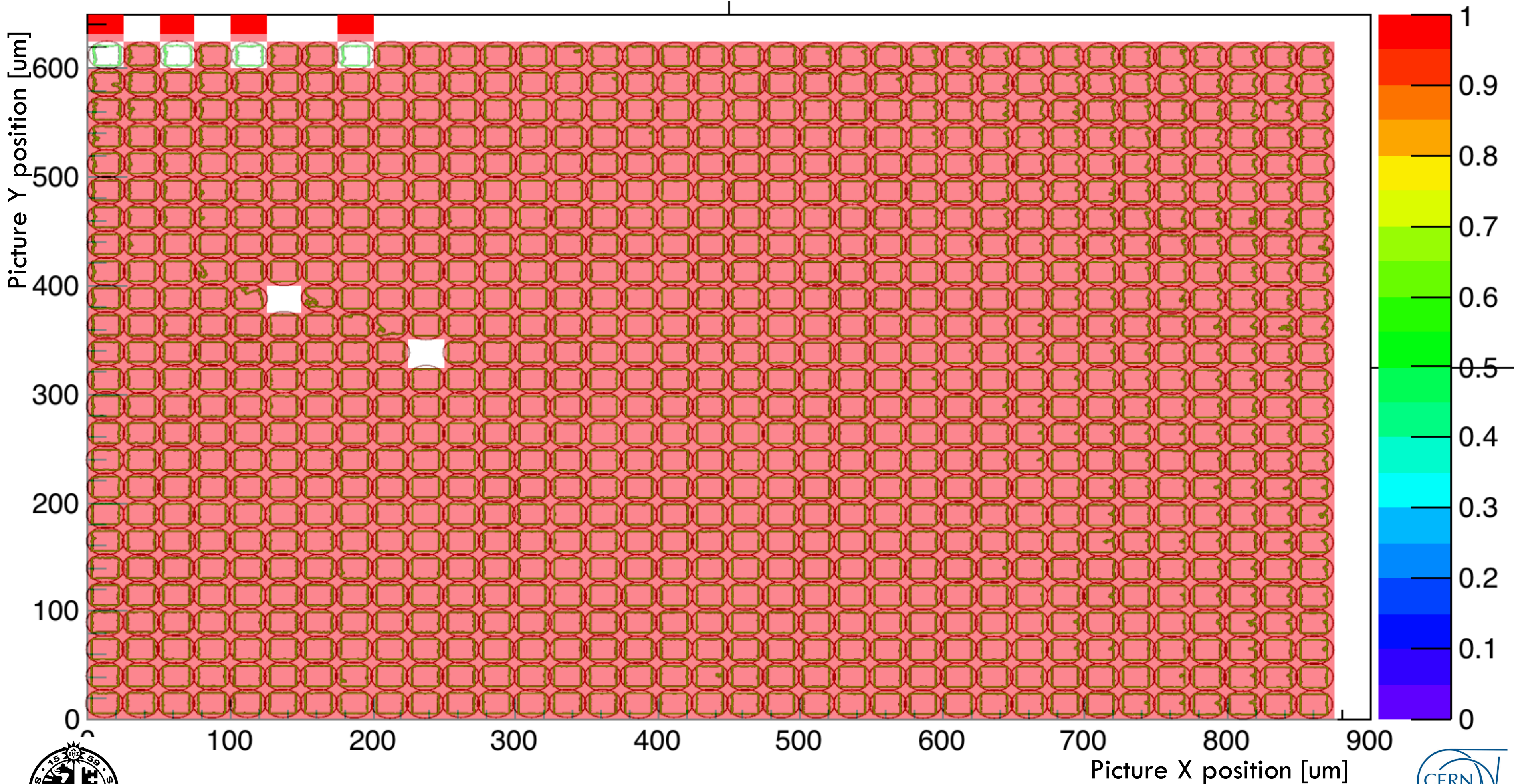
Lens Distortion

"Digitizing" the pixel information - CHIP



Lens Distortion

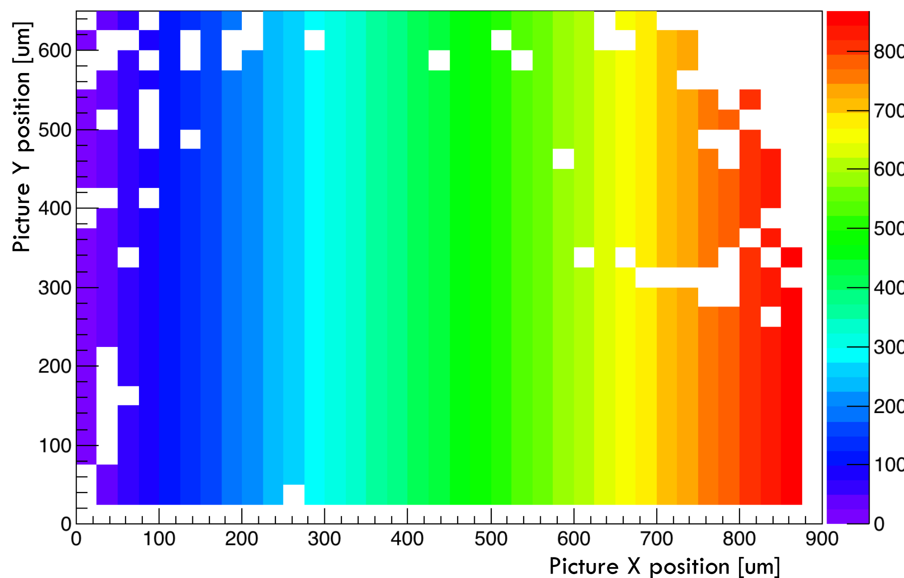
"Digitizing" the pixel information - SUB

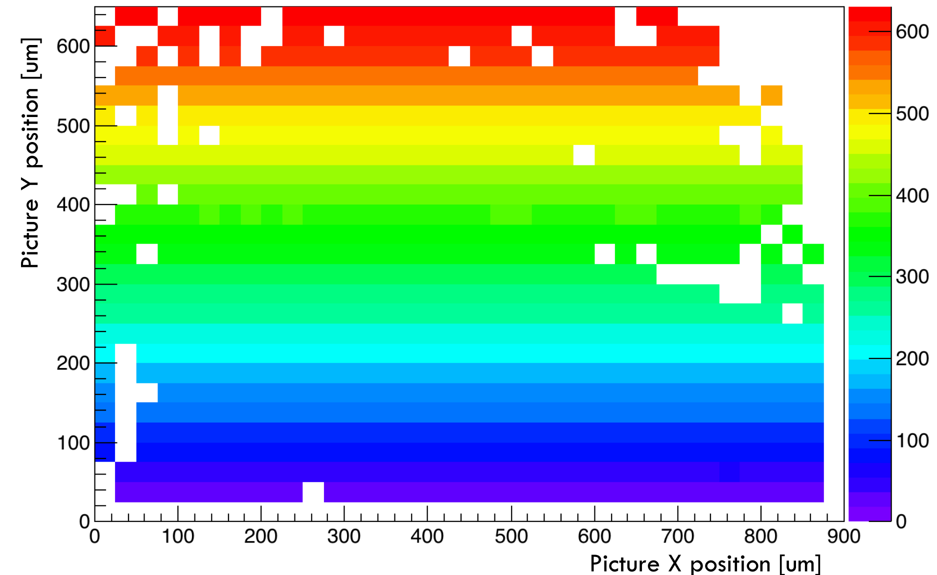


Lens Distortion

"Digitizing" the pixel information - CHIP

- Storing the pixel X and Y position in a histogram
  - Much easier to handle than a vector!

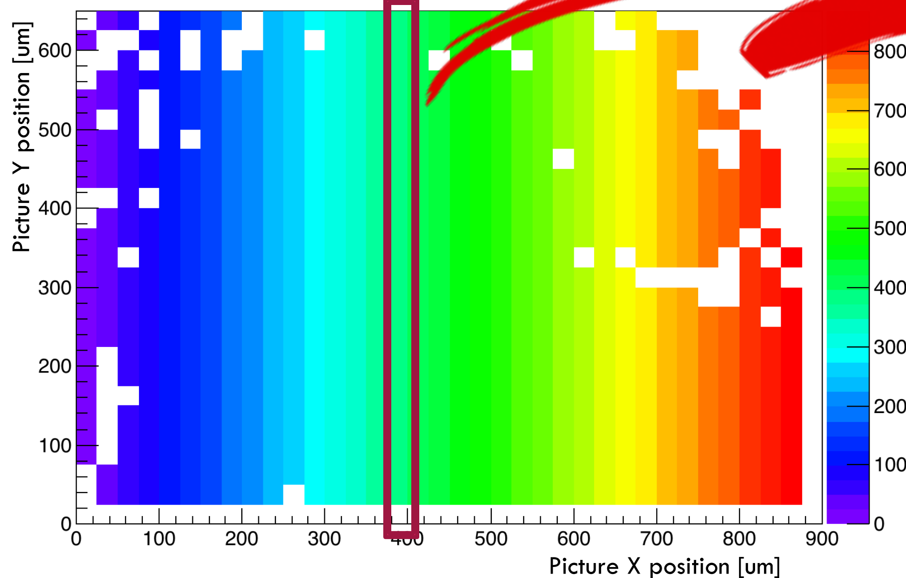


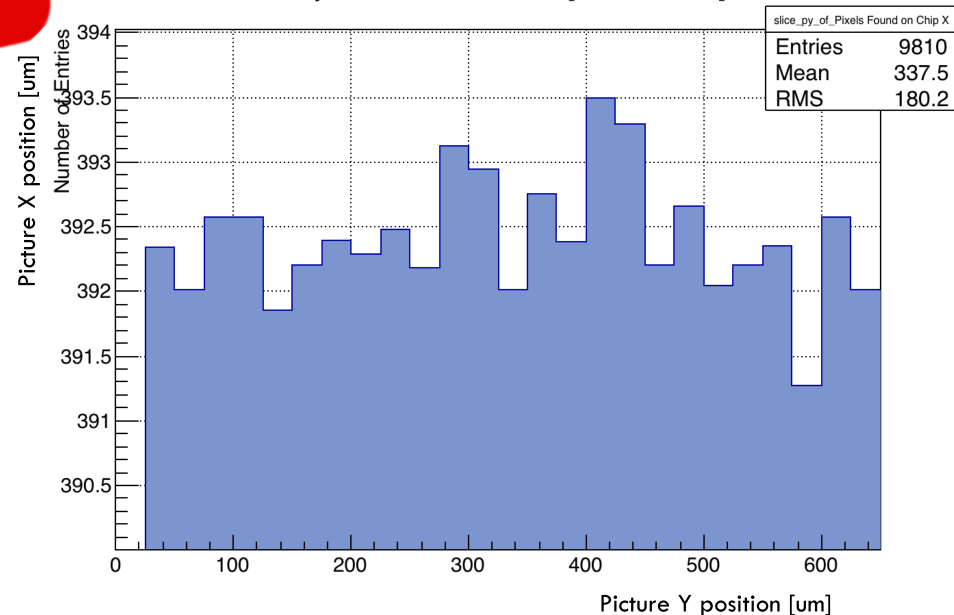


Lens Distortion

"Digitizing" the pixel information - CHIP

- Storing the pixel X and Y position in a histogram
  - Much easier to handle than a vector!



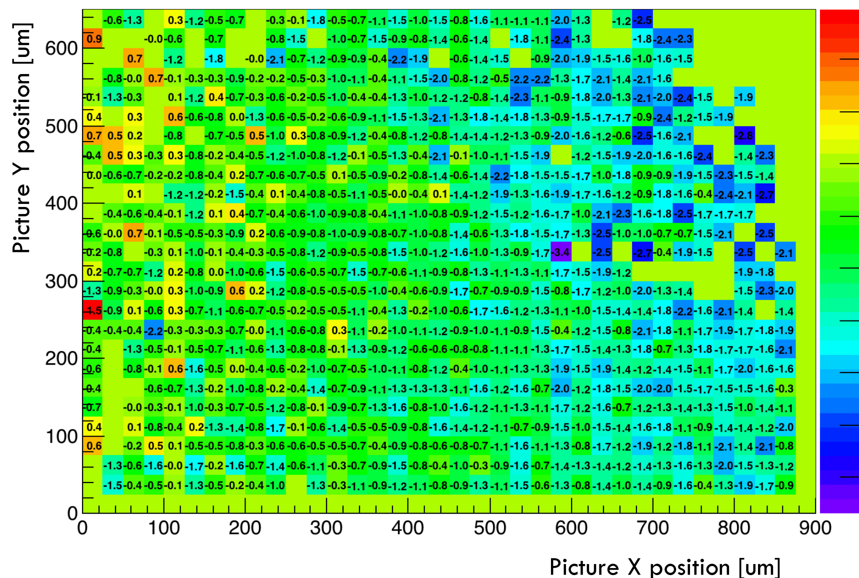


Lens Distortion

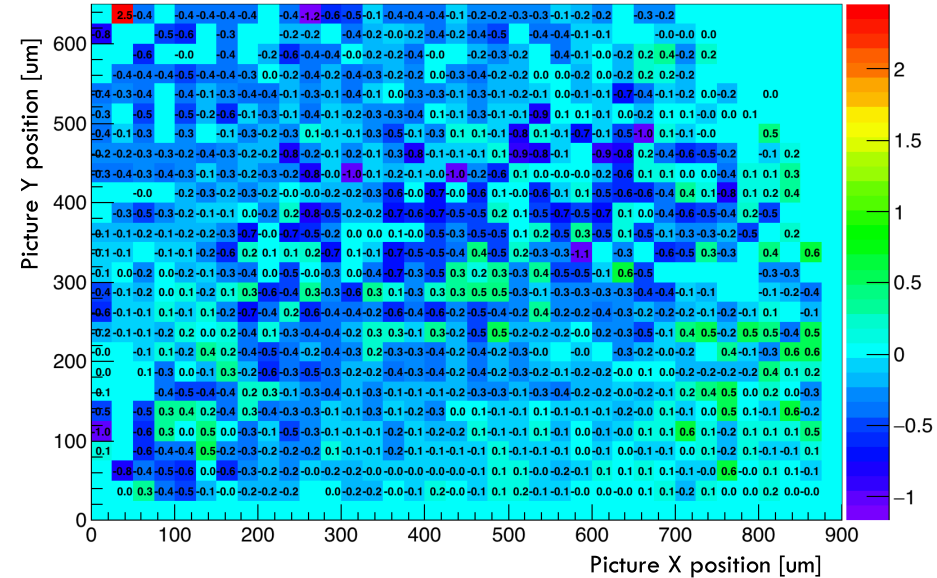
”Digitizing” the pixel information - CHIP

- Storing the pixel X and Y position in a histogram
  - **Offset = Pixel X,Y position – bin_address_position*25um**

Pixel X Offset [um]



Pixel Y Offset [um]

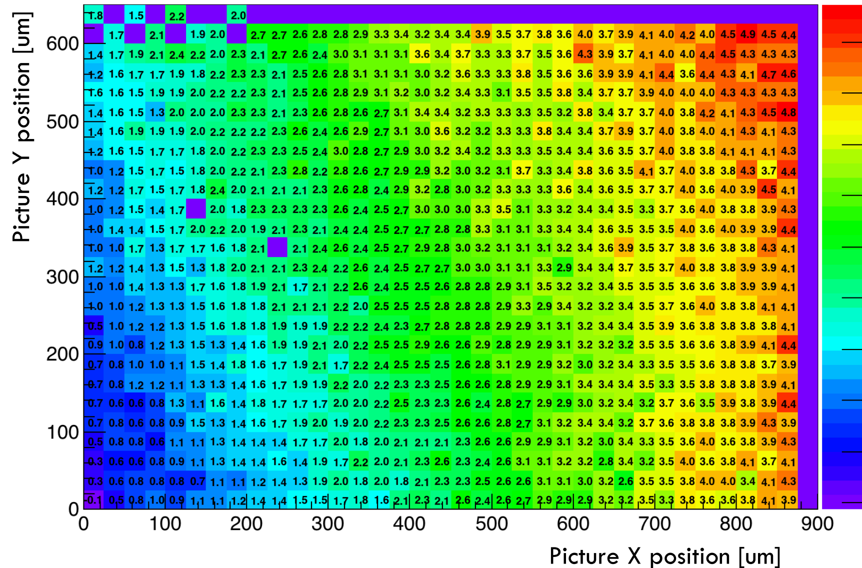


Lens Distortion

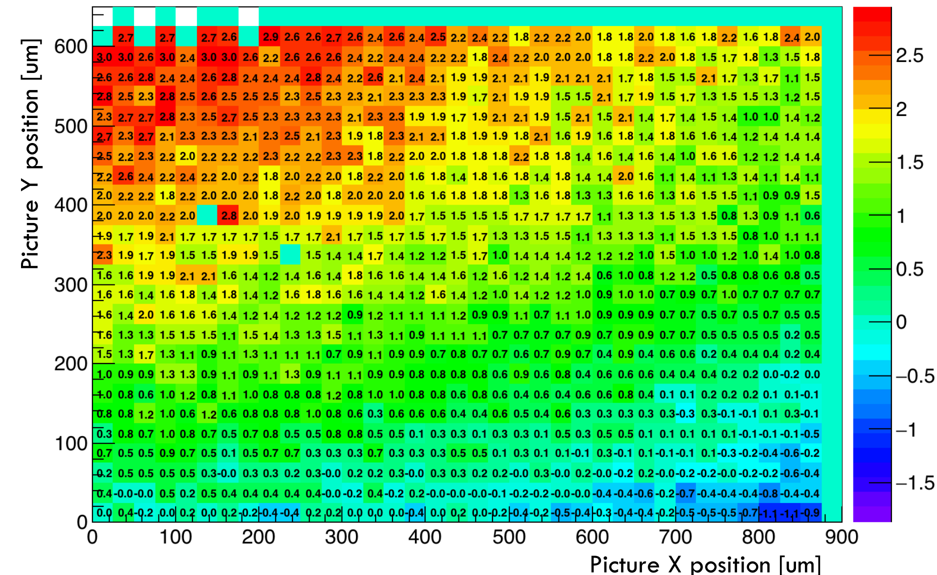
"Digitizing" the pixel information - SUB

- Storing the pixel X and Y position in a histogram
  - **Offset = Pixel X,Y position – bin_address_position*25um**

Pixel X Offset [um]



Pixel Y Offset [um]



Pixel pads overlap

Z scan

- A = 0.1 um
- B = 10 um