The CSOI approach for integrated micro channels

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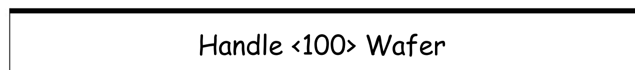
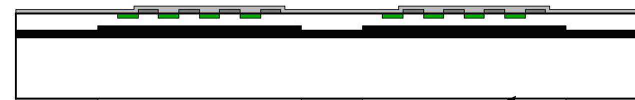
Processing thin detectors - the SOI approach

a) oxidation and back side implant of top wafer

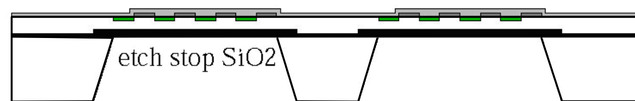


b) wafer bonding and grinding/polishing of top wafer

c) process → passivation



open backside passivation



d) anisotropic deep etching opens "windows" in handle wafer

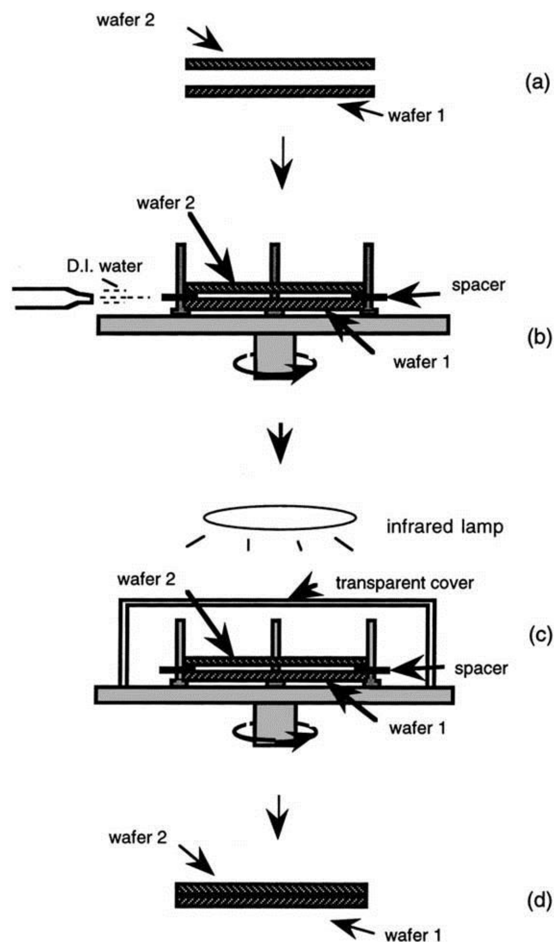
The sensor thickness becomes a free parameter, adjustable to the needs of the experiment!

Key Process Modules:

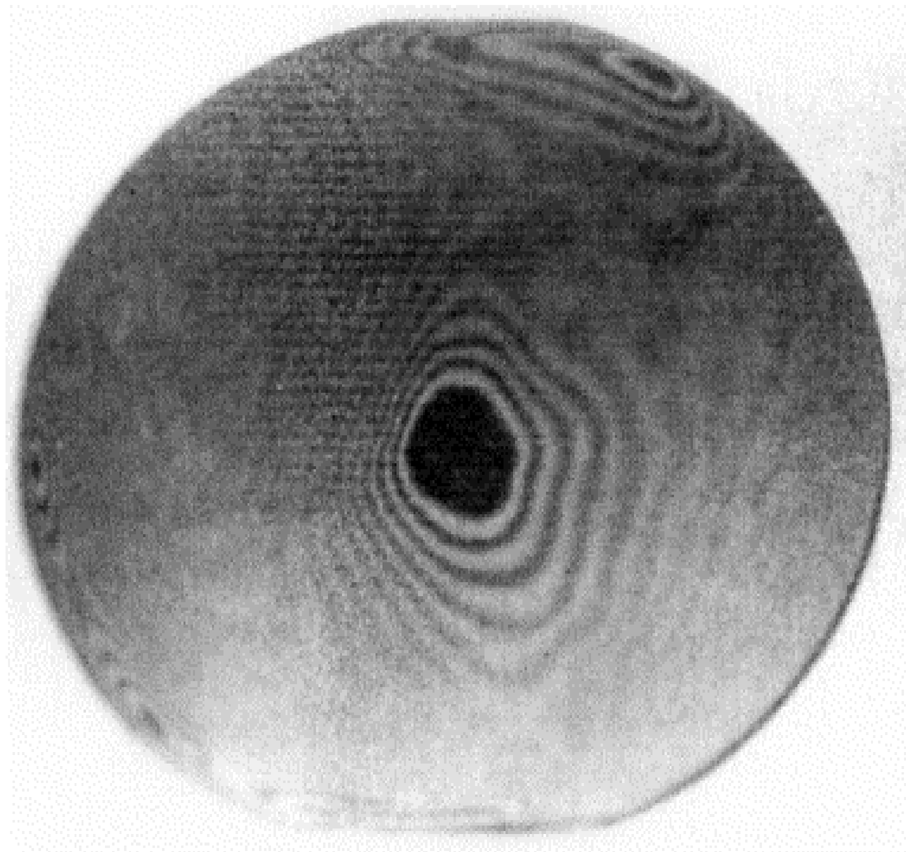
:- Wafer Bonding and thinning of top layer (external)
:- Sensor fabrication on SOI
:- Etching of the Handle Wafer

→ DEPFET for Belle II PXD (75μm)
→ Direct electron detectors (30 and 50 μm)
→ SiPMs - SiMPL (down to ~14 μm)
→ ATLAS ITk (150 and 100μm)

Direct Wafer Bonding in "Micro-Cleanroom"

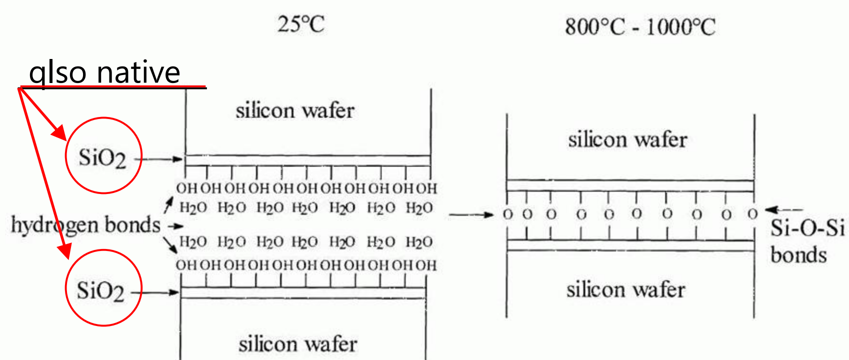


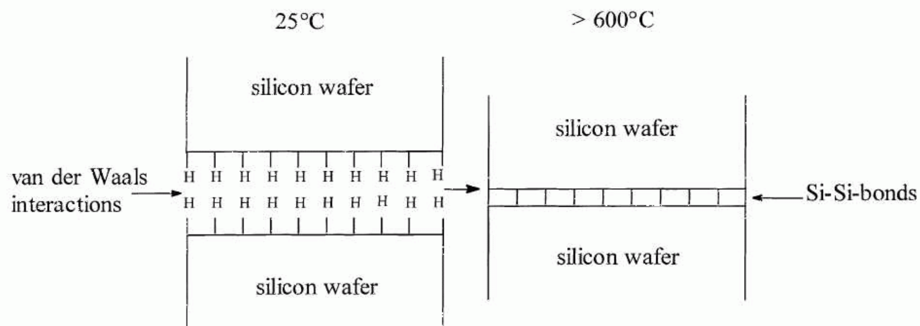
Q.-Y. Tong and U. Gösele " Semiconductor Wafer Bonding "
John Wiley & Sons, Inc.

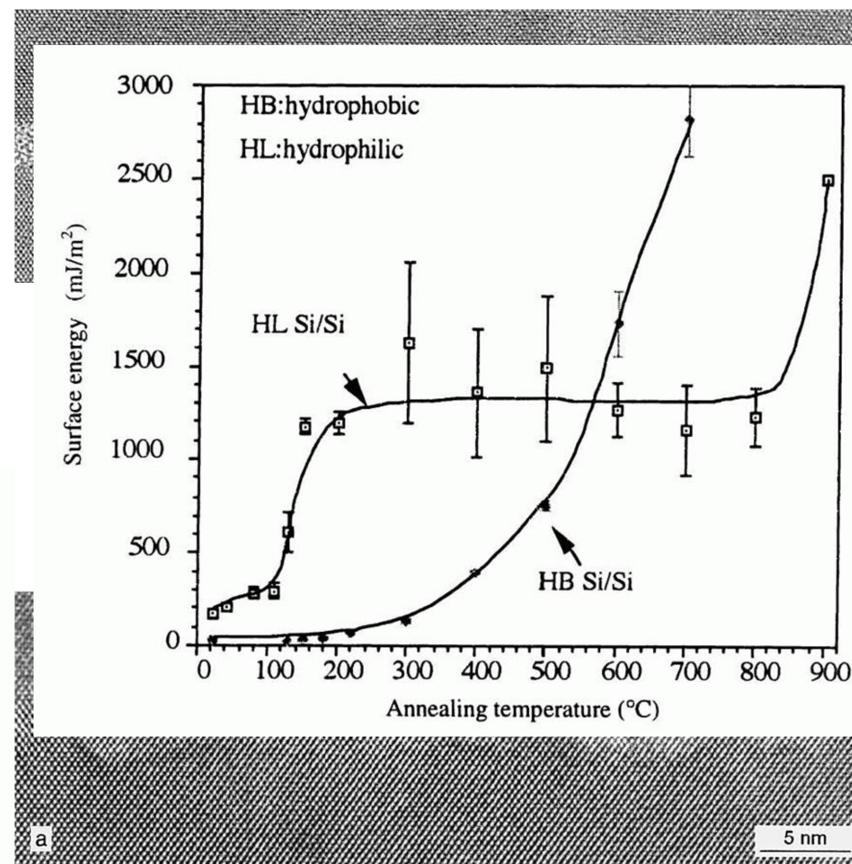


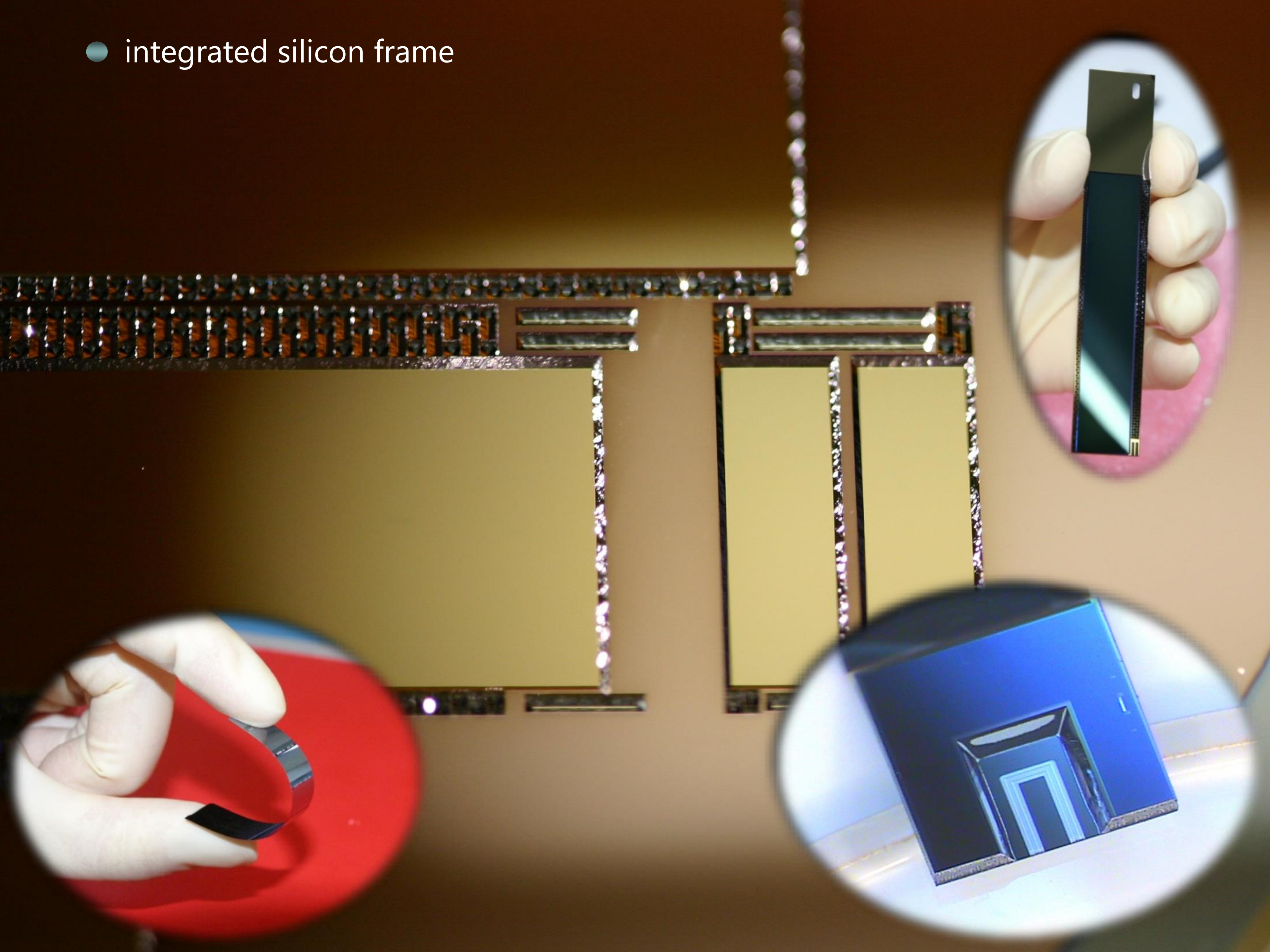
picture from: www.mpi-halle.mpg.de

Direct Wafer Bonding

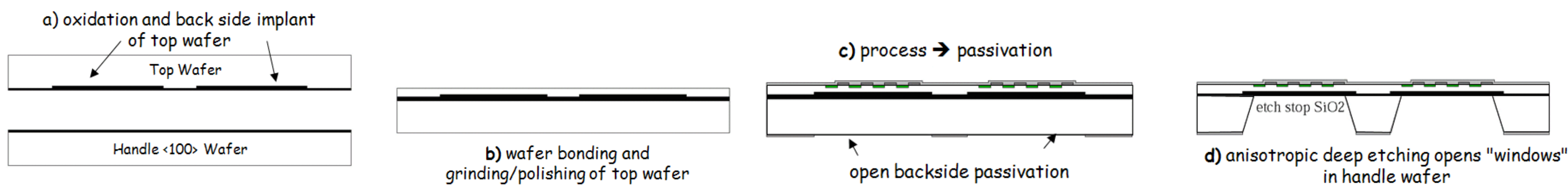


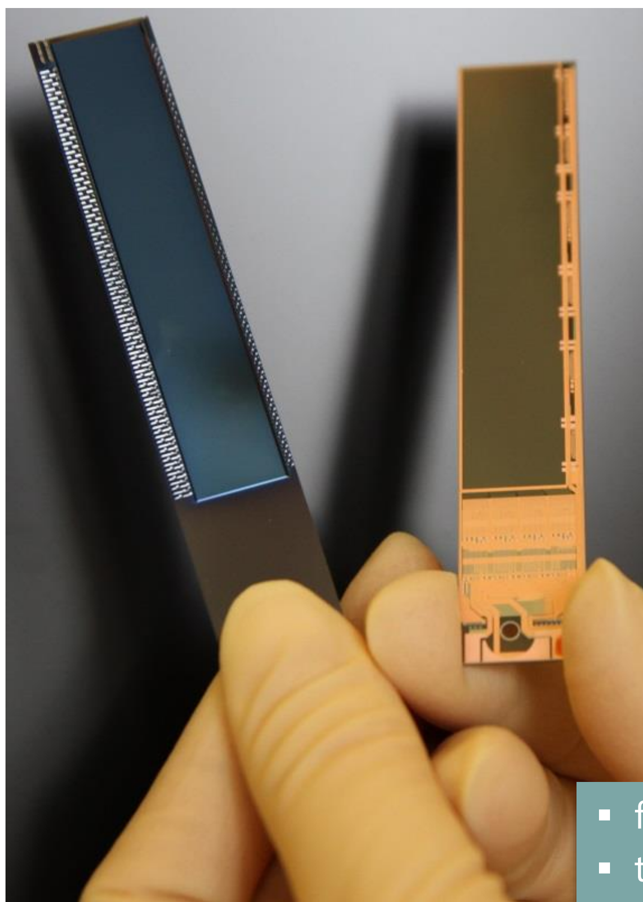


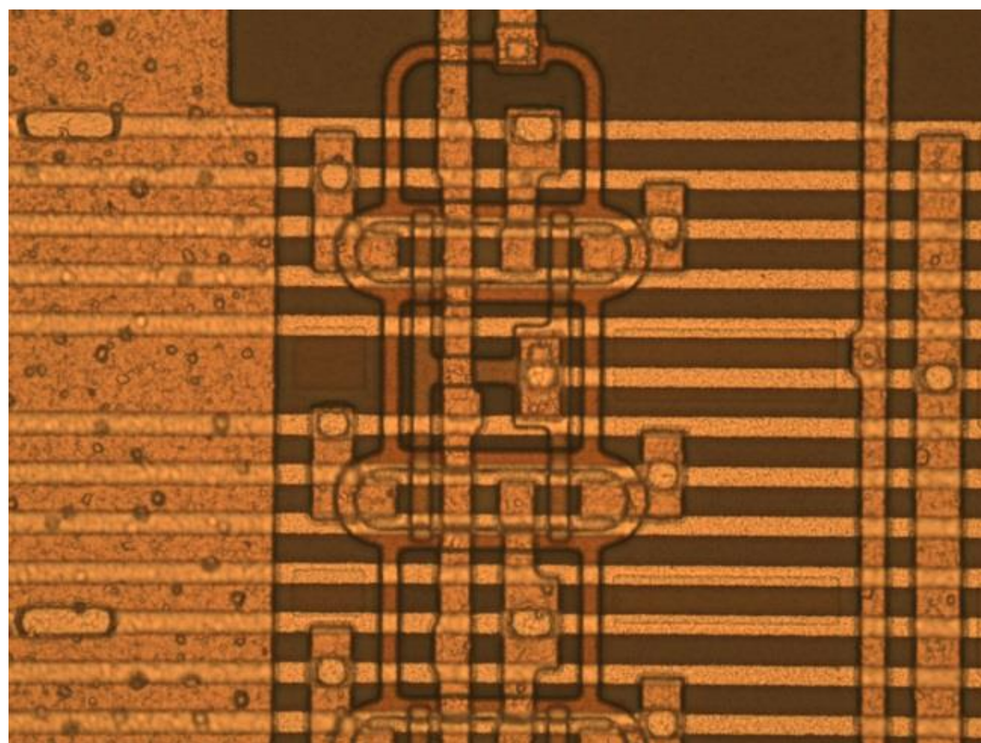



integrated silicon frame

thin DEPFETs

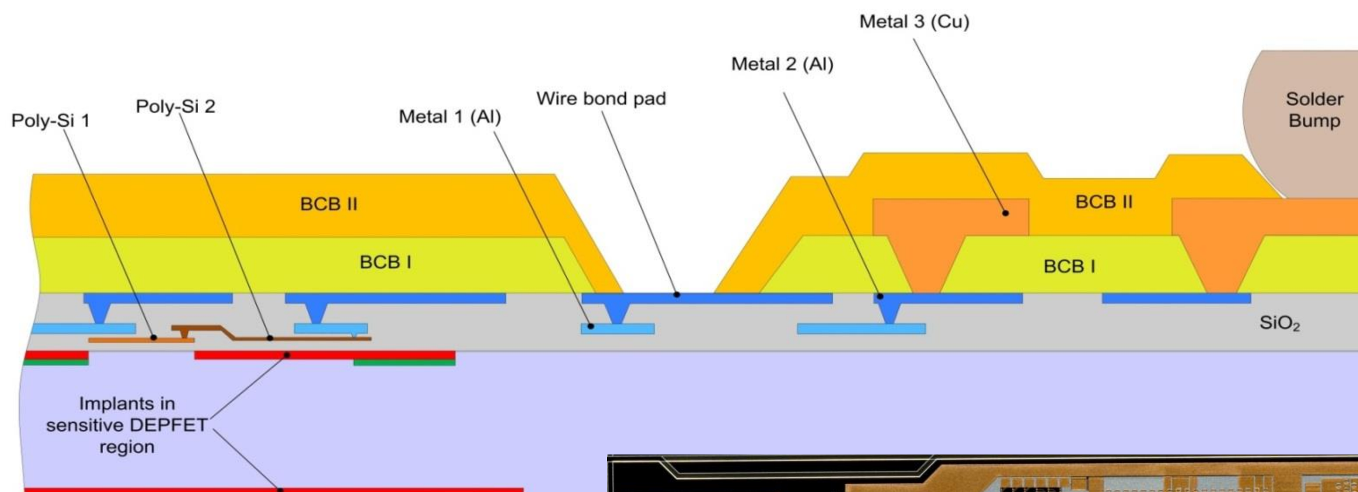


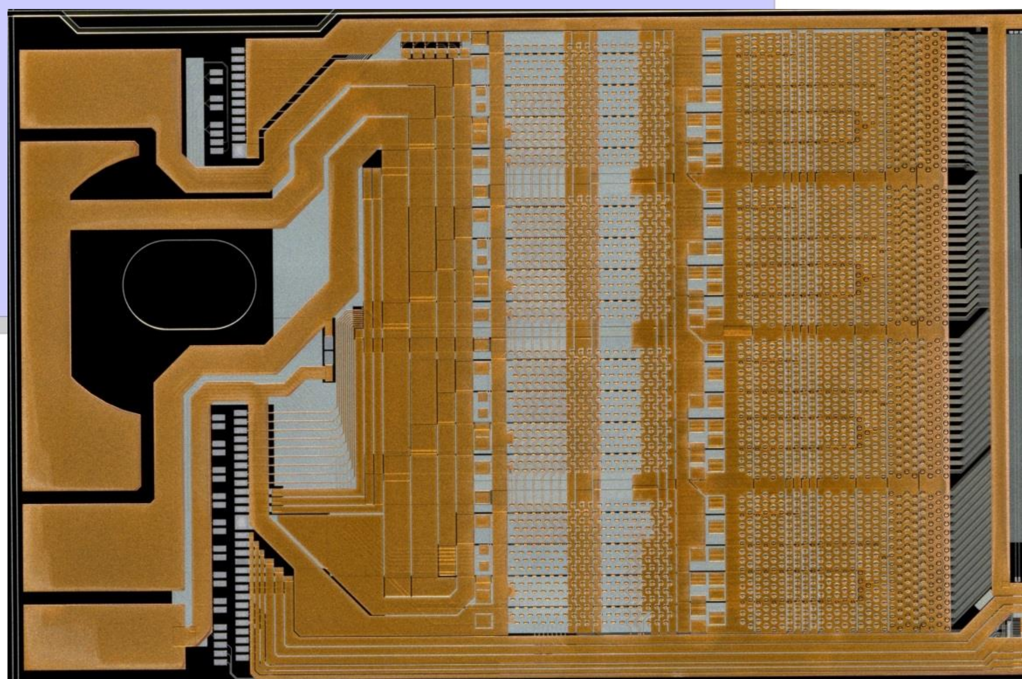




- full DEPFET technology in thin area
- thin area supported by a monolithically integrated silicon frame

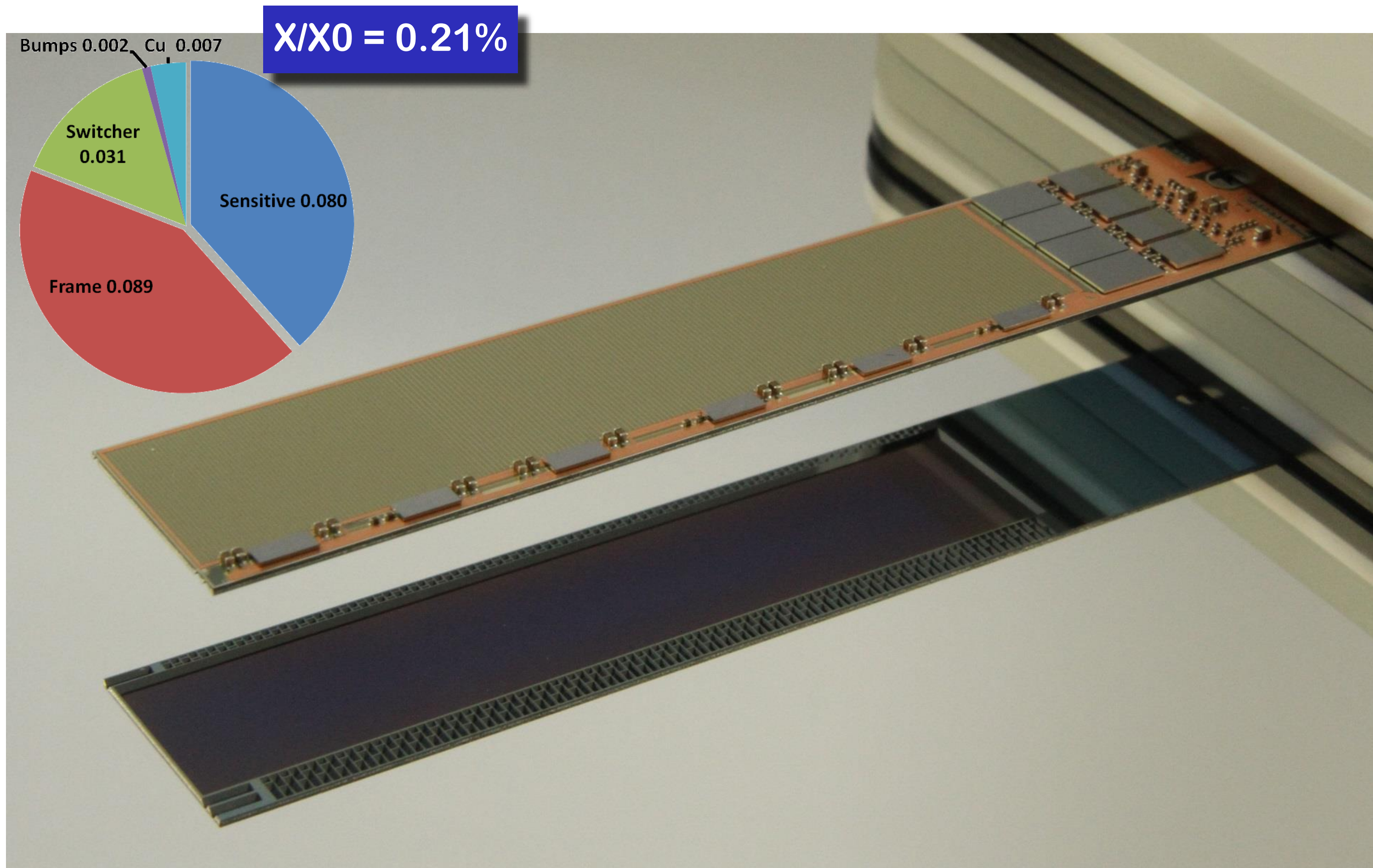
introducing a Cu layer on the DEPFET module



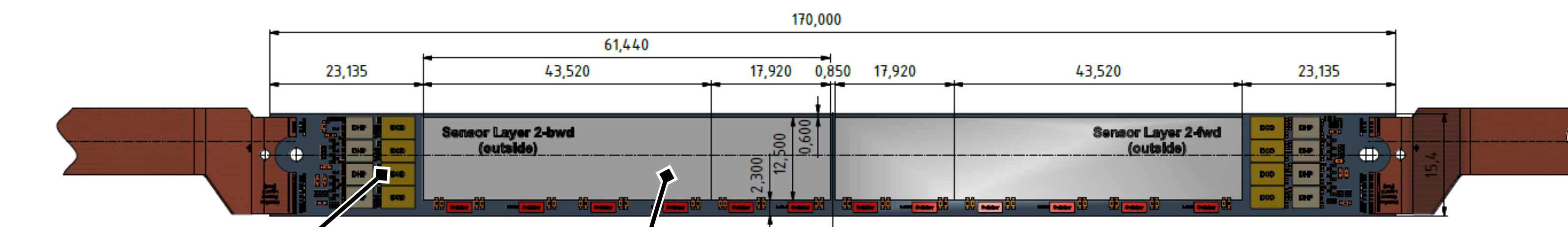


- three metal layer system in periphery
  - ↳ Copper as third metal
  - ↳ low-k dielectric to Alu2
  - ↳ UBM for flip chip
  - ↳ landing pads for passives
  - ↳ Solder connection to kapton

Belle II Module 0

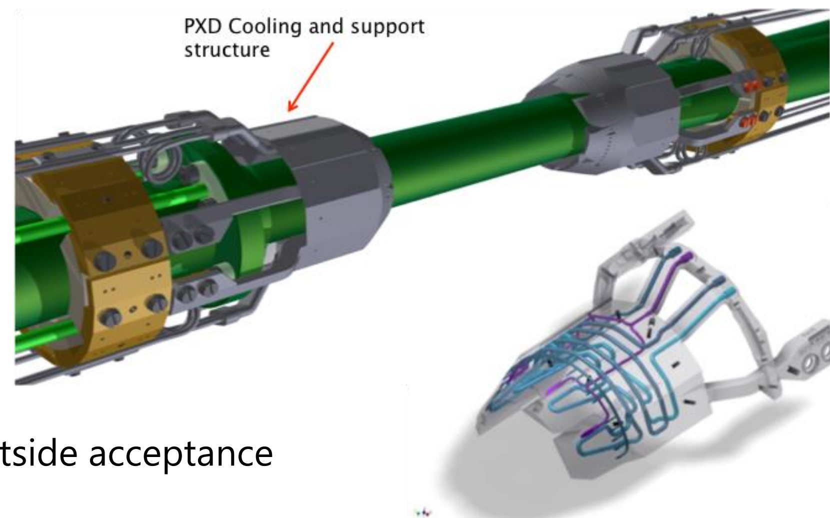


Thermal management and material



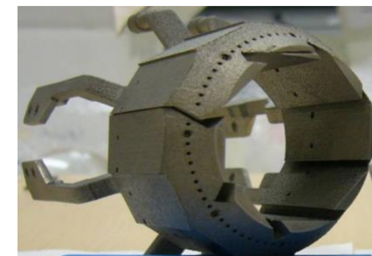
8W DCD&DHP

1W sensor & SWB → gas cooling

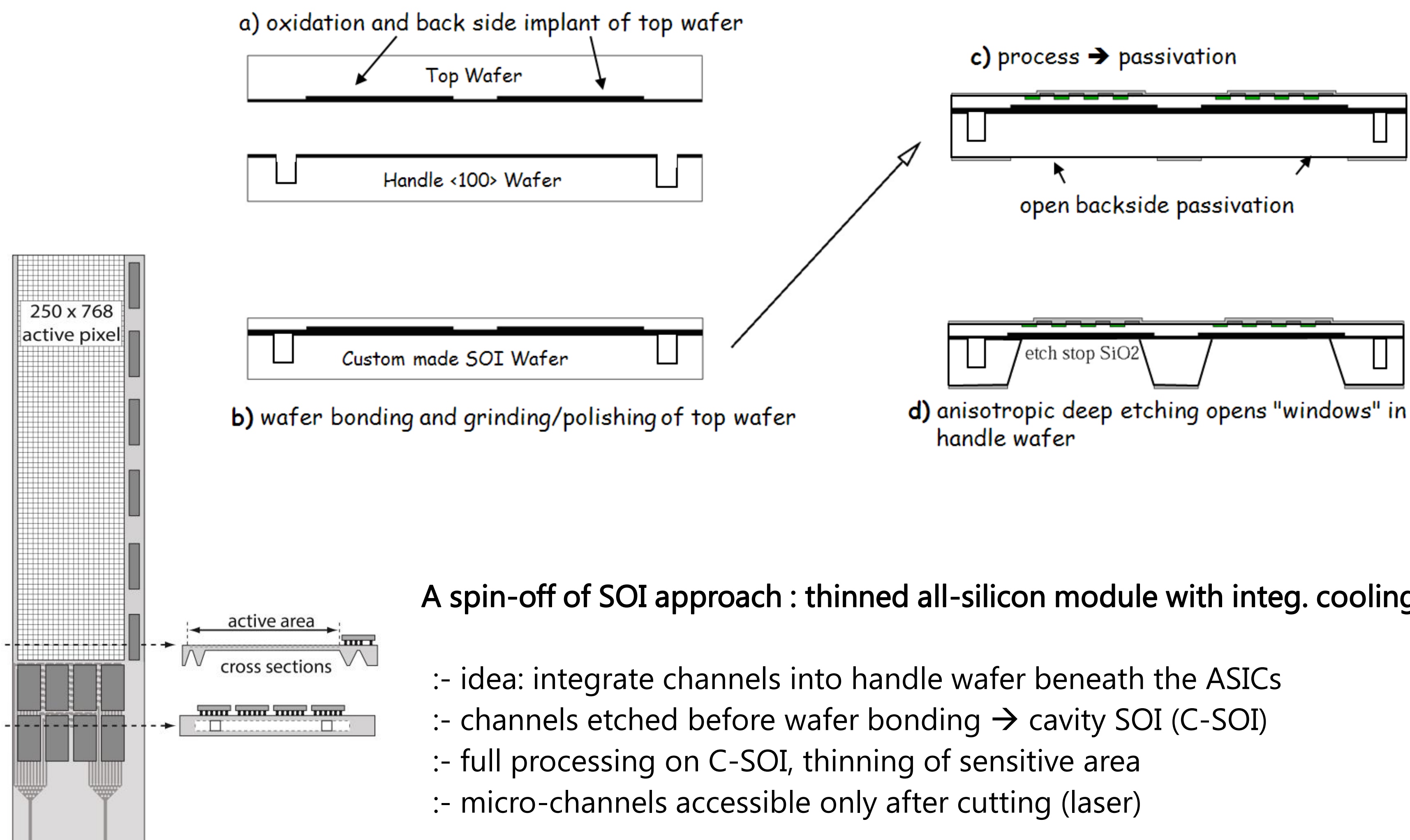


- Belle II
  - 9W/half ladder, 8W at EOS
  - Active (CO_2) cooling at EOS, cooling block outside acceptance
- difficult for experiments with larger acceptance region
- at EOS still high power density, active cooling would be good

→ How about silicon integrated cooling channels there ????



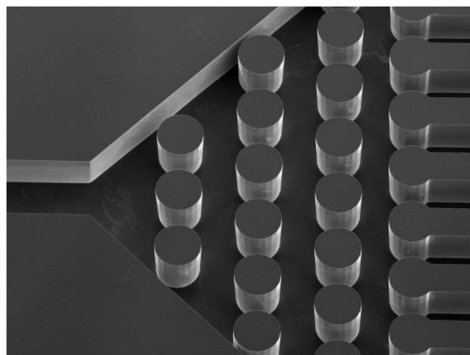
Integrated micro-channels



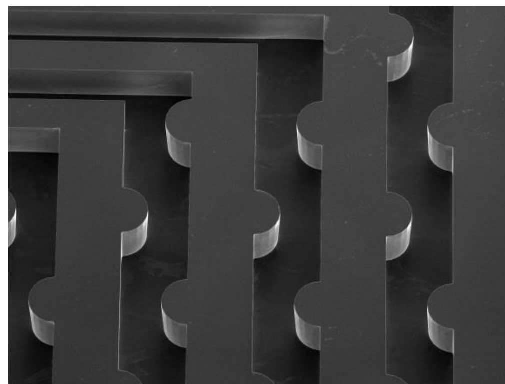
A spin-off of SOI approach : thinned all-silicon module with integ. cooling

:- idea: integrate channels into handle wafer beneath the ASICs
:- channels etched before wafer bonding → cavity SOI (C-SOI)
:- full processing on C-SOI, thinning of sensitive area
:- micro-channels accessible only after cutting (laser)

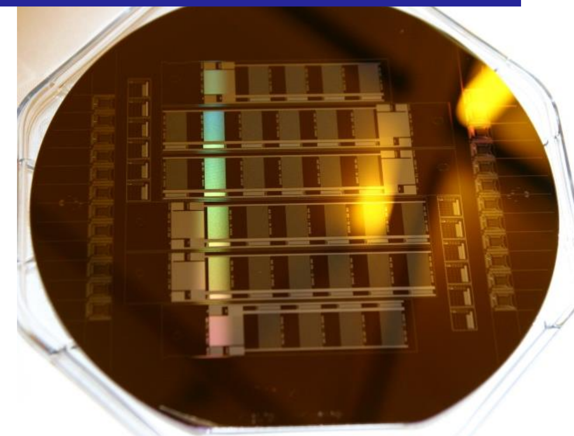
Prototypes with resistive heating and micro channels



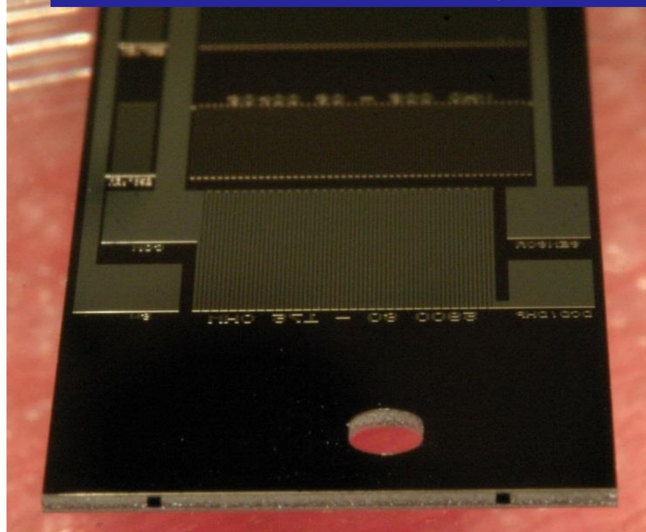
DRIE etching of handle wafer



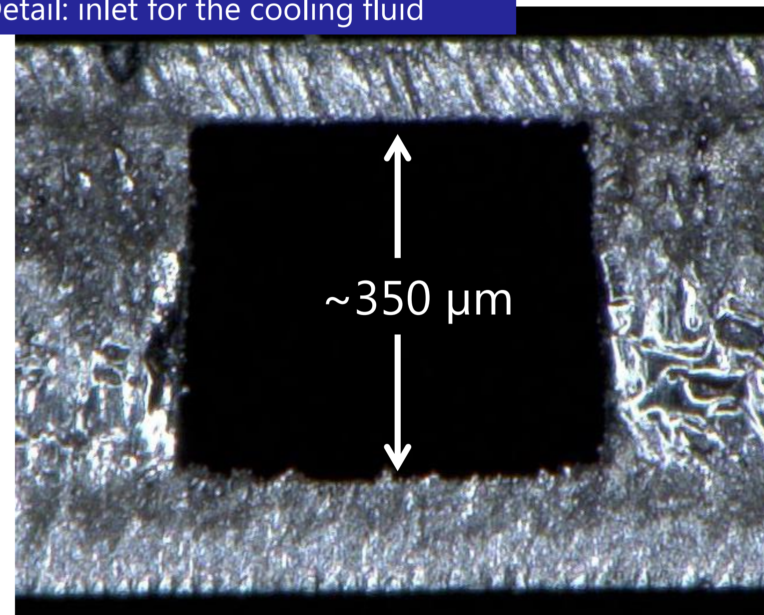
CSOI wafer with integrated ressistors



Module after cutting

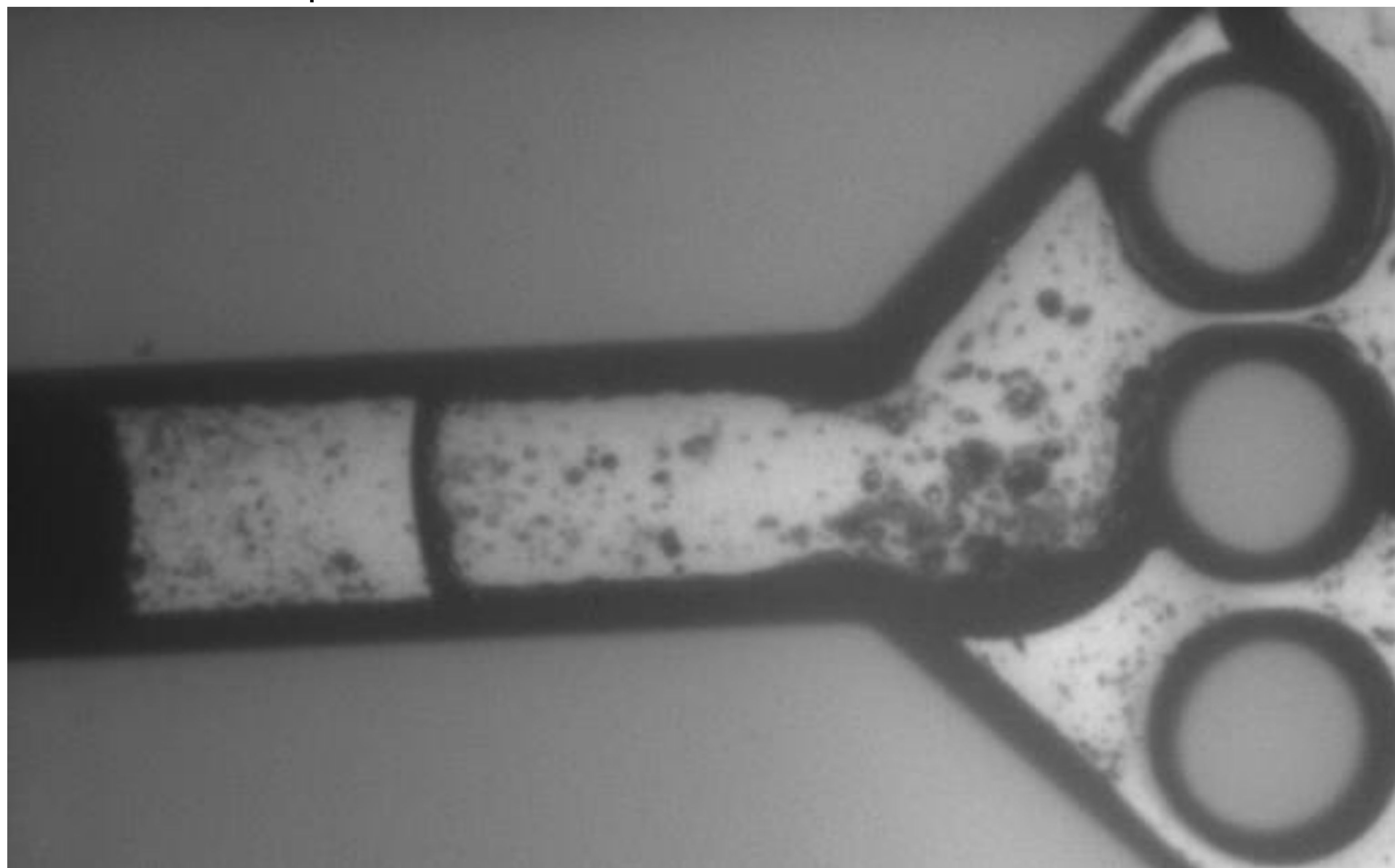


Detail: inlet for the cooling fluid

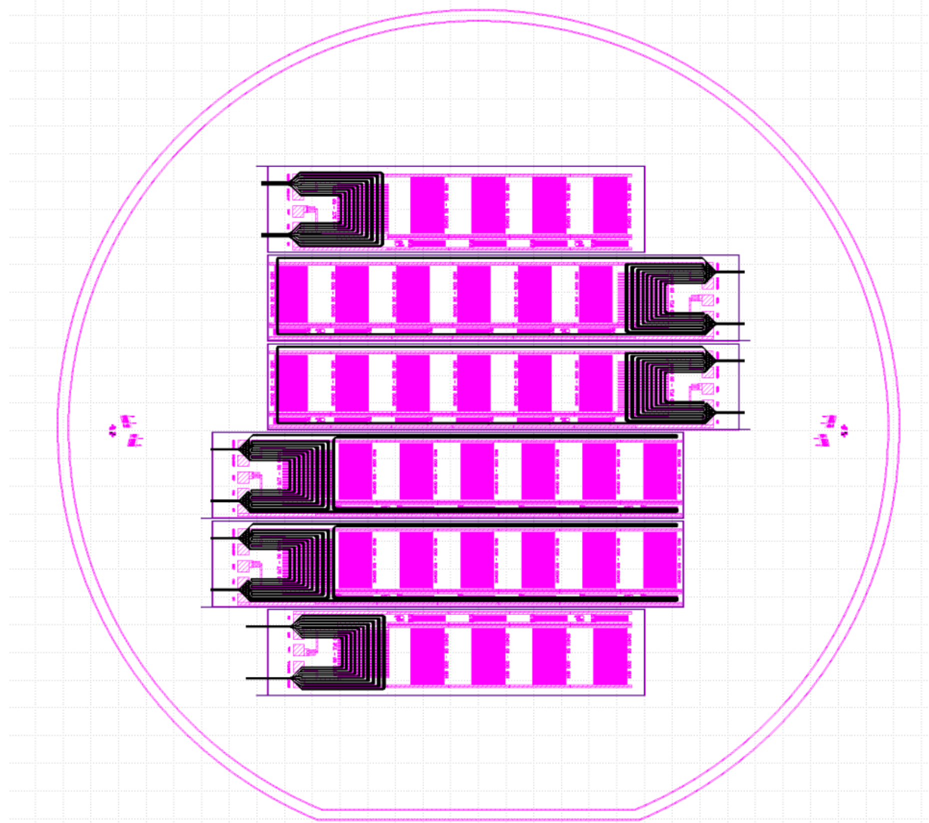


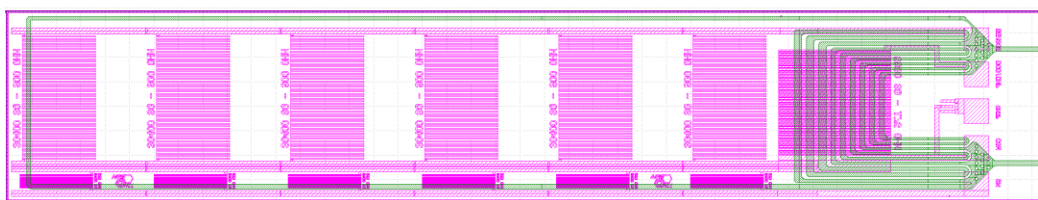
IR movie – just for entertainment

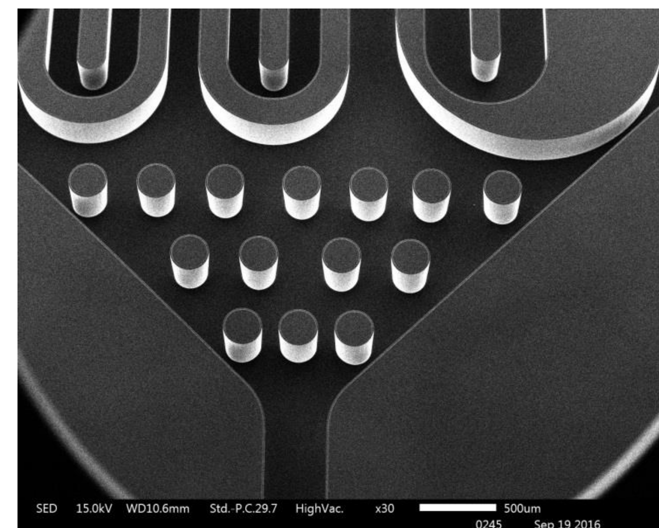
:- silicon particles in water
:- low flow 300µl/s

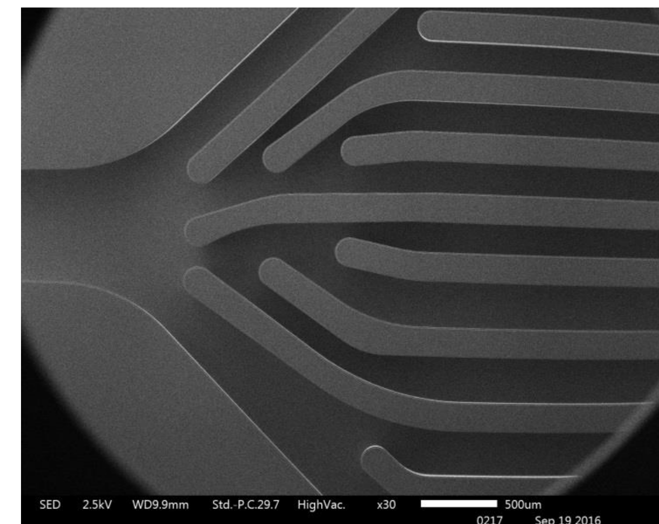


2nd round

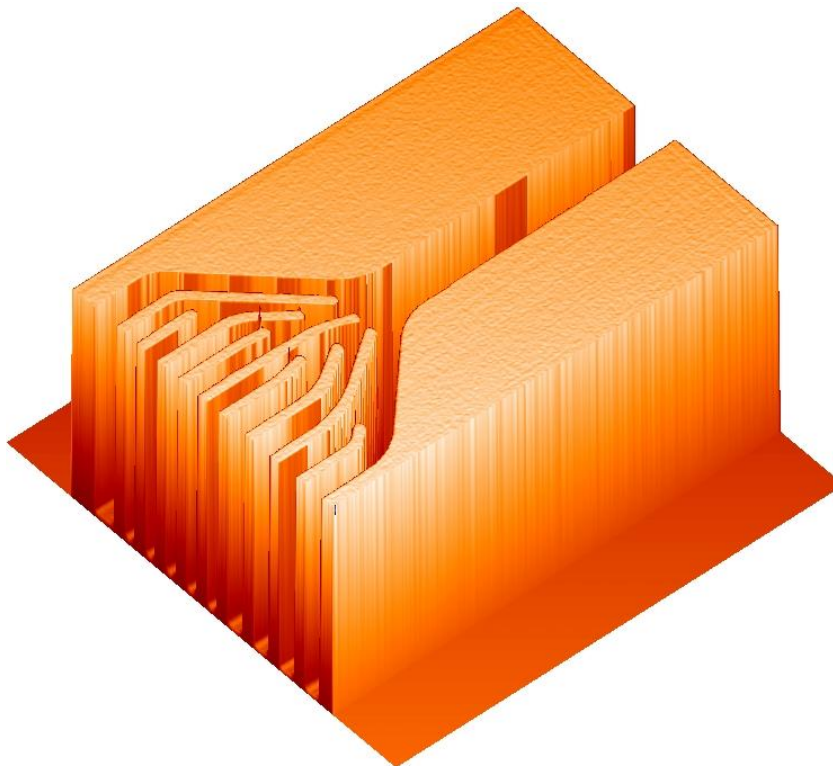


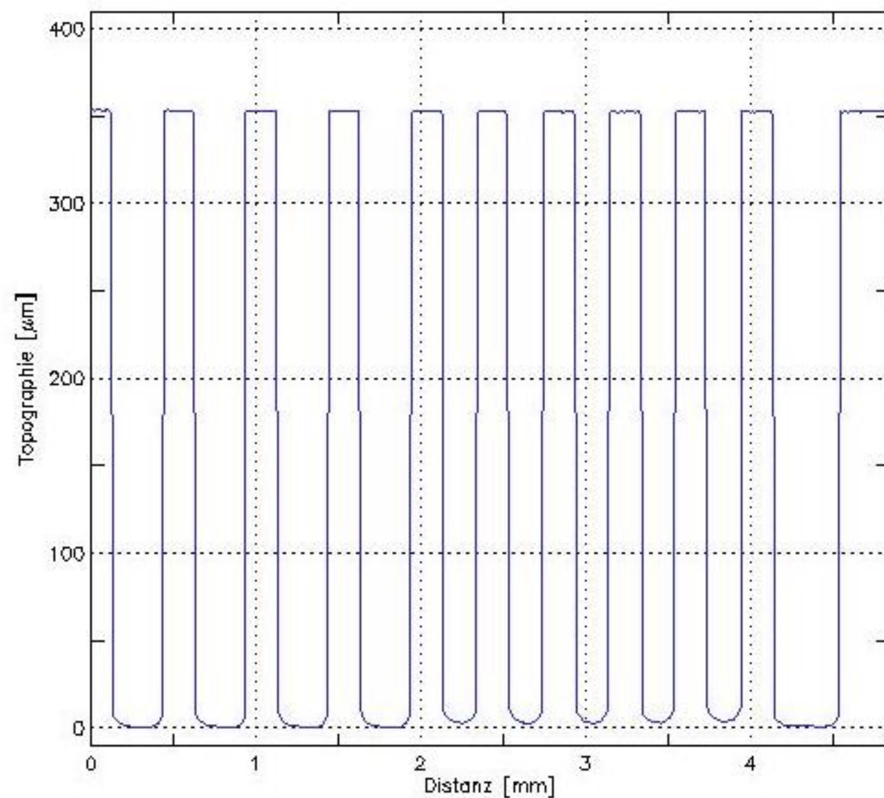






2nd round: Profiles before wafer bonding





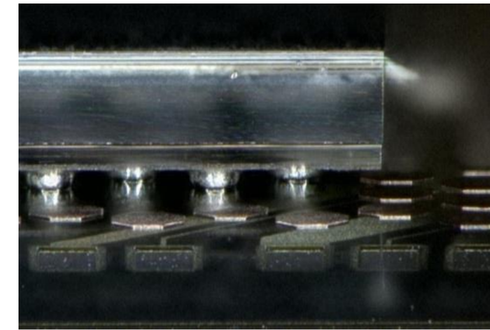
Summary

- Active pixel sensors for Belle II are already fabricated on SOI wafers
  - ↳ Convection cooling in thin sensitive region, "aggressive" CO2 at the end-of-stave (EOS)
- Natural next step is the introduction of integrated cooling channels at the EOS
  - ↳ Cavity SOI
- Feasibility studies done, look promising
- Concept can be extended to any kind of sensors on SOI, in particular hybrid pixel sensors as in ATLAS/CMS
  - ↳ Would of course require re-design of the module ..

Module Assembly – overview

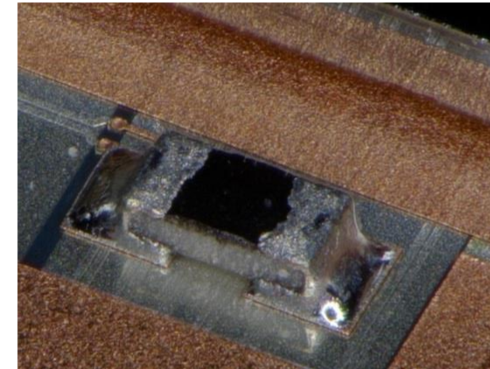
Flip Chip of ASICs (~240°C):

- ▷ Bumped ASICs have the same solder balls (SAC305)
  - ↳ DHP bumping at TSMC, DCD bumping via Europractice
  - ↳ So far SWB bumping on chip level
- ▷ Flip Chip of PXD modules on custom made support plates



SMD placement (~200°C):

- ▷ Passive components (termination resistors, decoupling caps)
- ▷ Dispense solder paste/jetting of solder balls, pick, place and reflow
  - ↳ PbSn 37/63 solder



Kapton attachment (~170°C), wire bonding:

- ▷ Solder paste printing on kapton,
  - ↳ SnBi solder
- ▷ Wire-bond, wedge-wedge, 32 μm Al bond wires