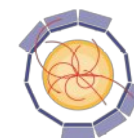
Activities in Task 14.3.1
Test infrastructure for innovative calorimeters with semiconductor readout

Vincent Boudry

École polytechnique, Palaiseau

AIDA-2020 2nd Annual Meeting
04–07/04/2017, Paris

TNA support + WP14

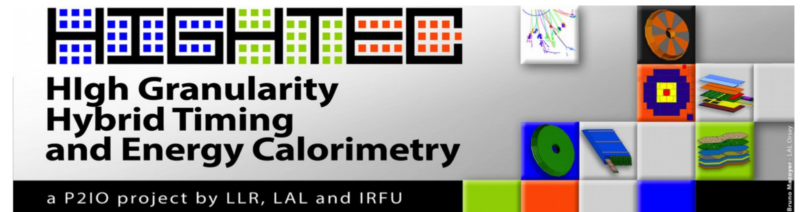


AIDA 2020

Recent news on SiW-ECAL

Funding from Paris-Saclay P2IO “physics of 2 Infinities and Origins” Gran t⟶ LLR, LAL & IRFU (CEA)

- HGCFC: High-Granularity Calorimeters for future Colliders started (oct. 2016). dubbed “**HiGHTEC**” in between
  - SiW-ECAL for LC’s
  - CMS-HGCAL ⊃ timing studies
  - ATLAS-HGTD design & studies



Coord. Y. Sirois

- Complementary of AIDA-2020:
  - Completion of SiW-ECAL prototype; Study of long slab; Mechanical studies
  - DAQ for ILD
- 2 post-docs recruited for 2 years:
  - **Adrian Irles (WP5)** (since 7/11/16) @ LAL on SiW-ECAL : DAQ & tests
  - **Artur Lobanov** (≥1/12) @ LLR on SiW-ECAL (25%) & CMS-HGCAL(75%): SK2(a) test & analysis

Plans for 2017 in a nutshell…

Test completely the 10 SLAB's produced in 2016

- June 2016 tests: mitigated results
  - SiW-ECAL suffered from noise (of still unknown origin)
    - ⇒ « SLAB's not tested in beam »
  - DAQ development (SiW-ECAL+ SDHCAL) ✔
    - Shown to work; To be completed with working prototype
- Standalone tests in June @ DESY
  - Improvement of DQM & DAQ (Adrian @ LAL)
  - Improvement of Power Supplies (LAL & LLR)
    - Some behaviour linked to number of SLABs in operation
  - Review of the procedure to optimise the noise & retriggering handling in the chips
    - Thorough check of rates vs conditions:
      - » slower clock (less edges)

~~Combined tests with SDHCAL → Fall~~

End March: Decision **not** to go in 2017: *manpower issues*

- after June validation
  - test in IPNL of both set-ups
- news mechanical structure
  - Flexible number of layers, for $24X_0$ W

Production of additional layers with SK2A & 525µm wafers

- Tests of SK2A (many improved features): **on-going**
- Test of wafers HPK wafers : **received. To be tested @ LPNHE**
- new PCB FEV12 ordered (to be received this week)
- Assembly bench adaptation @ LLR ⊗ LPNHE ⊗ LAL
  - thicker wafers for shorts slabs
  - **Long SLAB preparation**
  - Test of gluing with thin PCB's

Preparation of June 2017 BT @ DESY

	Week		TB21		TB22		TB24/1		TB24
				DATURA		DURANTA	PCMAG	Telescope in PCMAG	none
2-Jan-17	1		Shutdown						
9-Jan-17	2								
16-Jan-17	3								
23-Jan-17	4								
30-Jan-17	5								
6-Feb-17	6		Startup		Startup		Startup		Startup
13-Feb-17	7		Goe-ATLAS-3D-Dia	X	LHCb-SCiFi		BELLE-II		
20-Feb-17	8		AIDA2020WP5	X	LHCb-SCiFi				
27-Feb-17	9		ATLAS-X0	X	ATLAS-X0	X			
6-Mar-17	10		CMS-Pixel-Phase 1	X	ALICE-ITS				
13-Mar-17	11		CMS-Pixel-Phase 1	X	ATLAS ITk Pixel	X			
20-Mar-17	12		TBMST	X	ATLAS ITk Pixel	X			
27-Mar-17	13				ATLAS ITk Pixel	X			
3-Apr-17	14								
10-Apr-17	15		CMS-Tracker-PSP	X	CMS-Tracker-2S	X			
17-Apr-17	16		CMS-Tracker-PSP	X	CMS-Tracker-2S	X			
24-Apr-17	17		ATLAS-Strip-Pitch	X	ATLAS-Strip-Glue	X			
1-May-17	18								
8-May-17	19								
15-May-17	20				Setup				
22-May-17	21				ATLAS-ITk-Strips	X			
29-May-17	22				ATLAS-ITk-Strips	X			
5-Jun-17	23								
12-Jun-17	24		CMS-Tracker-PSP	X			CALICE-SiW-ECAL		
19-Jun-17	25		CMS-Tracker-PSP	X			CALICE-SiW-ECAL		
26-Jun-17	26		CMS-Pixel-Phase-2	X					
3-Jul-17	27		CMS-Pixel-Phase-2	X	Mu3e	X			
10-Jul-17	28		Summer Shutdown						
17-Jul-17	29								
24-Jul-17	30								
31-Jul-17	31								

DESY Testbeam Schedule 2017 - Version 9- 28/02/2017

Ralf Diener, Norbert Meyners, Marcel Stanitzki - DESY Test Beam Coordinators

Announced

June 12–24th in DESY, TB24/1 (PCMag line)

- Test 10 SLABs, with SK2 (same as June 2016)
- Possibility to have B filed test of electronics (secondary goal)
  - 120-130kg. Usable ∅ ~ 75cm

Test set-up:

- Remounted at LAL for implem of DQ (Adrian Irles)
- DAQ updates (Pyrame v3, ⊃ improved online rec).
- Power Distribution to be rebuild.

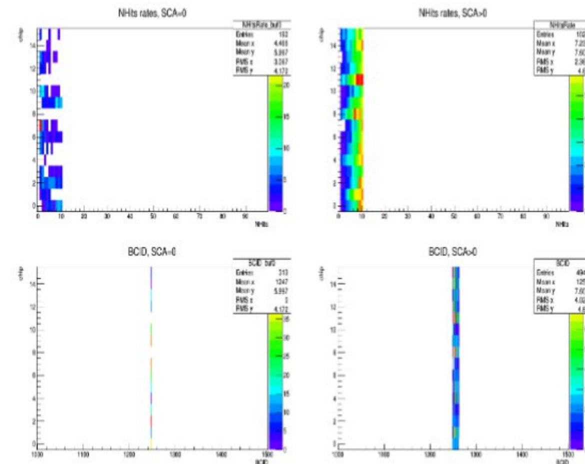
Testbench(es) 2017

- DAQ + Power Supplies rack from LLR
  - Plug & Play
- Prototype equiped with **5 FEV10 modules** with 16 chips **(skiroc 2)**, 64 chn each = 5120 chn.
  - 5 more at LLR to be integrated in the prototype for beam test.

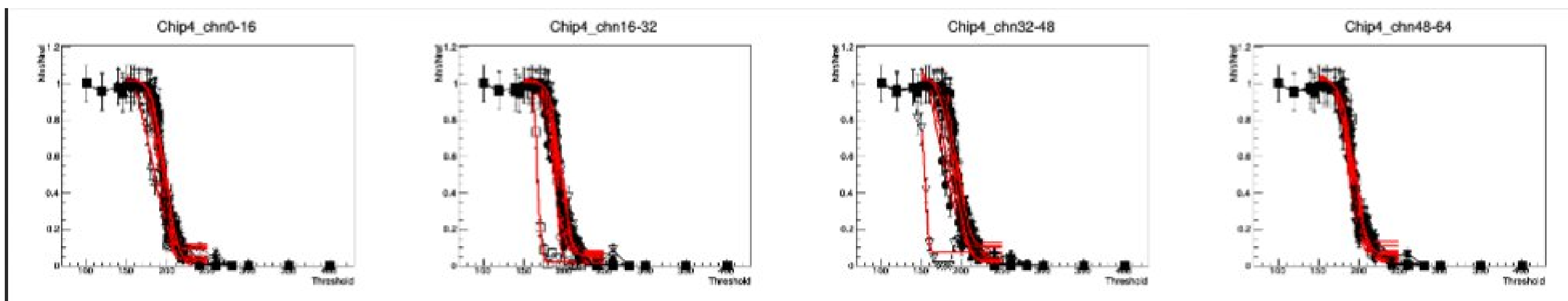
LABORATOIRE DE L'ACCÉLÉRATEUR LINÉAIRE

Irles, A. | CALICE Meeting | 22st Mars 2017 | Page 3

- Data taken at LAL with the prototype.
  - Noise run, with low fast shaper threshold value (DAC = 190)
  - FEV10, SK2.
  - HV = on (110V)
- Plots for one ASIC
  - Nhits (SCA=0 and SCA>0)
  - BCID (SCA=0 and SCA>0). As the threshold is quite low, the BCIDs are ~ val_evt BCID.

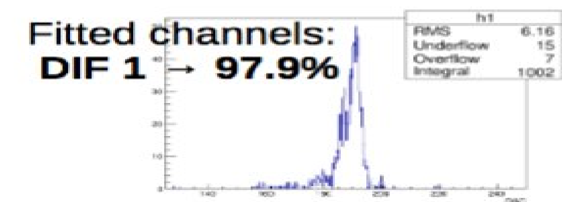


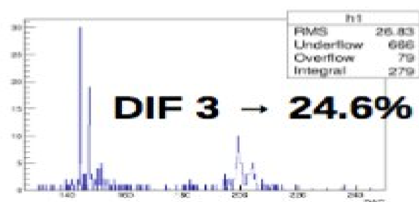
Threshold scans...

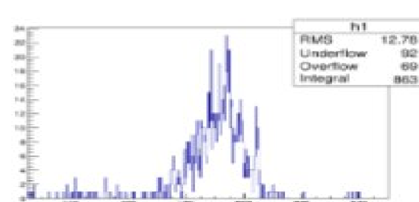


- Summary plots of optimal threshold fit for all DIFs

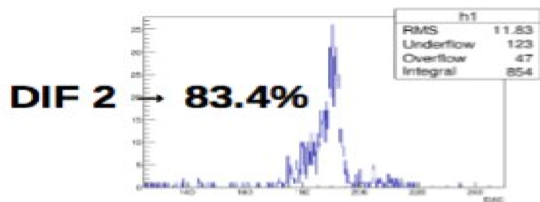
Fitted channels:

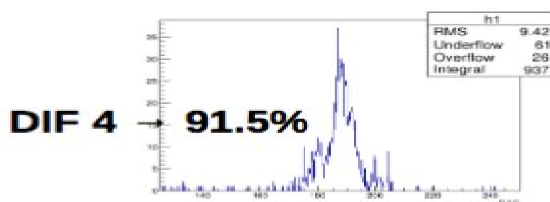






DIF5 → 84.3%





- Not optimized analysis or results checked carefully but ... **promising**.

Test of SK2 and SK2a (LLR)

Test bench at LLR:

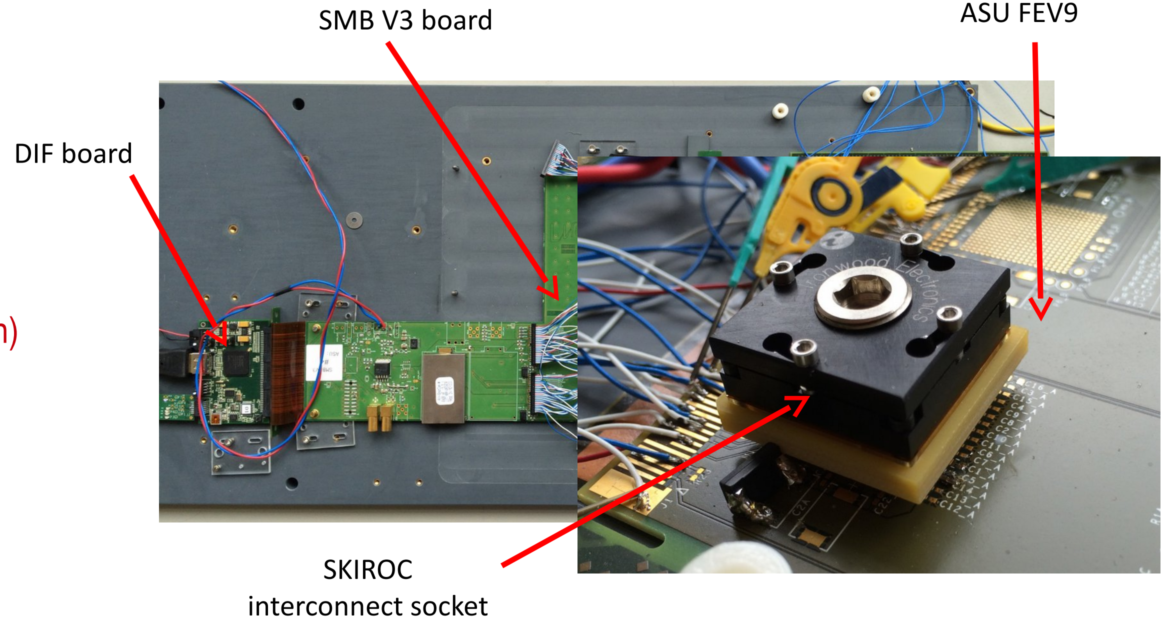
- FEV9 with single BGA socket
- ASIC in power pulsing (PP)
  - CCC, LDA, DIF, SMB v3
  - FastCLK: 50 MHz, Slow CLK: 2.5MHz
- DAQ software: Pyrame/Calicoes v2-3 (development branch)
- Possibility of in phase signal injection

⊕

- Quick exchange of ASICs
- External command lines available on FEV connectors
- Single chip allows high spill frequencies (up to 60 Hz)

⊖

- Socket less reliable than soldering
- Lower quality SMB-FEV connections ⇒ More exposed to noise



⇒ Thorough check of running cond. with single chips
⇒ Procedure for SLABs

A. Lobanov, S. Chaitanya, V. Boudry, J. Nanni

ASIC testing: set-ups

From : Izumi Sekiya, LCWS2016

Tests of SK2A (outside of Ωmega):

- Dedicated test board (all protections on)
  - Kyushu #LabView (copy of Ωmega)
  - Ωmega ↔ LLR (CMS & CALICE)
    - Adaptation to PYRAME (Yannick Geerebaert)
      - S2A → SK2CMS

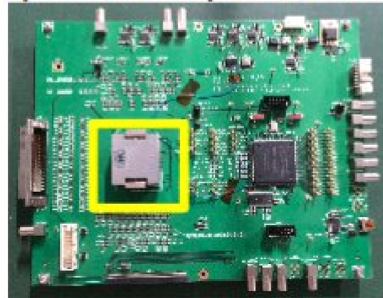
⊕

- ASIC soldered on board
- Decoupling capacitances on all critical power line
- External and internal signals available

⊖

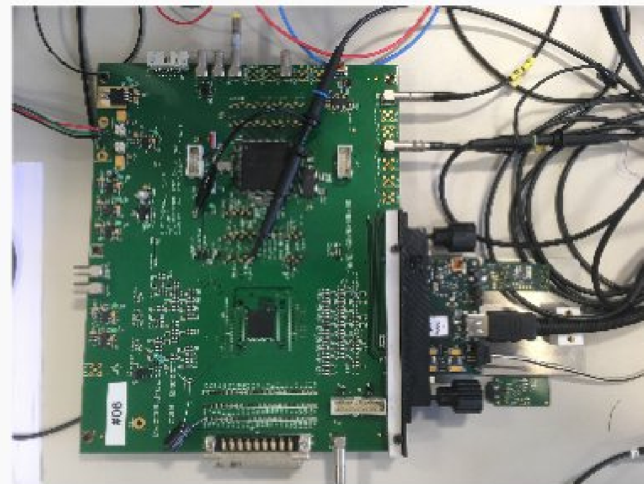
- No power pulsing possible
- ASIC not replaceable

Testboard1
-- Being equipped with a BGA socket
-- ASIC chip can be replaced easily



Testboard2
-- SKIROC2A is directly mounted on the board

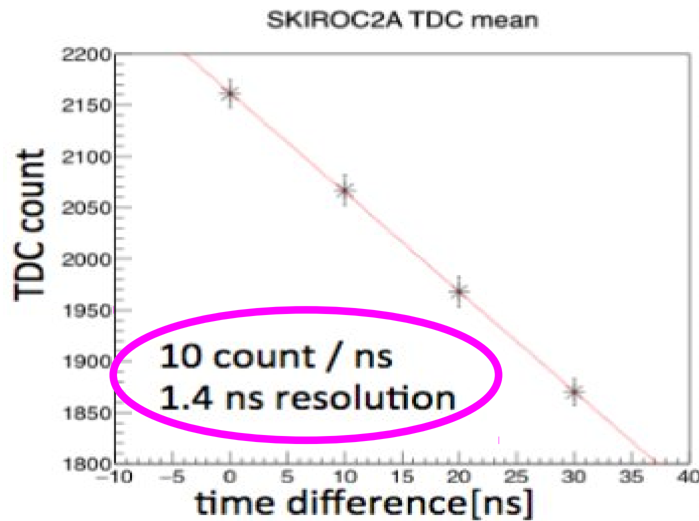
New Ω test board for SKIROC2A produced with DIF connector



SK2A first results

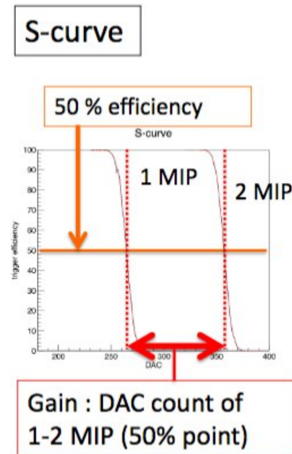
Thorough checks on 1 mip injected signal (Izumi Sekiya for Kyushu group)

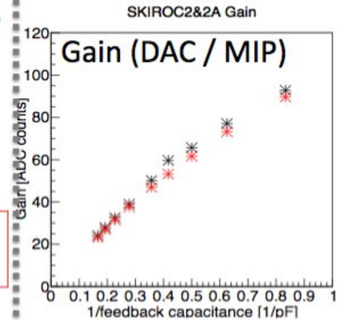
- All seems OK
- No difference in Analog part
- Trigger:
  - large channel-by-channel adjustment ✔
- TDC
  - Working!

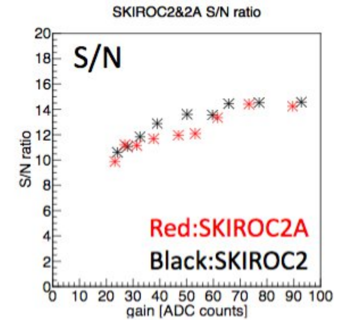


Fast shaper & triggering @SKIROC2,2A

- Test pulse in ch10
- Preamp of all ch active
- Trigger of all ch active
- Dependence on gain by feedback capacitance
- Socket version of testboard is used



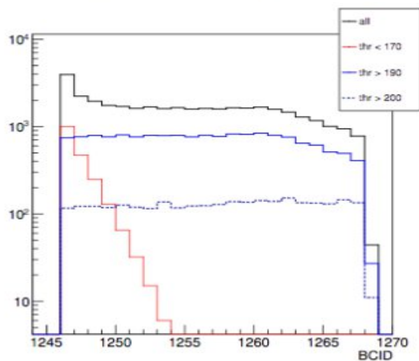


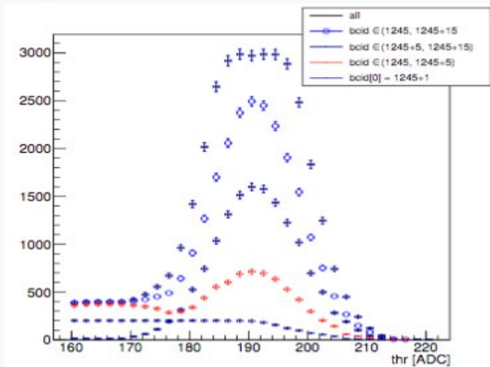


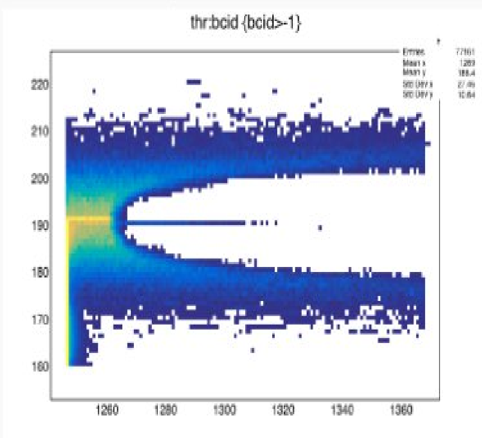
S/N=13~14, no difference seen between SKIROC2/A

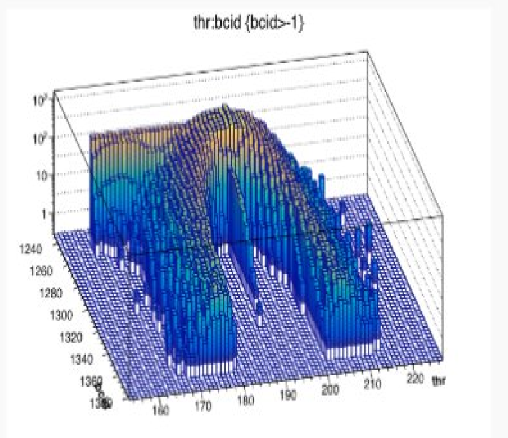
Noise on Trigger Channel
S-curves (single chan scan)

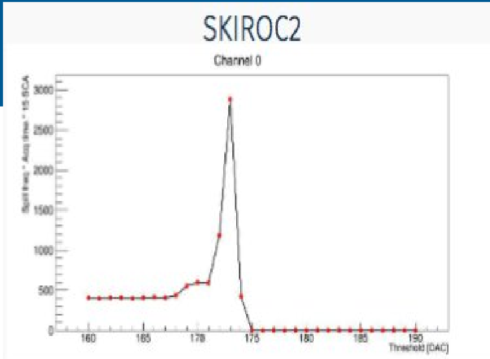
- Acqusition length: 10μs (spill length: 1.410ms)
- Sometimes “val_event” seems to trigger first few SCAs

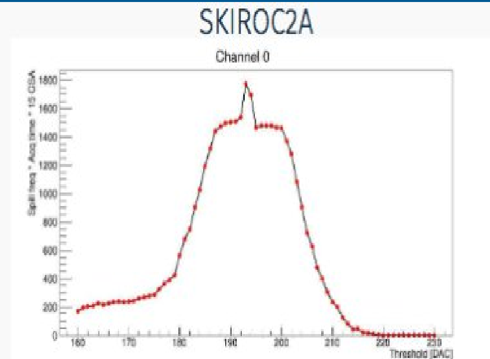




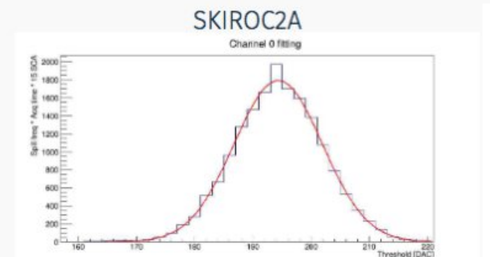


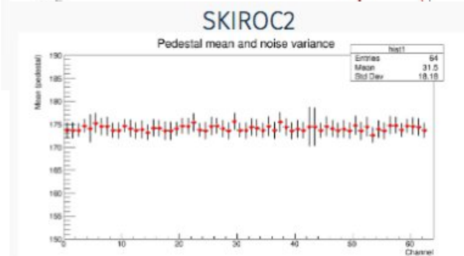


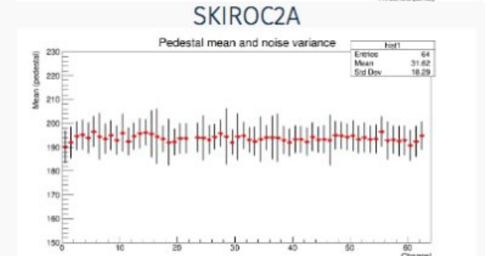




- SK2 has narrow peak (as expected), but SK2A has a wide distribution







Mean : 173.8 – 175; Variance : 0.8 – 1.3

Mean : 194 ± 1; Variance : 6 ± 0.4

- Low spread between channels in SK2 and SK2A

Planning 2017: Prototype

with 10 first[t] SLAB's

- noise handling
  - Scans.
  - Time dependance ?
  - PS dependance ?
- Cosmic data taking
  - ⚠ hasher running conditions… (longer integration time)

Beam test in 12–24 June @ DESY

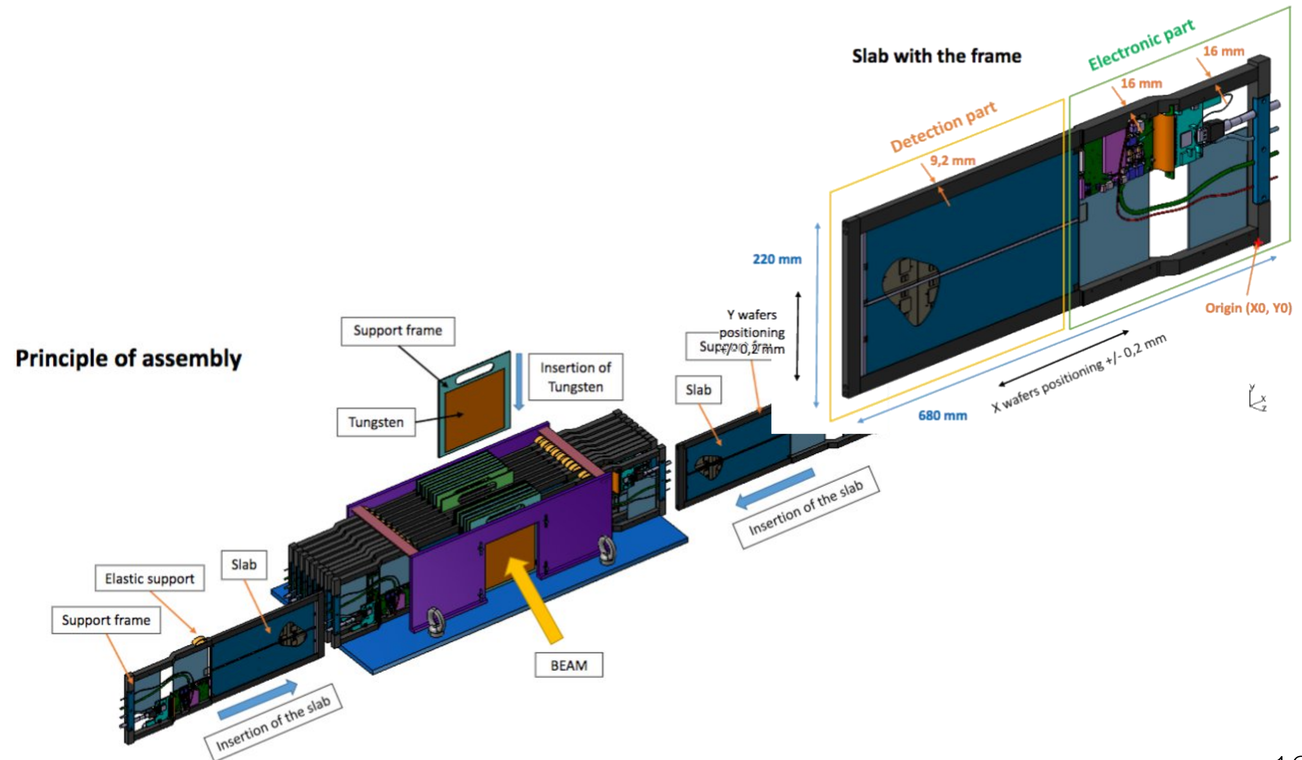
- Readiness review mi-April

Analysis + of nov 15 data.

- ⇒ Start of assembly for second batch …

⇒ Test of 20 SLABs early in 2018

- with new structure [Guillaume Fayolle]



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      - » slower clock (less edges)
      - » absolute noise rate determination

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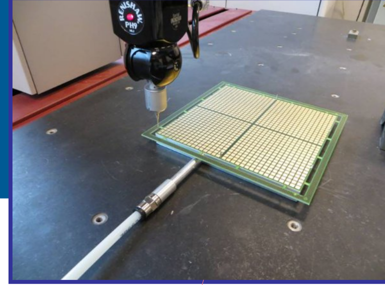
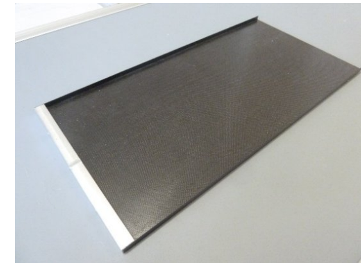
- Assembly bench adaptation @ LLR ⊗ LPNHE ⊗ LAL
  - thicker wafers for shorts slabs
  - **Long SLAB preparation**
  - Test of gluing with thin PCB’s

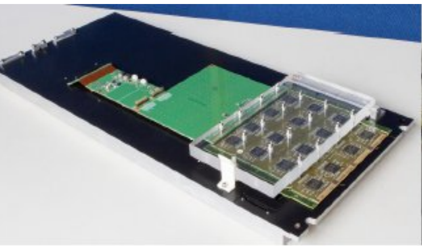
Full assembly chain

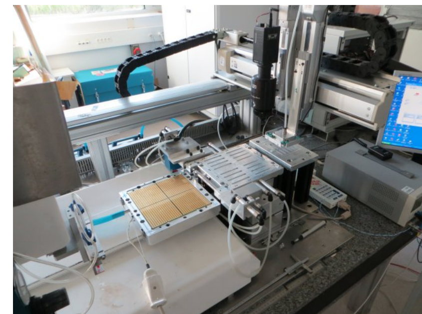
resp: R. Cornat

J. Nanni, M. Louzir, M. Frotin,
J. Bonis, P. Cornebise, J. David,
D. Lacour, S Pavy, P. Ghislain







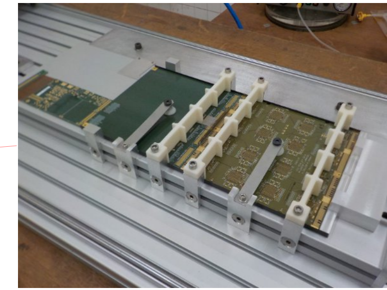


‘Simplified view’

LLR
- Cradle → Dimension check
- SMB → Electrical Testing
- DIF → Electrical Testing
- Raw PCB
- Cabling (ext) → Electrical Testing
- Wafer → Check of specifications Dimensions, Electrical (I, V, C), Visual aspect
- Functionnality tests → Validated SLAB

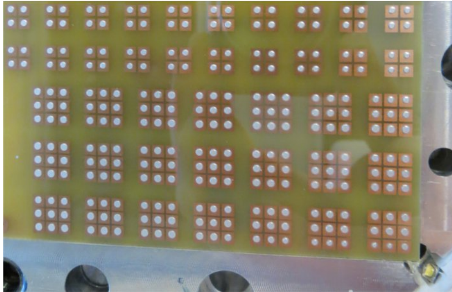
LPNHE
- Dimension check
- Dimensions check → Glue Deposition
- Positioning
- Gluing → Electrical testing → ASU

LAL
- Dimension check → Positioning and Gluing ← Kapton
- Dimension check → Positioning and Gluing
- Dimension check → Positioning and Gluing
- Dimension check → Positioning and Gluing
- Soldering ← Interconnexion Kapton
- Electrical test
- SLAB

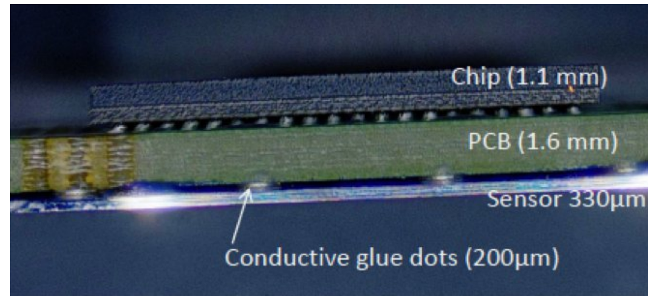


Test beam prototype and assembly process

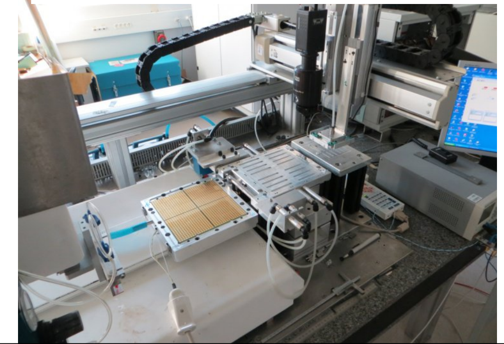
ATLAS HGTD prototype

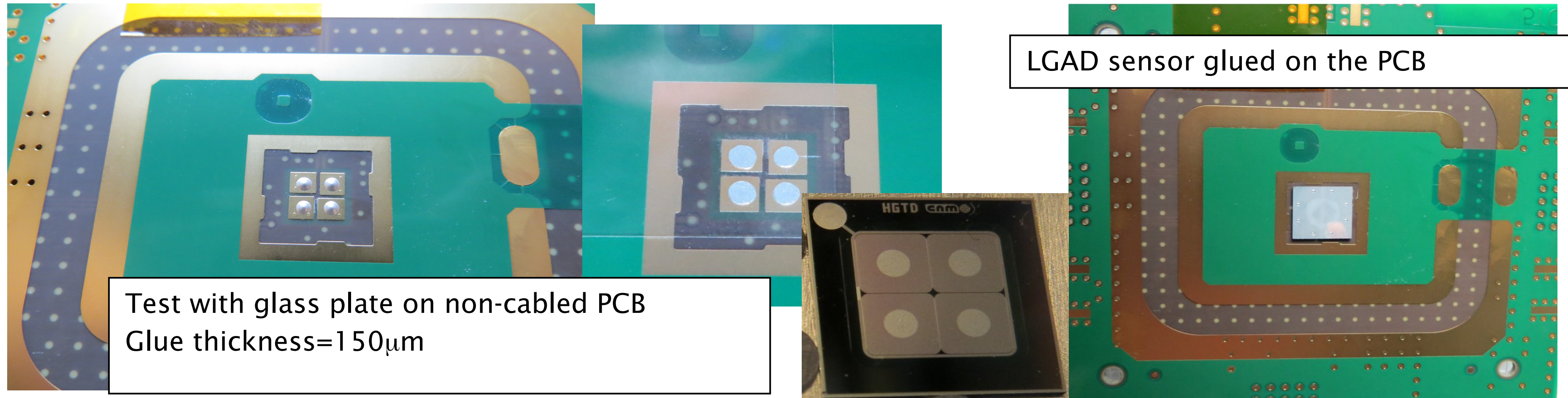


Active Sensor Unit after gluing



Gluing and positioning robots



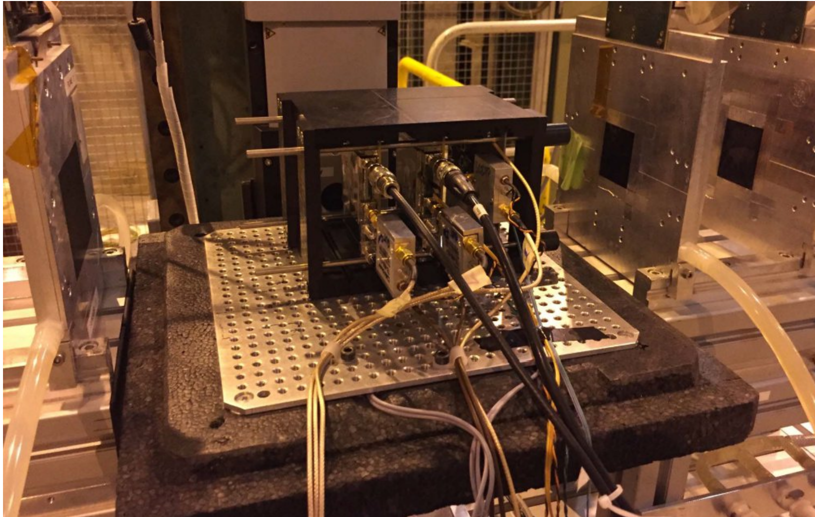


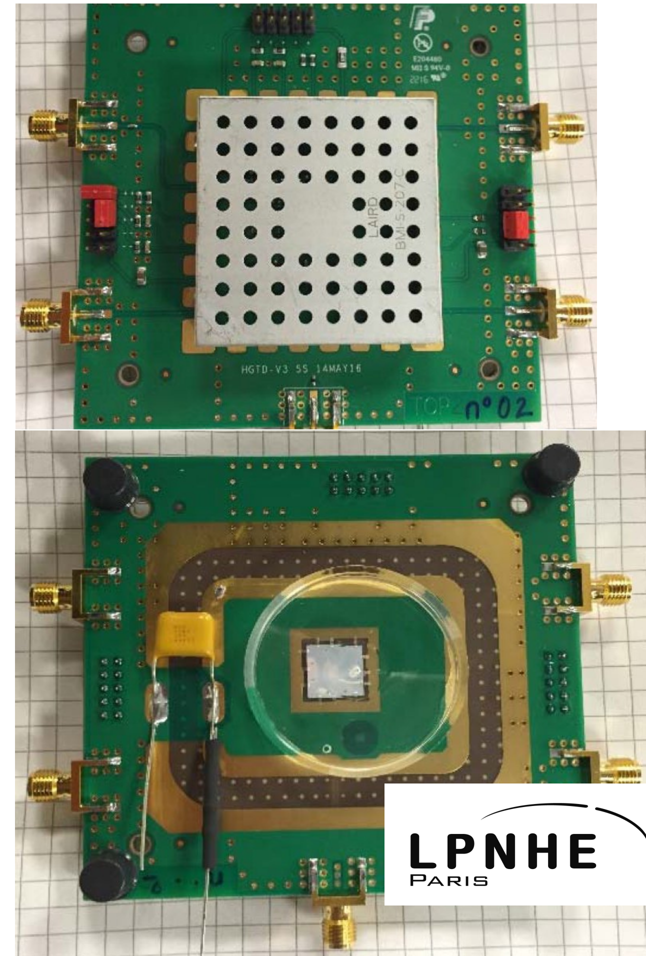
LGAD sensor glued on the PCB

Test with glass plate on non-cabled PCB
Glue thickness=150μm

Test beam

August and November 2016 – 120 GeV pions



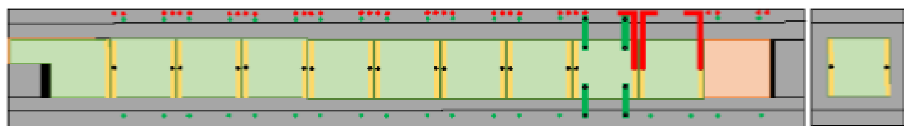


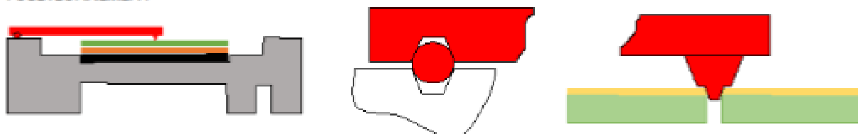
- 2 sensors IN2P3 3x3 mm^2 :
  - PIN diode
  - LGAD

Test bench for Long Slab Assembly

Mechanical [Julien, Alice]

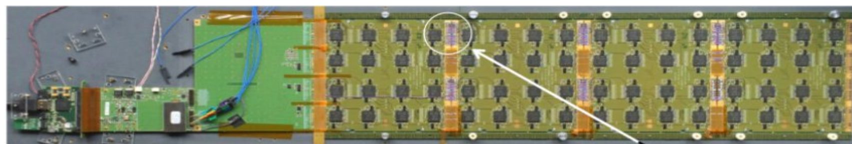
- Precision needed
  - Cumulative errors ⇒ need for positionning



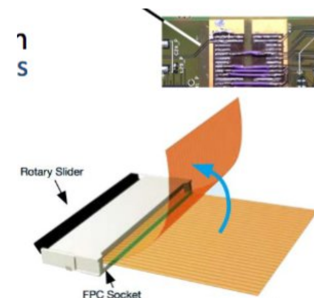


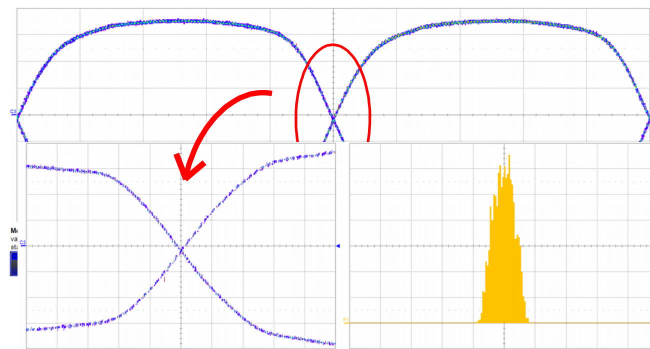
- 3 methods proposed
  - with risk evaluation… in discussion.
- Assembly bench upgrade beginning of summer

Electronics [Jérôme]



- 4 ASU set-up †
- New one ⇒ 10-12 ASU with
  - Soldering OR Connectors
  - Some baby wafers
    - Way to emulate missing ones





Wafers (Rémi, Taikan)

"Edgeless wafers"integrated in 2 of the 10 SLABs

- needs BT data (with muon beam ⟶ edge scan)

Baby sensors

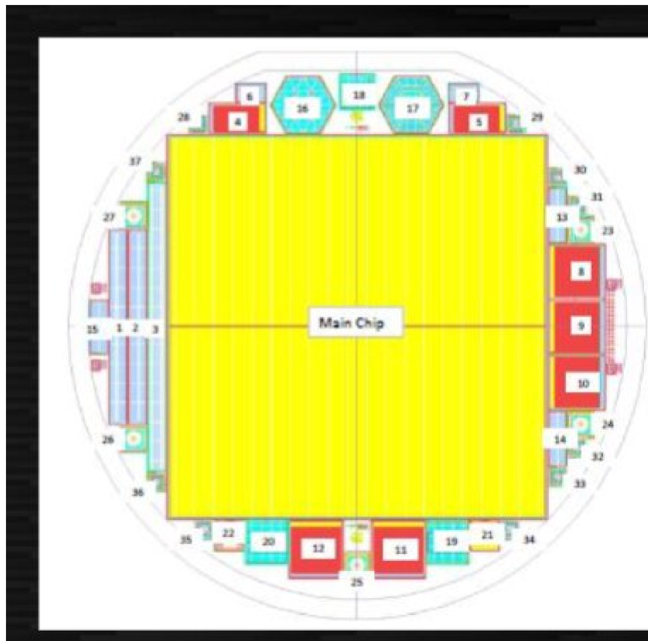
- HPK change or resistivity in 2013 (without notice)
- Parasitic production

Position Sensitive Detector

- Laser scan
  - reconstruction.

Production of SLAB in Japan (if budget)

- FEV altern.
  - existing version FPC (Kapton) ; Hexagonal 8"



320 μm thickness
lower resistivity

16,17: Hexagon
(hexagonal cells,
triangular cells)
19,20: 4x4 (small pix)
(0 GR, 2 GR, 2.5 mm)
21,22: PSD (7 mm)
(meshed, non-meshed)

Each > 40 sensors

News from HGCAL; preparation of BT in May

Some choices made during the last 2 months

- **not to** use a carbon fibre structure for HGCAL
  - more flexibility in technical choices
- Lead/Cu instead of W (for cost reasons) as absorber

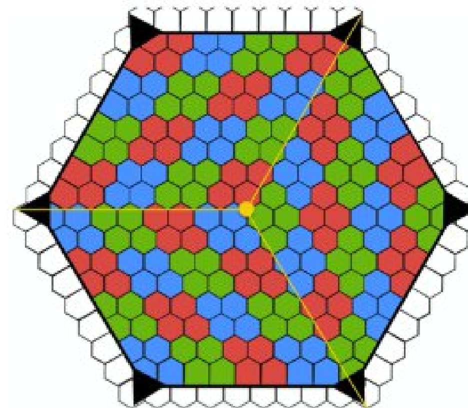
Pending: internal geometry (30° vs 60° elements)

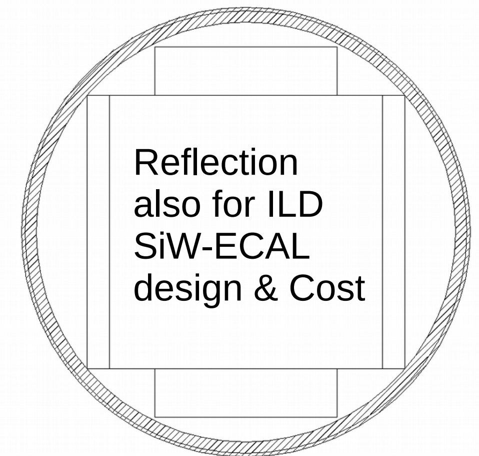
Technical Review of Square vs Hexagonal wafer

- started 9th of Nov. 2016, ~finished
  - almost definitive choice made to stick to hexagonal geometry
    - review with Wafer producers of 2 options
      - » with side wafers for square
    - yield, number of channels (power consumption ∝), coverage, geometry & trigger issues, …

ASIC's

- SKIROC2CMS gives acceptable results
  - ⇒ will be used for future Beam-Tests
- SK2A available for SiW-ECAL
  - Comparative tests @ LLR on-going





Deliverables & Milestones

Milestone number	Milestone	Related WPs	Est. date	Means of verification	Exp'd Del. date	
MS14	Assembly and QA chain demonstration for highly granular silicon calorimeters	14.3.1	M12	2-3 operational layers produced	30/04/16	23/06/16
MS15	Design specifications of test stations for irradiated silicon sensors and LHC oriented front-end electronics	14.3.1	M12	Report to StCom	30/04/16	24/06/16

Deliverable (number)	Deliverable name *(short description of deliverable)*	WP	Lead Participant	Type	Del. Month	Delivery Date
D14.3	Advanced Assembly chain for Si calorimeters *(prototypes assembly and technical documentation of process)*	14.3.1	CNRS	DEM	M36	30/04/18
D14.5	Common running of calorimeter prototypes *(technologies embedding Central DAQ standards from WP5 and performance results)*	14.4.1	DESY	DEM	M36	30/04/18

Networking

1) Infrastructure: To what extend is your work an infrastructure or part of an infrastructure that can be used in the European (and beyond) Research Area?

- Assembly benches techniques :
  - DAQ SW (Pyrame)
  - ASIC test → Ωmega chips,
  - Spring array & Gluing benches for PCB with pad readout,
  - pick and place for sensitive devices

2) Network: Does your work belong to a bigger network on similar research topics (this is similar but not exactly the same as 1))?

- P2IO: local to Paris region

3) Synergies: Do you create synergies beyond your actual field of working ?

- Counter-question: What is «the field of working» ? Silicon Sensors, Calorimetry, Detectors, HEP, Physics, Science, … ?

4) Industrial partners: Are you in contact or will you in the near future establish sustained contacts with industrial partners (of any size)?

- Hamamatsu (Wafers), Eolane (Assembly of Electronics components)

Extras

Overview ILD & RnD

From Japan & IN2P3

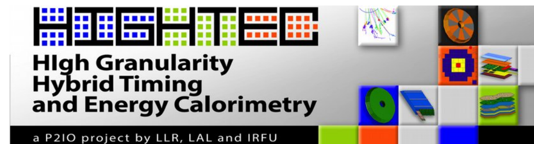
– Cost reduction : ⟶ redesign of ILD

– Support in France

- IN2P3 ⇒ Prototype & Beam Test

- AIDA-2020: assembly benches & BT

- HIGHTEC from P2IO
  [LLR, LAL, Saclay] ⊗ [CMS,CALICE,ATLAS]
  – HIgh Granularity Si CALOs
  – R&D: Long SLABs, COB, DAQ
  – PostDocs [Artur, Adrian]



Effort in design of ILD well restarted

… and documented!

⇒ criteria for prototypes

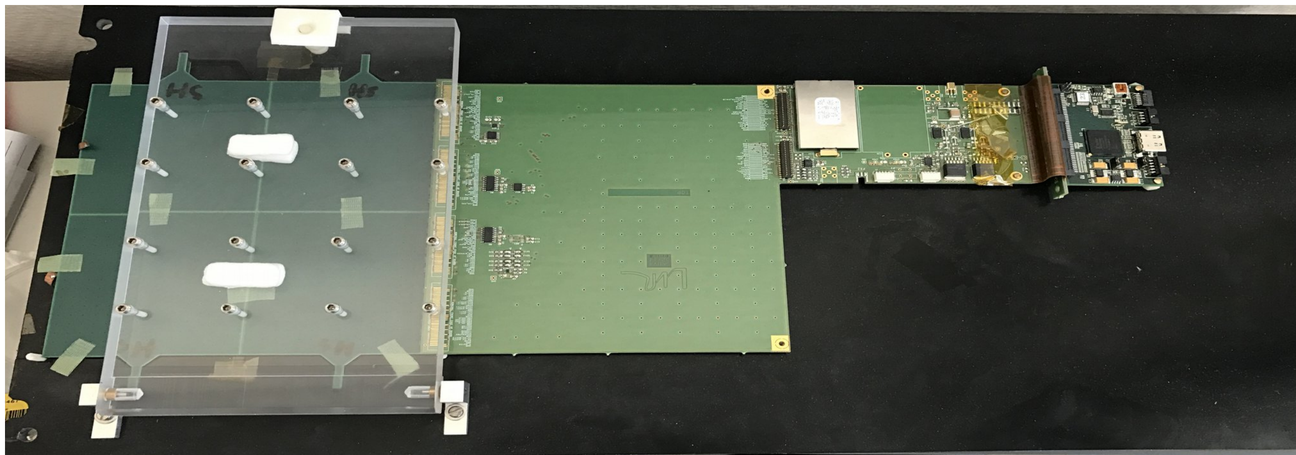
Main priorities

– Test of prototype [June 2017, 2018]
  - And analysis
  - No more BT in sept 2017
– Check critical Studies and R&D for ILD
  - e.g. Long SLAB
  - DAQ, geometry

↔ with contracts planning

Studies ASU with wafers

3rd bench



Goals:

- Mesure the leakage current,
- Compare level of noise, Scurves …
- Linearity of analog channel
- …