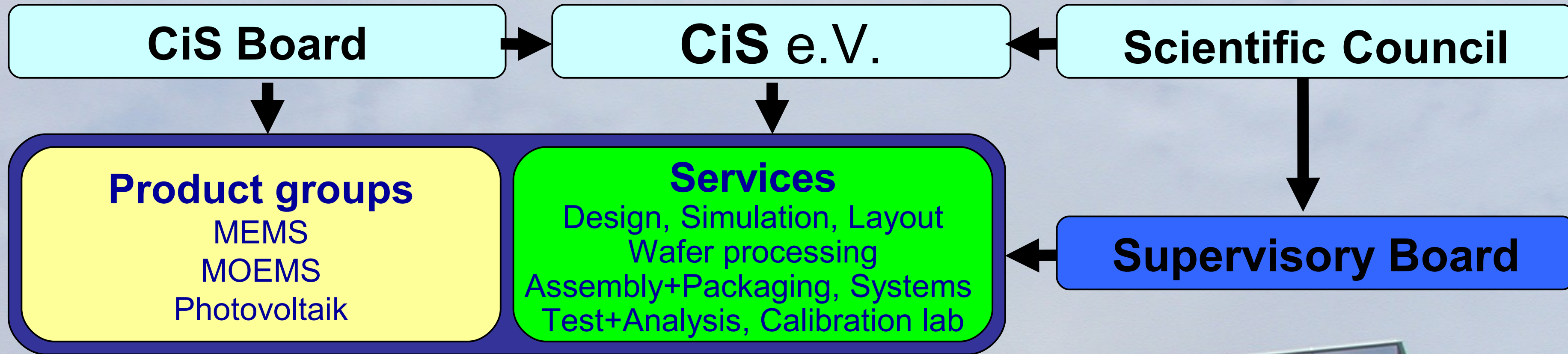
CiS Research Institut for Microsensors and Photovoltaics



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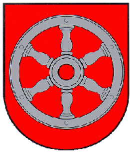


History

1993 Spin-off CiS

1996 DIN EN ISO 9001

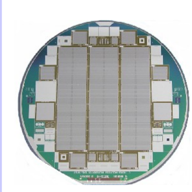
1997 First Prototyping of Silicon Radiation Detektors for HEP

1999 CiS Institut für Mikrosensorik gGmbH

2003 Technology Center AZM

Bussiness Centre for Application of Microtechniques

2004 Start of new clean rooms



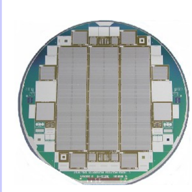
Outline

CiS in Brief

- CiS in numbers
- Products and Services
- Examples of Processing Equipment
- References
- Testing & Quality Assurance
- Present and Future Activities

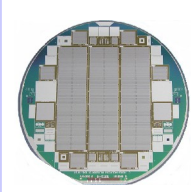
Radiation detectors for HEP application

- Process resources
- Process capabilities
- Bottle necks and risks
- Volume production scenario



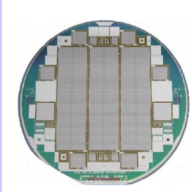
CiS in Brief

- CiS in numbers
  - Turnover 2008: 9.4 kEUR
    - Public sector and strategic programmes 51 %
    - Industrial contracts R&D 35 %
    - Industrial contracts (components) 14 %
  - Employees: 92
    - Scientists: 71 (11 with PhD)
    - Operators/skilled staff: 12
  - Qa system approved to ISO9001:2008
  - Clean room:
    - 70 m^2 acc10
      (high temperature processes, resist processing lab, ...)
    - approx. 200 m^2 acc100
      (test lab, assembly, ...)
    - 200 m^2 acc 10,000
      (services, assembly, packaging)



Competence in Silicon
Fields of CiS Activities

- **Research of new Sensor Principles**
- **Development** *Application Specific Solutions*
  - Chip Design + Layout + Mask set
  - Design of Components
  - Technology Simulations (Silvaco, FEM)
- **Wafer Processing**
  - 4 inch some process steps already in 6 inch (capable)
    equipment partly 6 inch compatible
  - Silicon (FZ, CZ, n-typ, p-typ, epi, bonded wafer)
  - Glass
  - Pre- and Post-Processing (DOFZ, UBM, ...)
- **Assembly and Packaging**
- **Test and Analysis**



Products and Services

- Research
  - Applied and business research
  - test wafer prototyping for R&D projects
- Application studies
- Technology development
- Prototyping
  - Multi-Project/Chip-Wafer-Services
- Series production

  up to a few thousand wafer p.a.
- Foundry services

Main Products

CiS Forschungsinstitut für Mikrosensorik und Photovoltaik GmbH

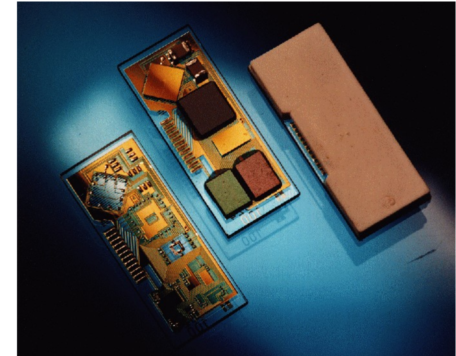
PIN-Diode Arrays

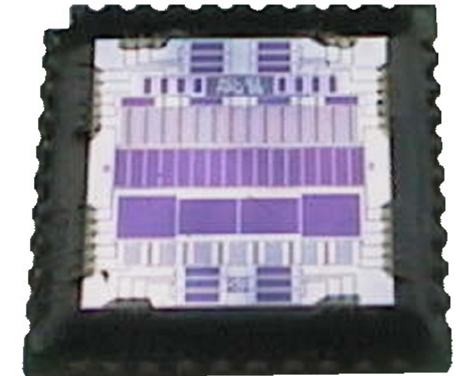
Emitter-Receiver-Modules

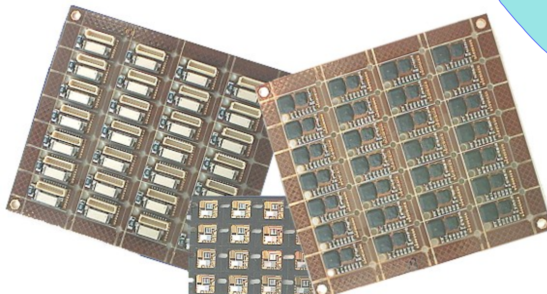
Silicon Radiation Detectors

Humidity Sensors

MEMS





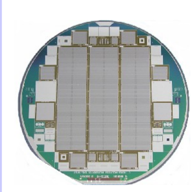


Examples of Processing Equipment

- High temperature facility
  - ◦ dry and wet oxydation (O_2,HCl, H_2O, /O_2) without organics !
  - ◦ oxygen enrichment (DOFZ)
  - ◦ anneling steps (N_2 800…1200°C, H2 …420°C)
  - 6 inch capable
- Automatic coating and developing cluster for double-sided processing
  - 6 inch capable
- Double-sided alignment and exposure facilities
  - 2009 BA/MA6 → 6 inch capablility planed
  - alignment precision rear to front side better than 5 µm (normal ~ 2 µm)
  - BA/MA6 → ~ 1 µm
- Projection photolithography: projection mask aligner (up to 4 inch)
  - 2009 MAP600 → 6 inch capable
  - PEB

Examples of Processing Equipment

- Spray coating equipment
  - new equipment developed → 6 inch capable
- Lift-off masks for UBM
  - single layer resist system or ▪ double layer resist system
- galvanotechnical UBM in application (like IZM-process, licenced by IZM)



External Technology Steps

- **Epi layer**
  - Okmetic (certificated supplier) + ITME (R&D)
- **Silicon Fusion Bonding** → **CiS 2009**
- **Wafer Polishing**
  - Okmetic (certificated supplier)
- **CMP**
  - ZMN Ilmenau
  - …
- **Implantation**
  - **Ion Beam Services (F + GB high dosis fascilities)** **IBS Rousset** **IBS Bathgate**

    → Boron, Phosphorus, Arsenic, …
  - **FZ Dresden-Rossendorf**

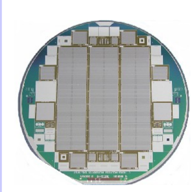
    → high energy implantation

    → unusual dopands
- **Au Metalization**
  - ifw Jena
- **DRIE/ICP**
  - ZMN Ilmenau

Overview CiS-production of radiation detectors

Detector	HEP / CP	Detector Typ			Batch Qty	Wafer Qty	Yield 1AP	Yield 1AT	Yield 1AG	Yield 2AT	Yield 2AG	delivered
N768	EURISYS	dsp Microstrip	ac	n-bulk FZ	22	528	89%	85%				400 pcs wafer
ALICE S2	Canberra / CERN - LHC	dsp Microstrip	ac	n-bulk FZ	62	1488	96%	85%	82%	98%	86%	1.280 pcs wafer
ATLAS WEDGE	CERN - LHC	ssp Microstrip	ac	n-bulk (DO)FZ	217	5208	95%	75%	72%			3.300 pcs wafer
H1-PHI 1st Production	DESY	ssp Microstrip	ac	n-bulk FZ	8	192	98%	91%	89%	85%	85%	120 pcs wafer
H1-PHI 2 nd Production	DESY	ssp Microstrip	ac	n-bulk FZ	8	192	94%	84%	80%	80%	80%	150 pcs wafer
ATLAS PIXEL Preseries	CERN - LHC	dsp n-in-n Pixel		DOFZ	4	96	88%		47%			30 pcs wafer
ATLAS PIXEL	CERN - LHC	dsp n-in-n Pixel		DOFZ	60	1440	92%	67%	61%			800 pcs wafer
CMS PIXEL Prototyping	CERN - LHC	dsp n-in-n Pixel		DOFZ	3	72	79%		51%			25 pcs wafer
CMS PIXEL Series with UBM	CERN - LHC	dsp n-in-n Pixel		DOFZ	24	576	78%		92,2%			410 pcs wafer
CMS PIXEL Half M. Series with UBM	CERN - LHC	dsp n-in-n Pixel		DOFZ	4	96	81,3%		96,9%			50 pcs wafer
XPAD3_01		ssp p-in-n Pixel		FZ	2	42	91%		88%			37 pcs wafer
BTeV_01_Prototyping		dsp n-in-n Pixel		DOFZ	2	48	87,5%		77%			35 pcs wafer

ssp MS	3.570 pcs wafer
dsp MS	1.680 pcs wafer
ssp PS	37 pcs wafer
dsp PS	1.350 pcs wafer



Radiation Detector References

- **Micro-strip detectors**
  - **R&D single-sided**

    → SDTWnn prototyping R&D CiS → Uni Hamburg
    → RD50

    - **DOFZ, FZ, epi (high ohmic, up to 150 µm thick), CZ, MCZ**
    - **n-typ and p-typ**

  - **Production single-sided**

    → ATLAS WEDGE W12

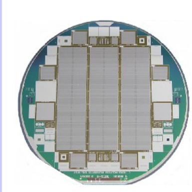
    - DOFZ, **implanted bias resistors**, ac, **moderated p-spray**

    → ATLAS WEDGE W21, 22, 31, 32

    - **implanted bias resistors**, ac, **moderated p-spray**

    → H1-PHI

    - **punch-through biasing**, ac, field plate



Radiation Detector References

- **Micro-strip detectors**
  - **R&D double-sided**

→ D0 prototyping delivered to Eurisys / F

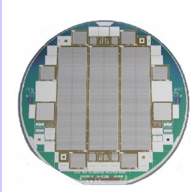
- **poly-silicon-resistor biasing**

→ CBM01 + SPID GSi / FAIR

- **punch-through biasing,** ac,
  double metalization layer (front side)
- **poly-silicon-resistor biasing**

→ SDTW07 R&D CiS

- **p-typ-bulk, p-typ-epi**
- **punch-through biasing,** ac,
- **poly-silicon-resistor biasing**
- **poly-silicon filed plates**



Radiation Detector References

- **Micro-strip detectors**
  - **Production double-sided**

→ STAR delivered to Eurisys / F

- **punch-through biasing**, ac, field plate

→ N768 delivered to Eurisys / F

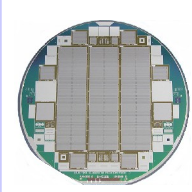
- **punch-through biasing**, ac, field plate

→ ALICE S2 delivered to Canberra / B

- **punch-through biasing**, ac,
  front side p-strips, back-side n-strips isolated by **p-spray**

→ AMS-2C (150 pcs) delivered to MSU / RF

- thick HT-oxid (650nm), **FOX-FET biasing**, dc,
  front side p-strips, back-side n-strips isolated by p-stop



Radiation Detector References

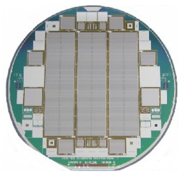
- **PIXEL detectors**
  - **R&D single-sided**

→ XPAD3 prototyping delivered to cppm / F

→ SDTW07 R&D CiS

R&D test chips for other institutes

- **p-typ-bulk**
- **poly-silicon-resistor biasing**
- **poly-silicon filed plates**



Processing example
Under Bump Metallization

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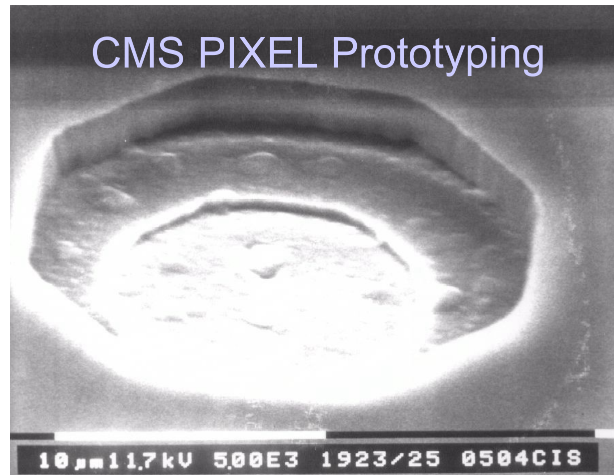
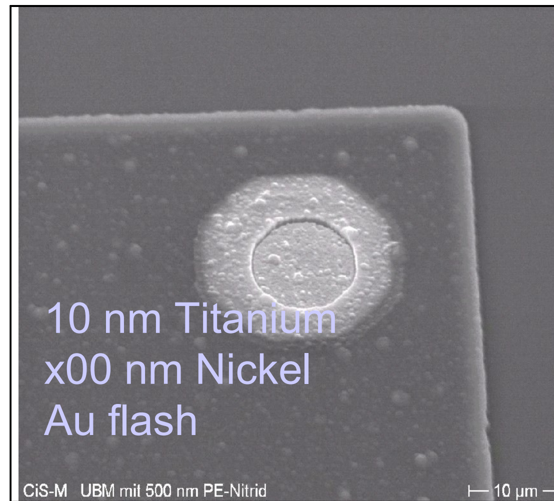
• single or double layer resist system
• special remover





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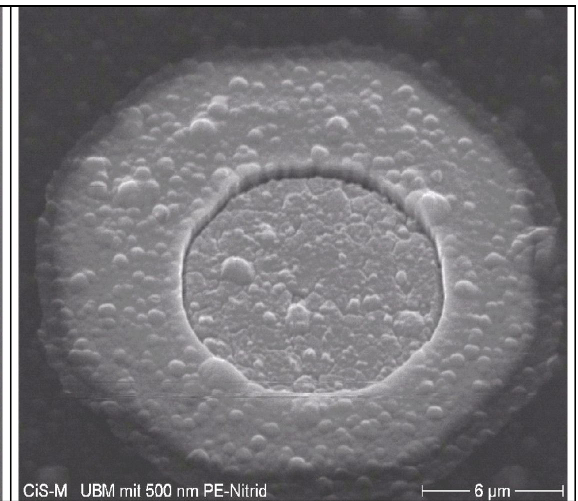

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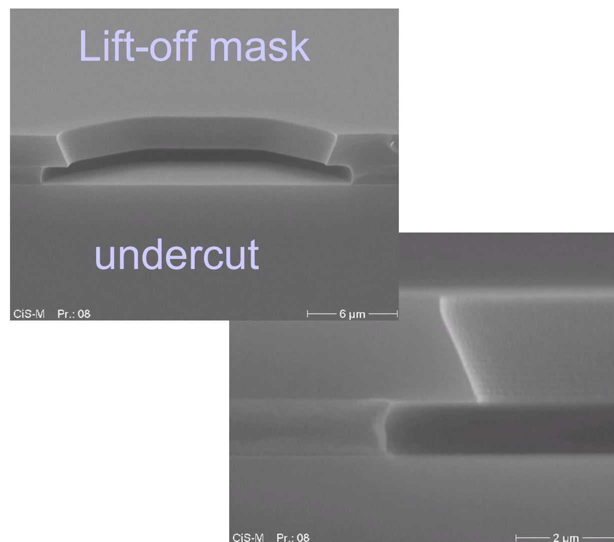

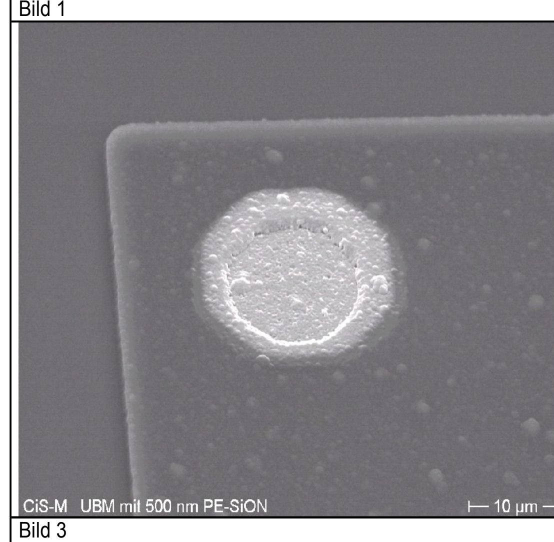

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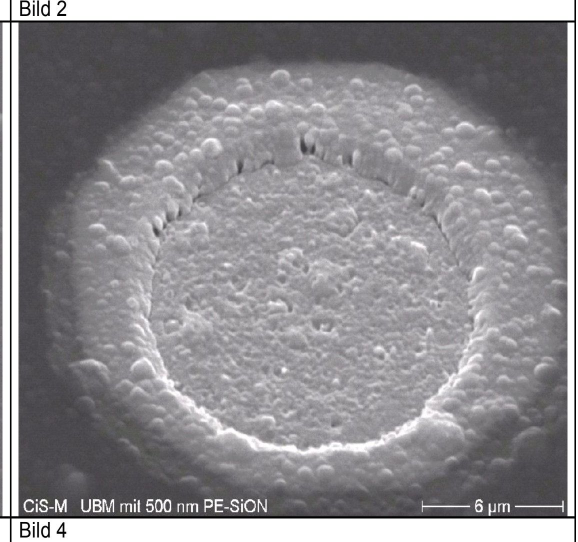

Bild 4

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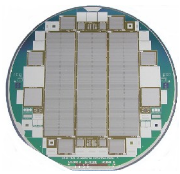


Road Map HEP detectors

Productivity
Application fields

6 inch Cluster
4 inch Processing

6 inch ssd detectors
350 µm thick
(2010)

epi detectors

ssp & dsp
radiation hard
detectors

APD
Arrays

Sensor
Chips

Sensors
with
active components
on-chip

Multi-Domain-
Micro-Systems

Through Silicon Vias
Silicon Fusion Bonding
Wafer / Chip stacking

Technological
Level

Wafers
Micro Systems
Chip-scale Systems

Wafer Processing Capabilities

- Clean Room Operating: three-shift working regime
- Capabilities: about 4,000 Lithographies per month

  ⇒ 50,000 technological layers p.a.

  that means for instance

  up to 3,000 pcs double-sided PIXEL wafers

2009/2010 new equipment

+ additional capability

more than 10,000 Lithographies per month

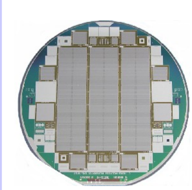
Volume production scenario II

- Alternative wafer processing 6inch
  - X-FAB is located in the same area as CiS
  - already very close co-operation

    →processing of Microstrip detectors for Eurisys before it was transfered to CiS

    →design and test will performed by CiS
  - X-FAB: 6 inch
    - BiCMOS 0,6 µm ⊕ 0,8 µm
    - CMOS (Fab in Erfurt) 0,6 µm ⊕ 0,8 µm ⊕ 1,0 µm
      - hihg voltage module available
    - CMOS (other Fabs) 0,18 µm ⊕ 0,35 µm ⊕ 0,6 µm
- Advantages:
  - higher processing capabilities: min. 3.000…5.000 wafers p.a.
  - shorter target times

    →implantation in process line integrated (in Erfurt vs. ibs/F)
  - Process quality: improved inline-monitoring and quality system (certificated ISO 9001:2000 and ISO/TS 16949:2002)



Additional tasks

- CiS wafer processing capability
  - 4 inch usual   some key steps also in 6 inch available
  - advantage of 4 inch wafers for double-sided PIXEL: processable 250 µm thick wafers
  - throuput more than three thousand wafers per year
  - batch processing time
    - ssp R&D / Prototyping batches   12 … 14 weeks (normal service)
    - ssp 4 and more batches   9 … 12 weeks
    - dsp R&D / Prototyping batches   14 … 18 weeks (normal service)
    - dsp 4 and more batches   12 … 14 weeks
    - hot runs available   < 6 … 8 weeks

Bottle necks and risks

- **Bottle necks:**
  - Implantation limited by external services (ibs): logistics
  - Lithography: limited by number of mask aligners (planned invest)
  - Furnace:
    - if DOFZ will be necesarry (24 h target time)
    - poly resistors (capability, process control)
- **Risks:**
  - tight in-line parameter control for production line
  - clear separation of procedures for production and research
    Quality system ISO 9001 approved
  - cost structure: ability to meet price targets
  - Process and detector quality: inliost structure: ability to meet price targetsne-monitoring parameters
  - Limitations in production capabilities
    by equipment repair service and maintenance

    → invest to remove bottle necks and limitations

    → alternative scenario for volume production

Thank You for Your Attention !