# Improvement of planar silicon Pixel Sensors for the ATLAS ITk upgrade

BCD School Cargèse, April 5th 2017

Sascha Dungs

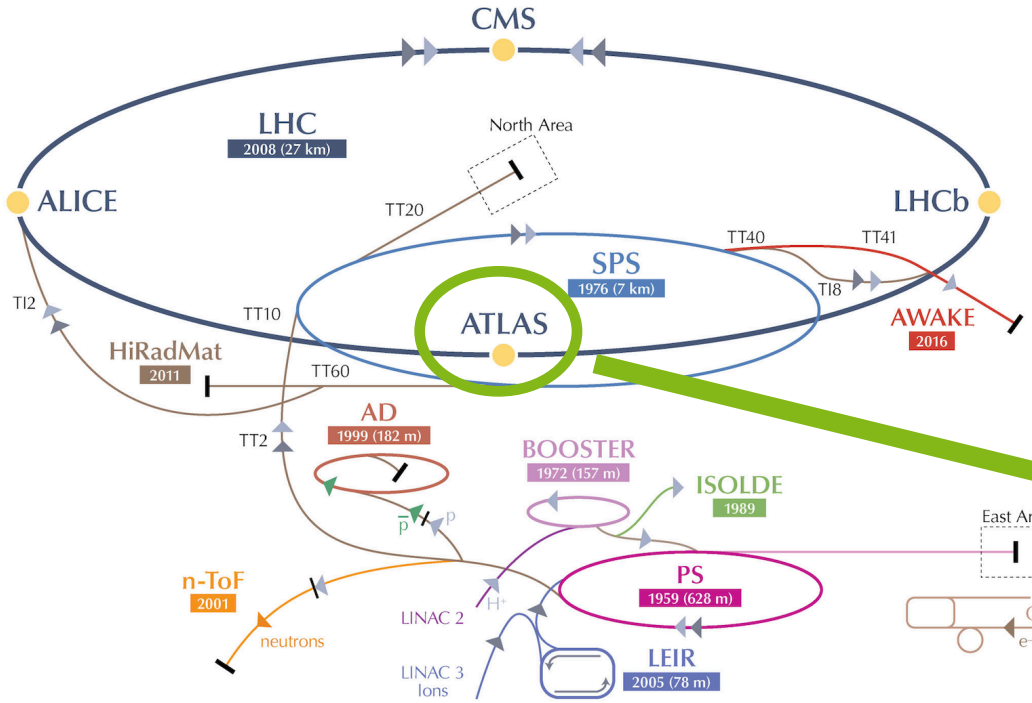
TU Dortmund, Experimentelle Physik IV

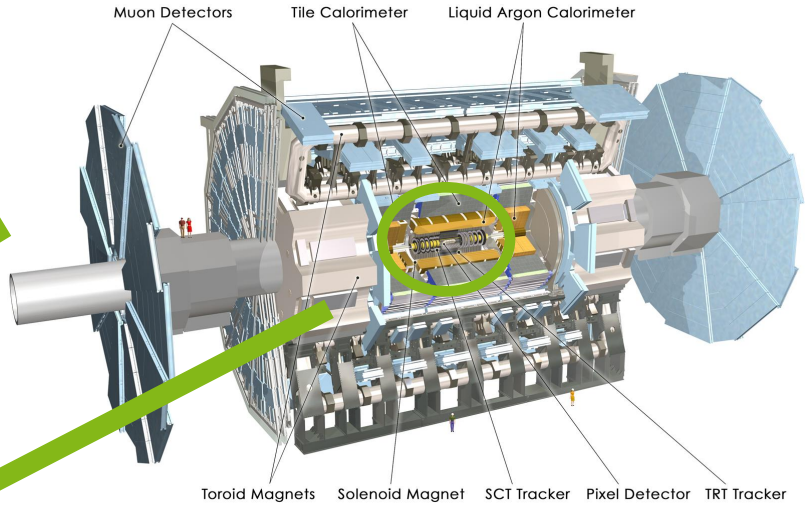
technische universität dortmund

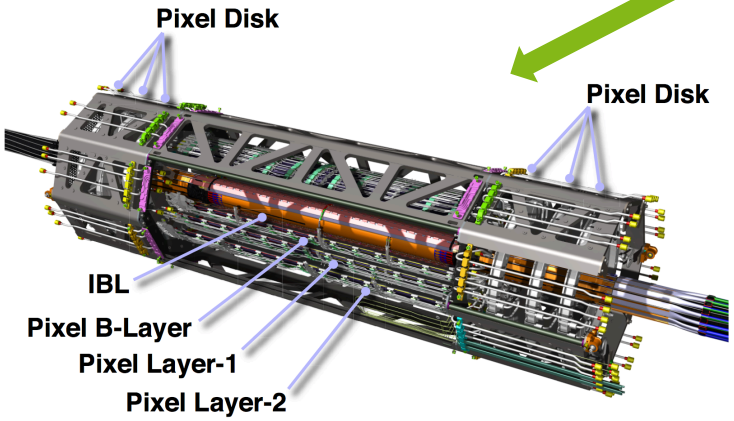
ATLAS EXPERIMENT

# ATLAS Pixel Detector



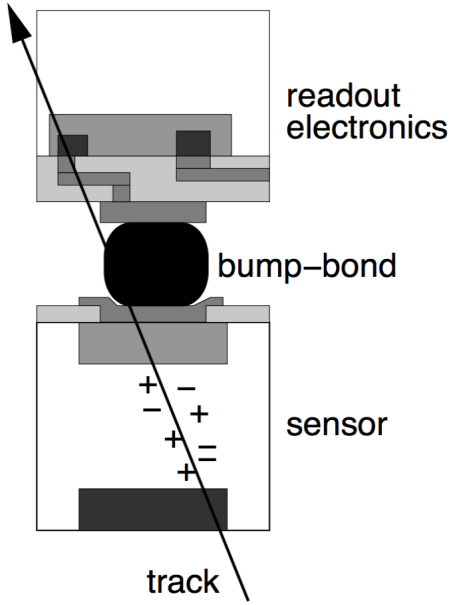


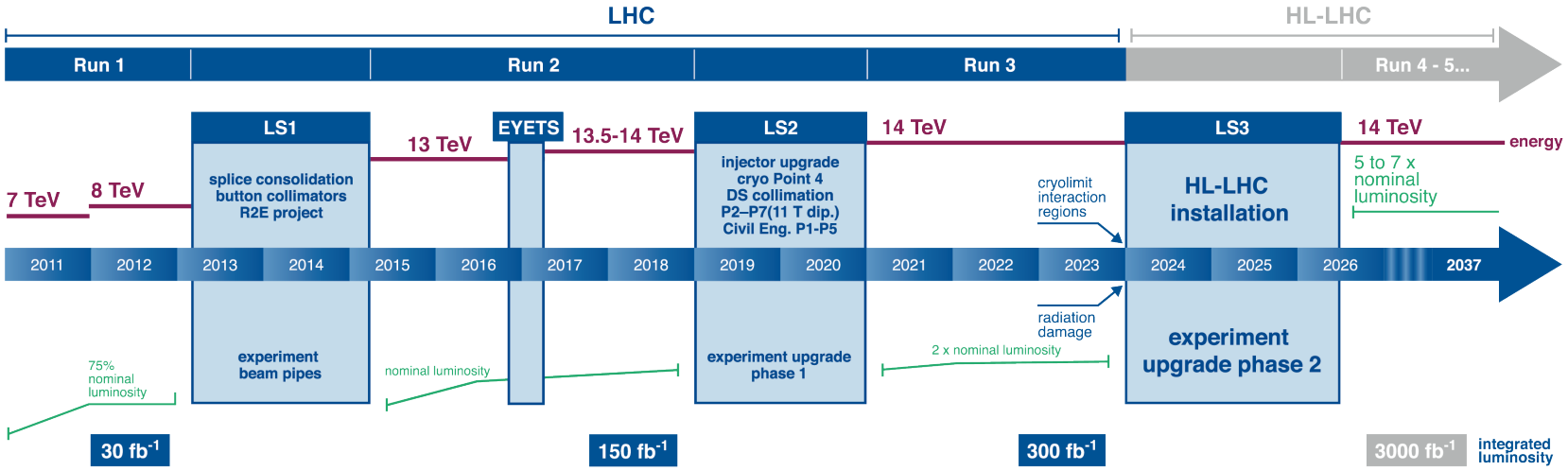



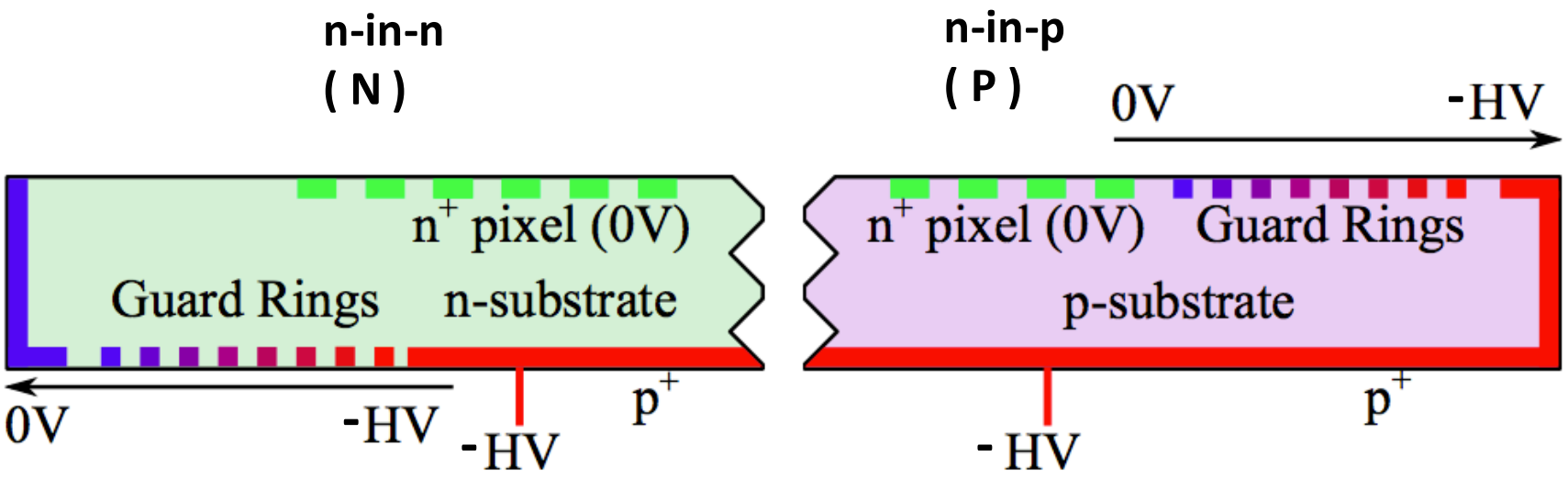
# LHC / HL-LHC Plan

- currently the pixel detector consists of hybrid modules with n-in-n type pixel sensors
- for the phase 2 upgrade the inner detector will be replaced completely
- final layout is not set yet, but well-established hybrid concept is preferred
- n-in-p type pixel sensors could be a possible cost-effective alternative for n-in-n sensors



# Sensor Types




- front side: $n^+$-implants (→ pixels)
- back side : $p^+$-implants
- Guard Rings for defined potential drop

- n-type substrate
- GR on p-side
- two side processing

- p-type substrate
- GR on n-side
- one side processing

# Tasks

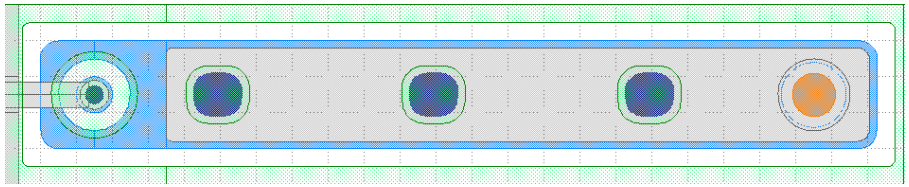
technische universität dortmund

**Design of new n-in-p sensors:**

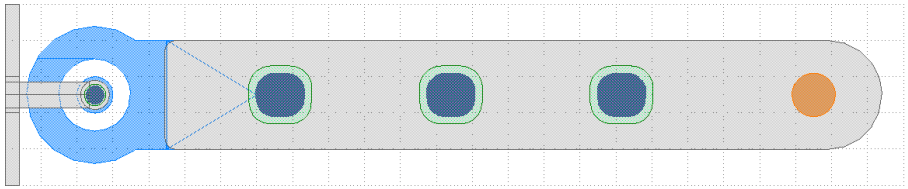
- efficiency improvements
- material reduction

- same design to compare the types
- new FE-Chip -> pixel size 50x50 µm$^2$

Standard n-in-n IBL pixel design (250x50 µm$^2$)



Example for equivalent n-in-p pixel design



**Comparing measurements:**

- IV and CV characterizations are done
- further measurements follow, e.g. hit efficiency

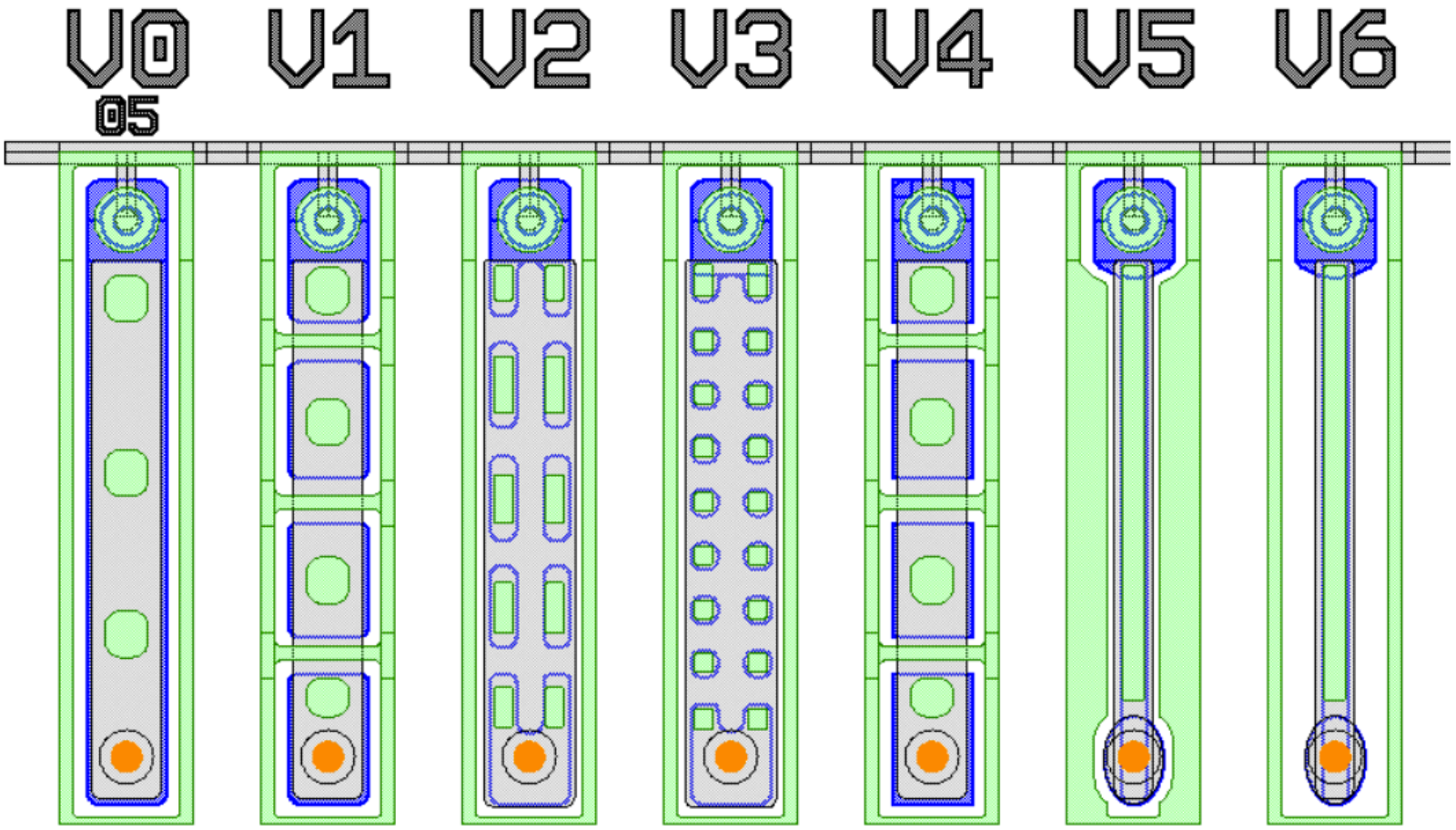
| | D-01 | D-02 | M-01 | M-02 | M-03 |
|---|---|---|---|---|---|
| manufacture | CIS | CIS | HLL | HLL | CIS |
| type | n-in-n | n-in-n | n-in-p | n-in-p | n-in-p |
| thickness [µm] | 200 | 200 | 150 | 150 | 100 |

Thank you for your attention!

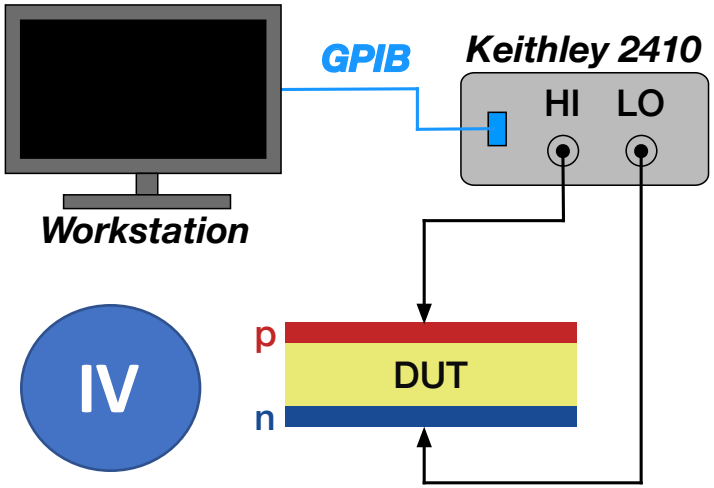
# Backup

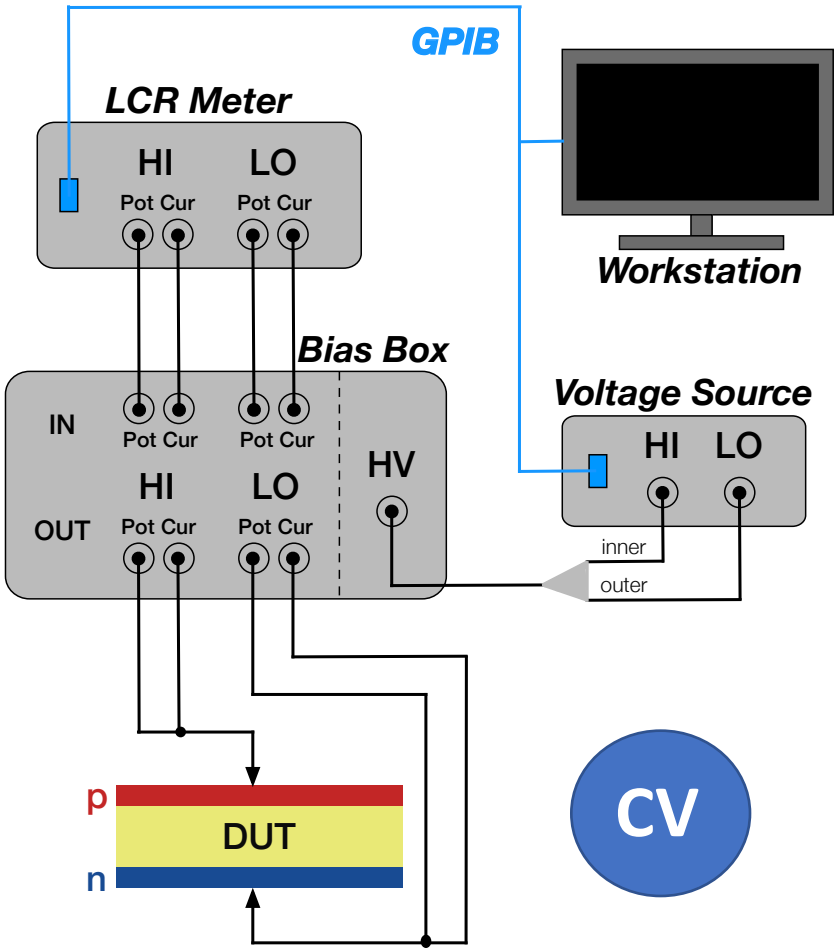
# Pixel Modifications

technische universität dortmund



# Setup for IV and CV Characterizations




Criteria for good sensor:

- thickness $\leq$ 200µm
- leakage current:
  - $I_{total} \leq 0.75\mu A/cm^2$ at 20°C
    $\Rightarrow I_{max} \approx 2.5\mu A$
  - measured at $V_{depl}$ + 50 V

# FE specifications

technische universität dortmund

| | RD53 | *FE-I4* |
|---|---|---|
| technology | 65 nm | *130 nm* |
| Pixel dimension | 50 µm x 50 µm | *50 µm x 250 µm* |
| # of pixels | ~140 000 | *26880* |
| chip dimension | 18 mm x 20 mm | *19 mm x 20 mm* |
| hit rate | 3 GHz/cm$^2$ | 0.4 GHz/cm$^2$ |
| in-time threshold | < 1000 e | *< 4000 e* |
| typ. noise (ENC) | < 100 e | *< 300 e* |
| bandwidth | 5 Gb/s | *160 Mb/s* |
| rad. hardness | > 5 MGy | *> 2.5 MGy* |