State of the art and perspectives of CMOS avalanche detectors

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CERN seminar

January 20, 2017

INFN Istituto Nazionale di Fisica Nucleare

Research on silicon detectors in Trento

Clean room

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Outline

- Introduction
- CMOS-integrated single-photon detectors: an overview
- APiX: Geiger-mode avalanche pixel detectors for ionizing particles
- Conclusion and future perspectives

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Geiger-mode avalanche detectors

a.k.a. Single-Photon Avalanche Diodes (SPADs), SiPM cell

$V_{BIAS} > V_{BD}$

SPAD

R_Q

I_{SPAD}

V_{EX}

Quenching

Avalanche triggering

Recharging

V_B

V_{BIAS}

V_{SPAD}

Geiger-mode avalanche detectors

1 primary generated electron-hole pair: very large current pulse ~10^5 - 10^6 electrons

$V_{BIAS} > V_{BD}$

SPAD

Vout

R_Q

Vout

V_{EX}

time

events

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CMOS SPAD characteristics

Features:

- Single-photon sensitivity → shot noise limited
- Excellent timing resolution: ~100 ps FWHM

CMOS:
- **Monolithic integration** of SPAD and processing electronics
- Arrays → **single-photon imaging**

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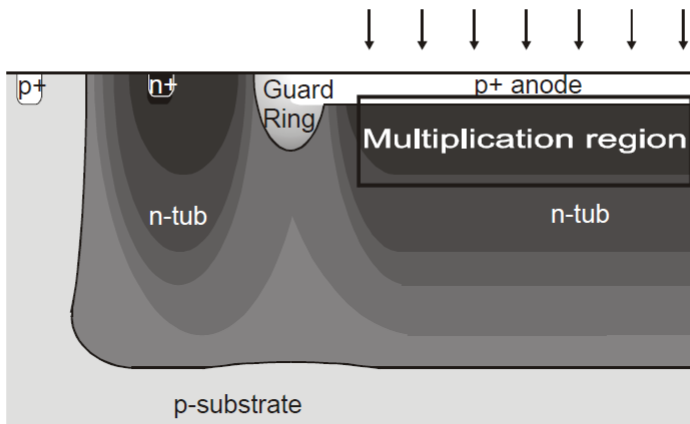
CMOS SPADs: early example at EPFL



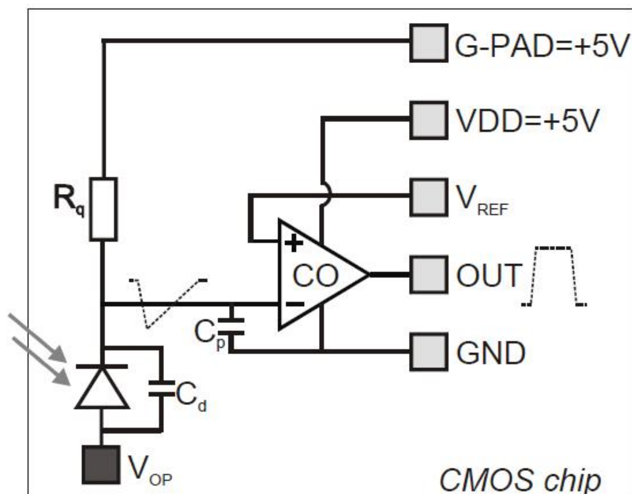
Process: **CMOS 0.8µm**

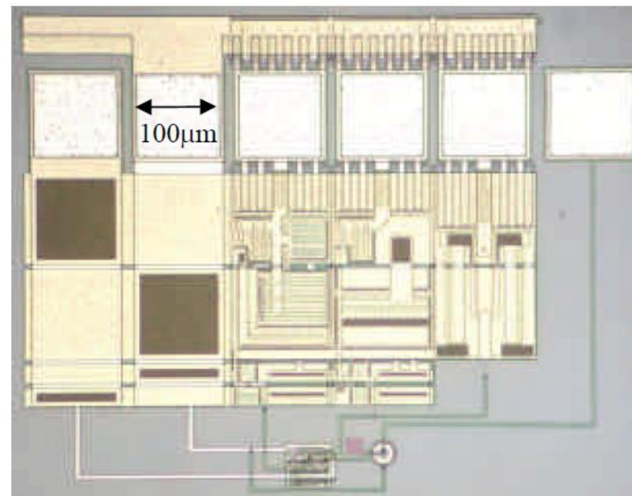
Area: 30µm^2

Peak PDE: 20%

DCR: 300 Hz

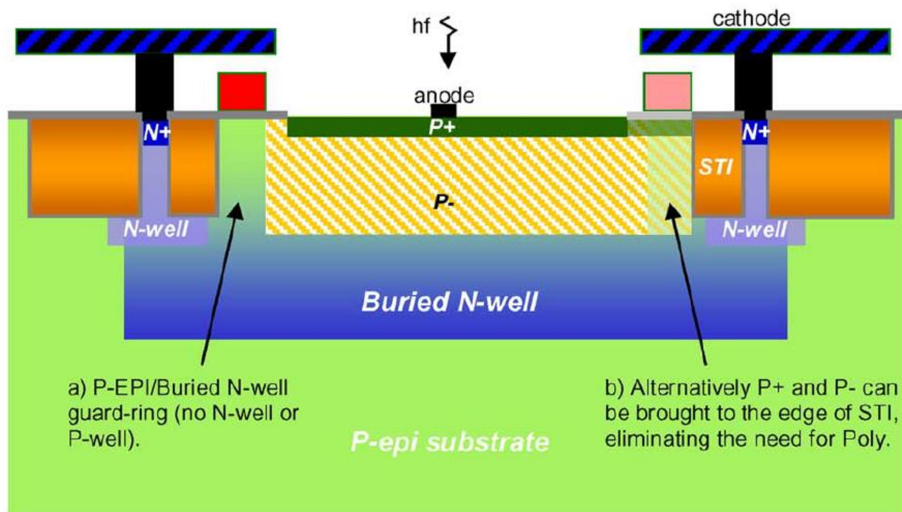
Timing resolution: 50 ps FWHM





A. Rochas et al., Proc. SPIE **2003**

CMOS SPADs: deep submicron



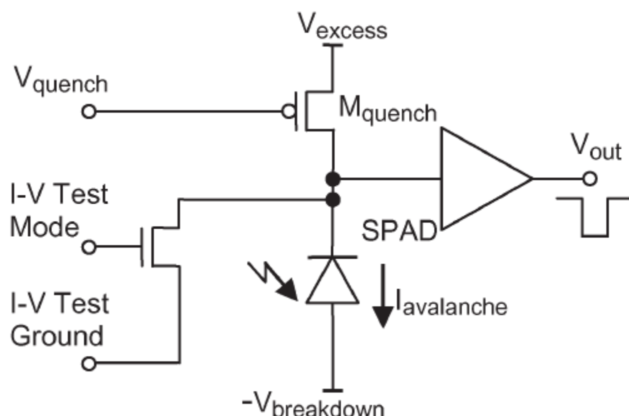
Process: **CMOS 130 nm**

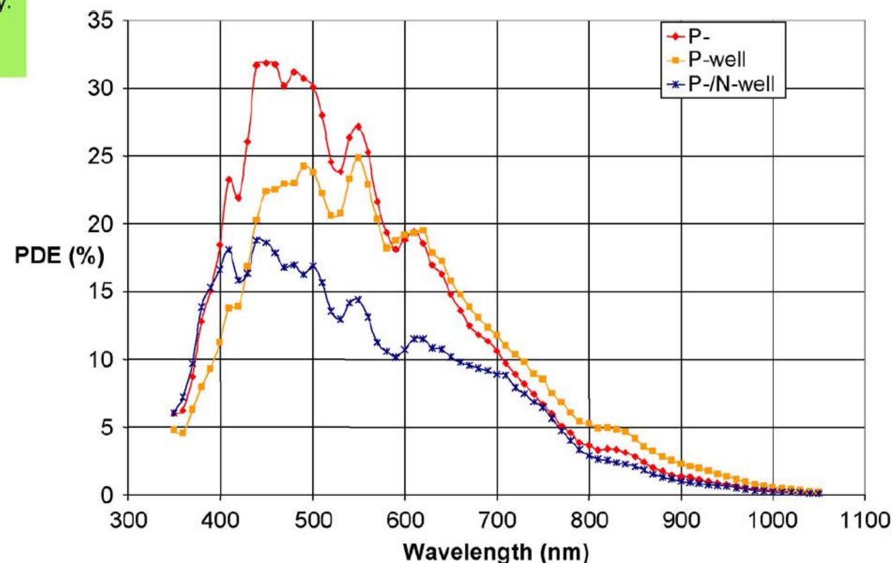
Area: 50μm^2

Peak PDE: 33%

DCR: 40 Hz

Timing resolution: 237 ps FWHM





J. Richardson et al., IEEE Trans. Electron Dev. **2011**

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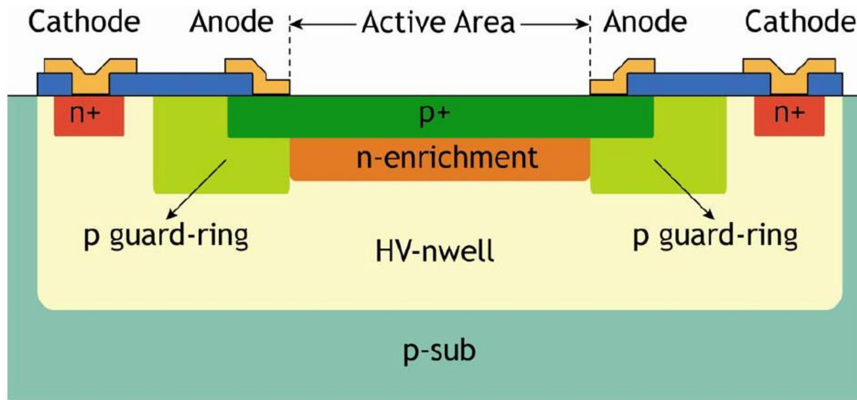
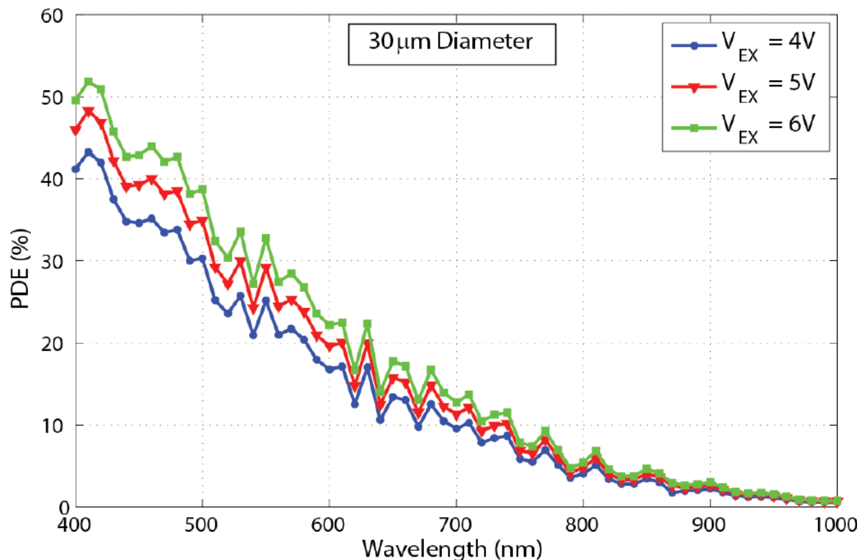
CMOS SPADs: high efficiency





Process: **CMOS 350nm**

Imaging with custom implantation

Area: 700μm^2

Peak PDE: > 50%

DCR: 50 Hz

Timing resolution: 142 ps FWHM

D. Bronzi et al., Proc. IEEE ESSDERC **2012**

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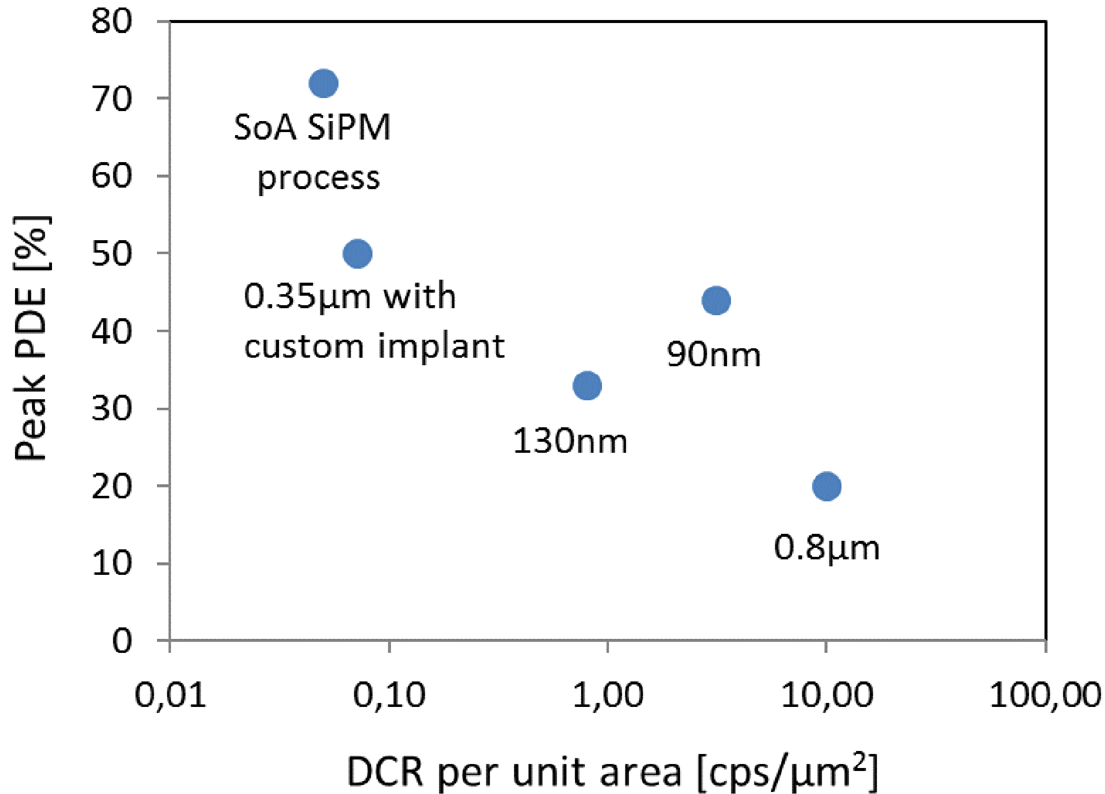
Summary and comparison with SiPM



SiPM:
For major manufacturers
PDE > 70% (single cell, not considering FF)
DCR ~ 50 kHz/mm^2

With customization, CMOS can approach SiPM performance

For a complete overview, see D. Bronzi, et al., IEEE Sensors J. 2016

SPAD array applications

- Time-Of-Flight optical ranging, LIDAR
- Fluorescence spectroscopy
- Raman spectroscopy
- Gamma ray detection (PET)
- Quantum cryptography
- …

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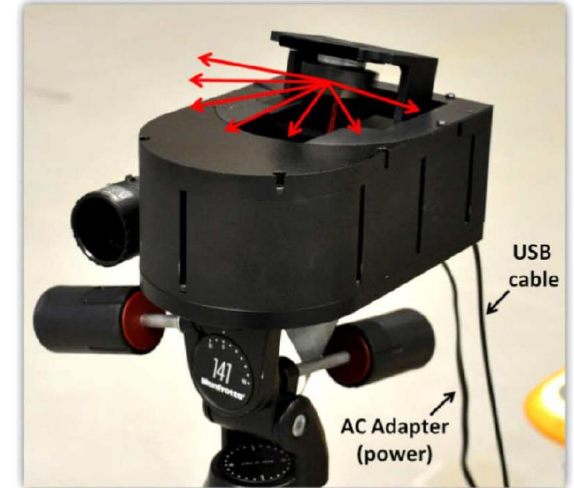
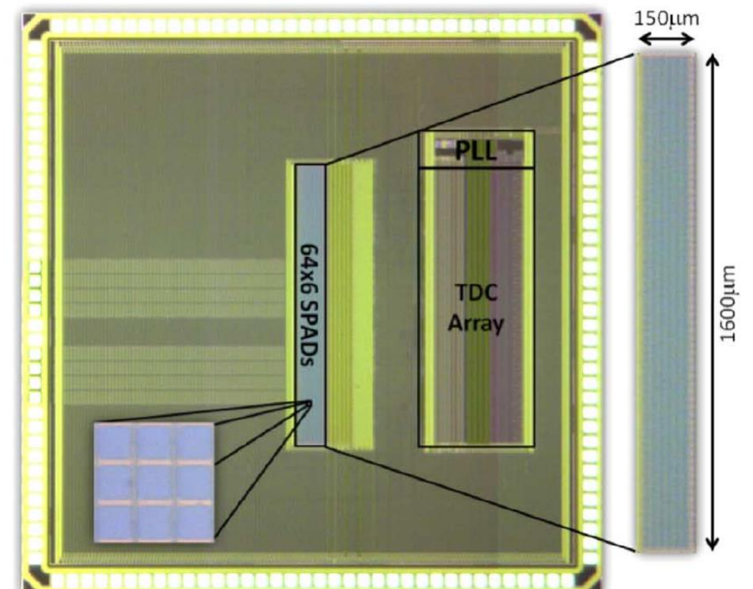
Time-of-Flight optical ranging



Automotive LIDAR developed by Toyota

- 180nm CMOS
- SPAD array with integrated TDCs
- 70% array Fill Factor
- Distance range: 100 m



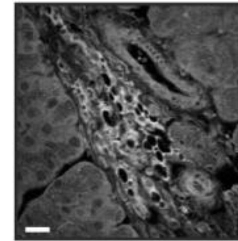
C. Niclass et al., IEEE J. Solid-State Circuits, 2013

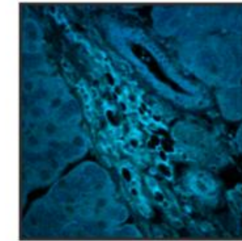
Fluorescence microscopy

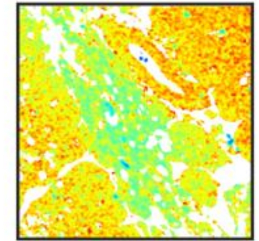
Multi-parametric **fluorescence imaging**

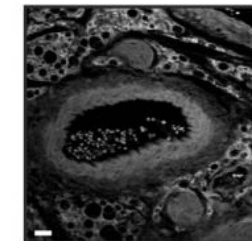
- 350nm CMOS (AMS)
- 4-line SPAD array
- Sub-ns gated counters
- 36% Fill Factor

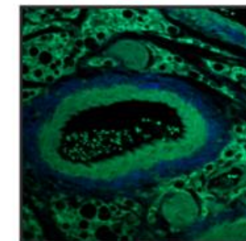
Intensity | Color | Lifetime

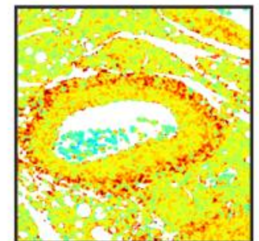


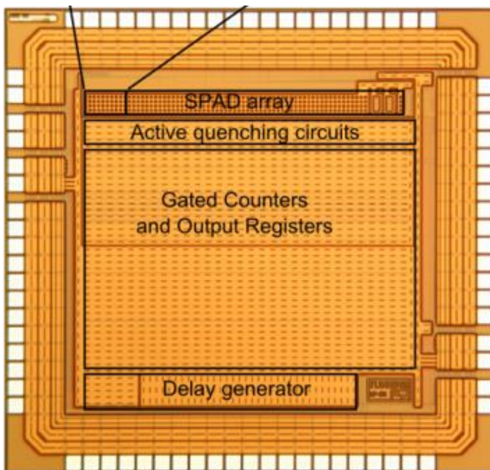












Label-free imaging of unstained liver tissue excised from a tumorogenic murine model

M. Popleteeva et al., Opt. Expr, 2015

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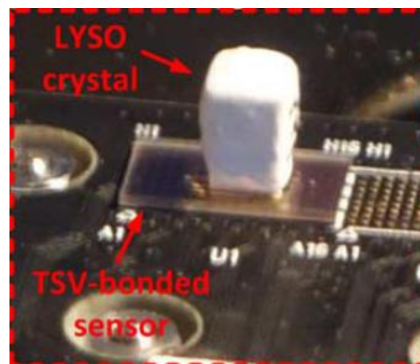
Digital SiPMs for PET

SPADNET project (EU FP7)

- 130nm CMOS process
- Large pixels including 180 SPADs (Mini-SiPM)
- integrated TDCs
- 42.6 % pixel Fill Factor



L. Braga et al., IEEE J. Solid-State Circuits, 2014

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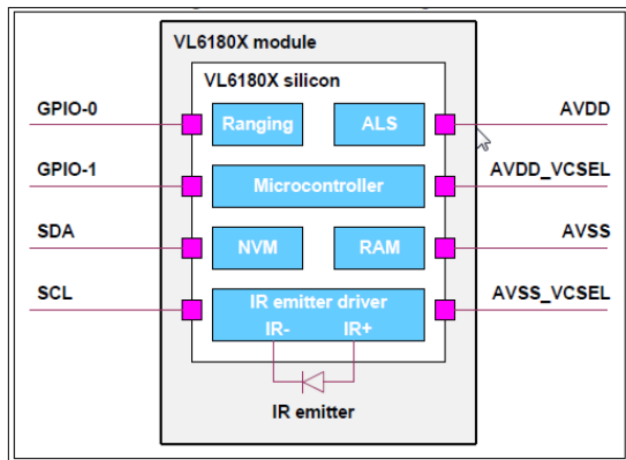
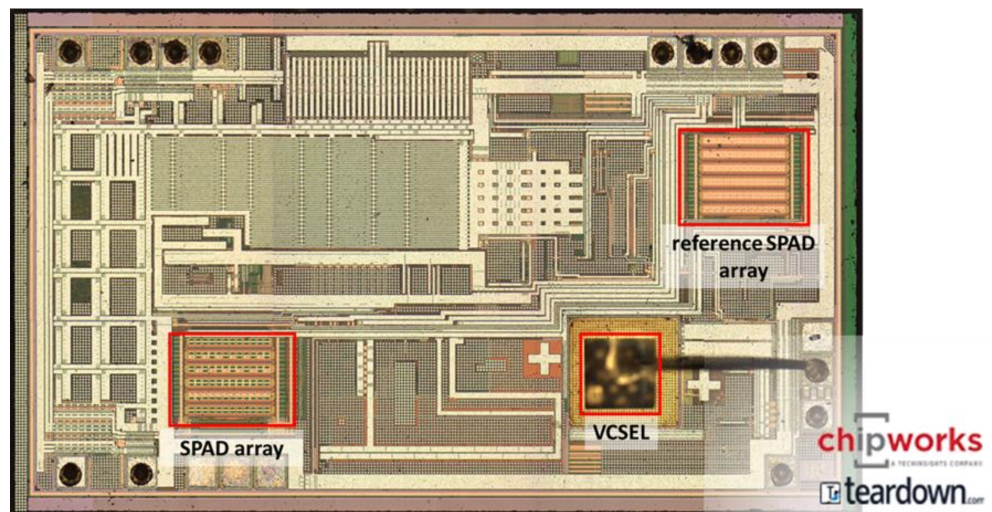
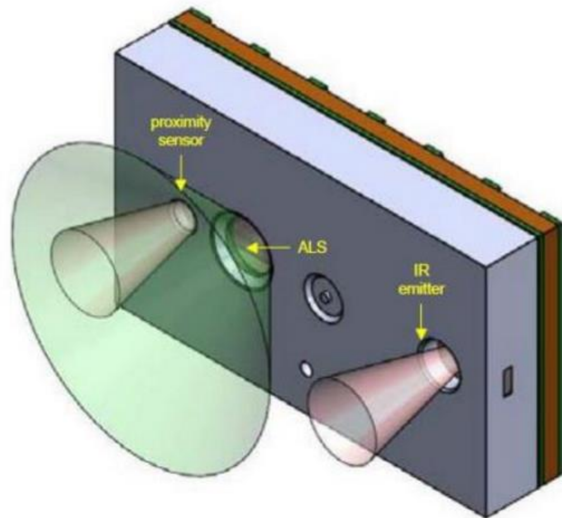
First consumer products: ST ToF sensor

Proximity sensor based on SPAD array and pulsed VCSEL

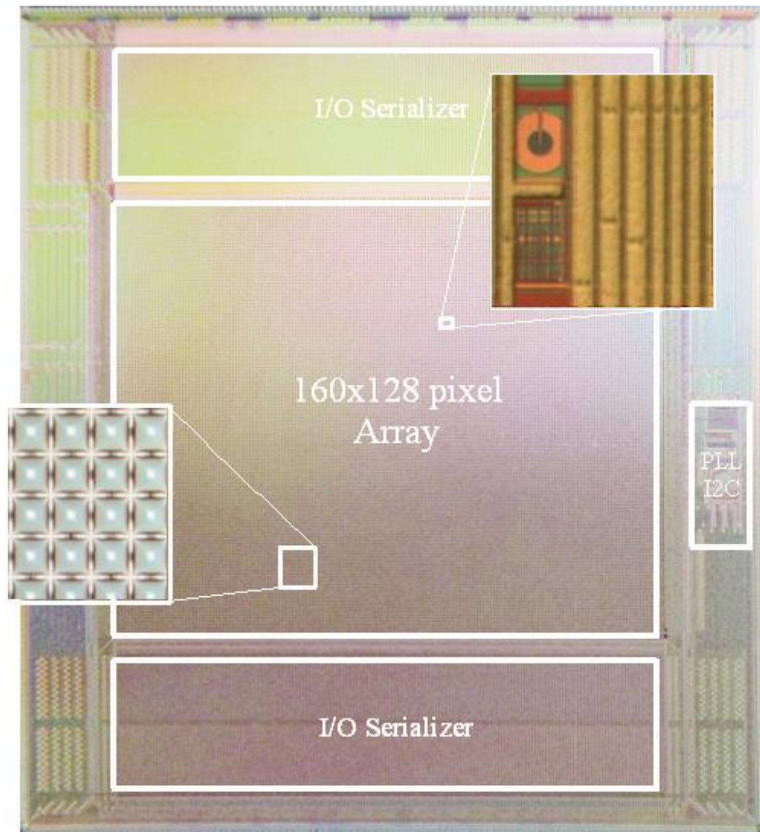






- Presented in **2014**
- Mobile applications (mounted on iPhone7)
- Low power
- Short range (15 cm)

SPAD image sensor



C. Veerappan et al., ISSCC 2011

MegaFrame EU project (FP6)

- 160 x 128 pixel array
- Technology: 130nm CMOS
- In-pixel Time-to-Digital Conv.
- 140ps timing resolution
- **Pixel pitch: 50um**
- **Fill factor: 1%**

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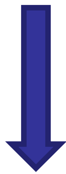
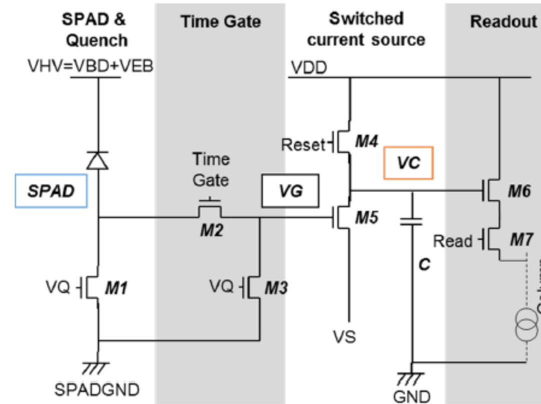
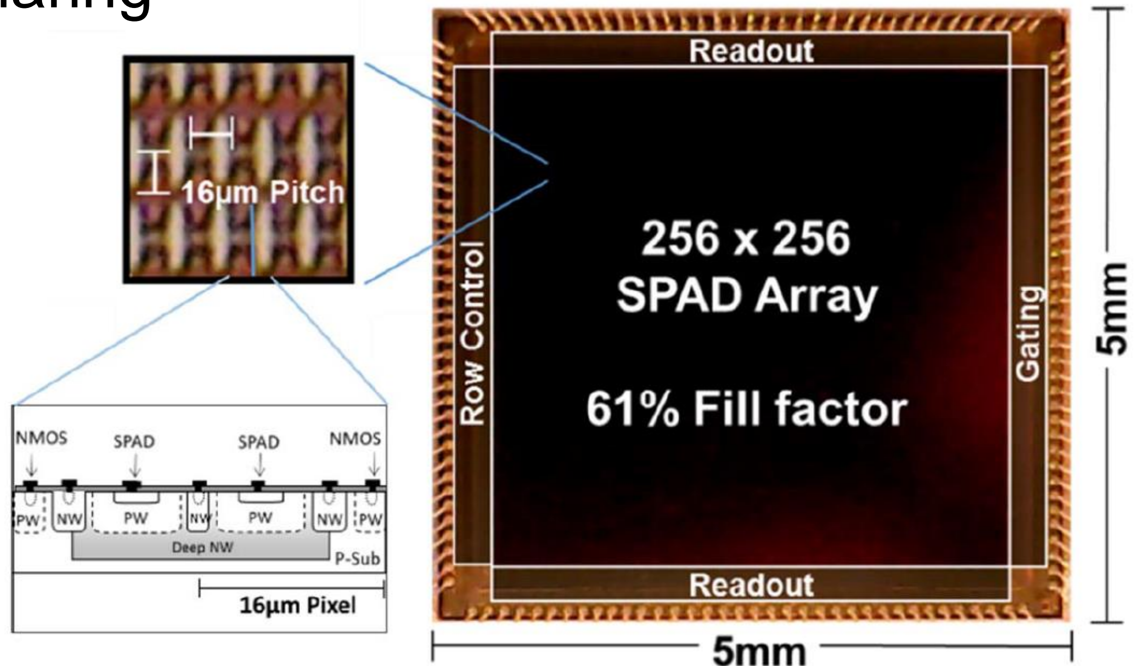
Improving the Fill Factor

- 16µm x 16µm pixel
- 65nm CMOS
- binary pixel
  (7 transistors)
- SPAD deep nwell sharing
- Improved SPAD GR



61% Fill Factor





I. Gyongy et al., IEDM 2016

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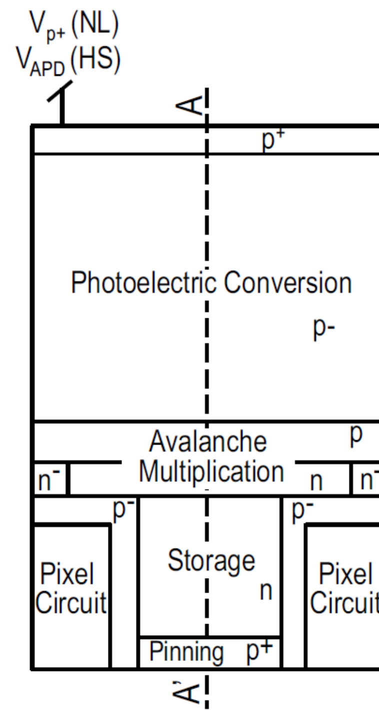
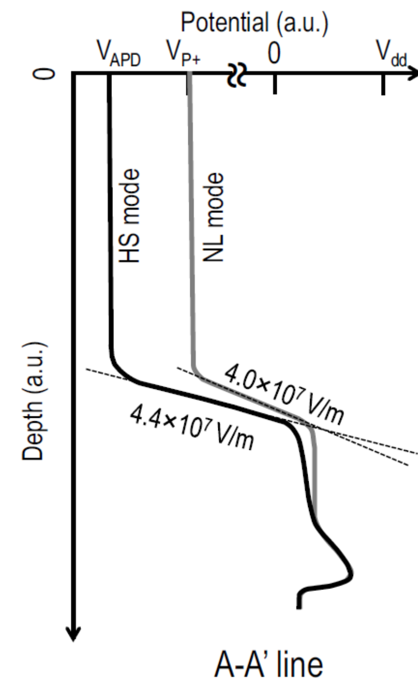
Deep APD

Panasonic project

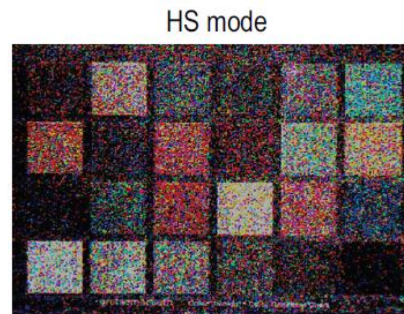
- 110nm CMOS
- Backside illumination
- **Avalanche multiplication region below electronics**
- Pixel pitch 3.8µm
- 4 transistors / pixel
- Linear and binary mode

M. Mori et al., ISSCC 2016

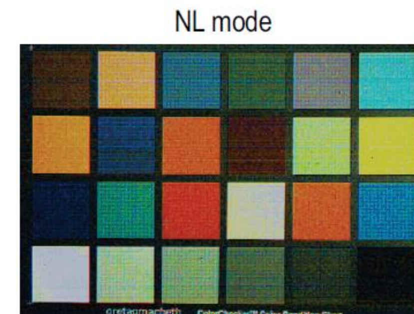




HS mode



NL mode



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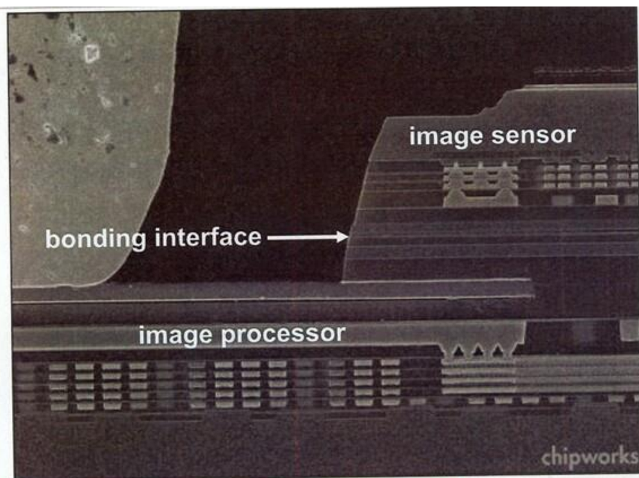
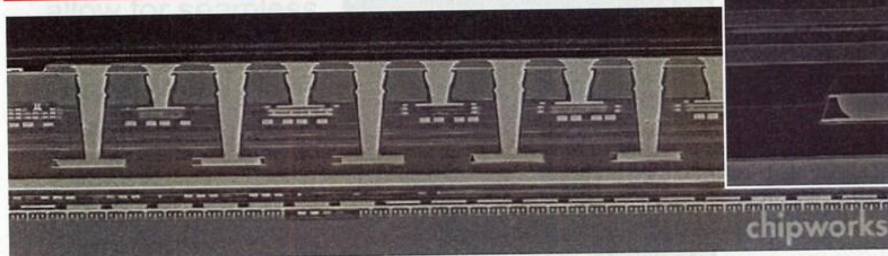
3D integration

High density interconnections successfully demonstrated for image sensors

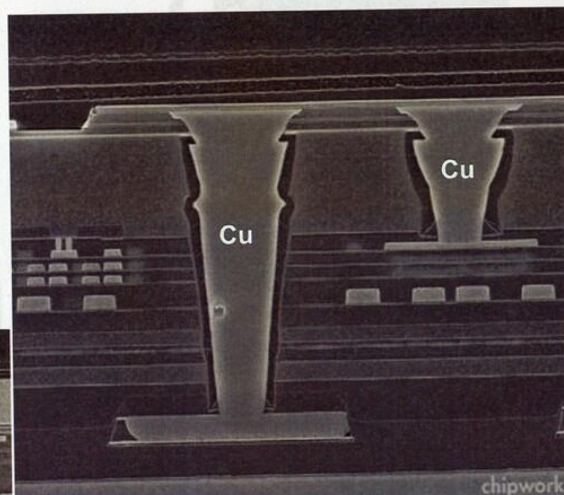


SEM cross-section of stacked dies



SEM cross-section of TSVs

Sony 13 Mpixel stacked image sensor (2013)



electroiq.com

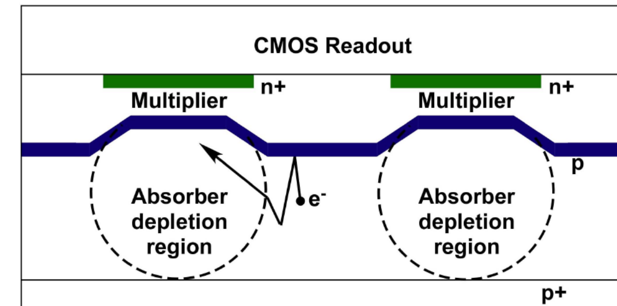
3D-integrated SPAD image sensor 1

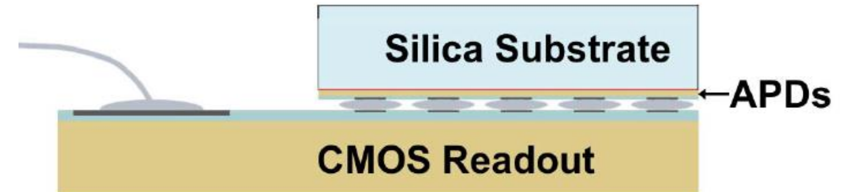
MIT Lincoln Laboratory

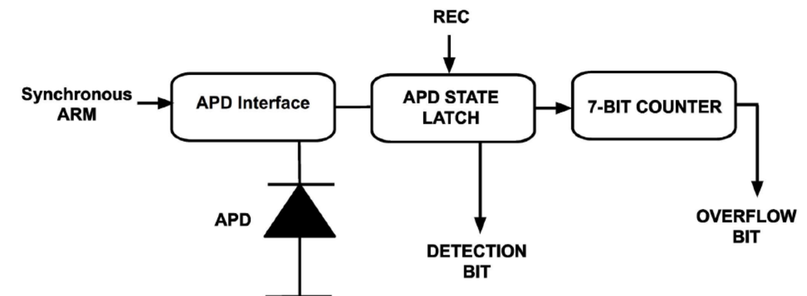
- 25µm pitch
- 180nm CMOS + custom (APDs)
- 7-bit counter/pixel
- Backside illumination

10 - 20% detection efficiency
(limited by optical cross-talk)

B. Aull et al., IEEE Sensors J., 2015







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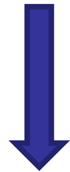
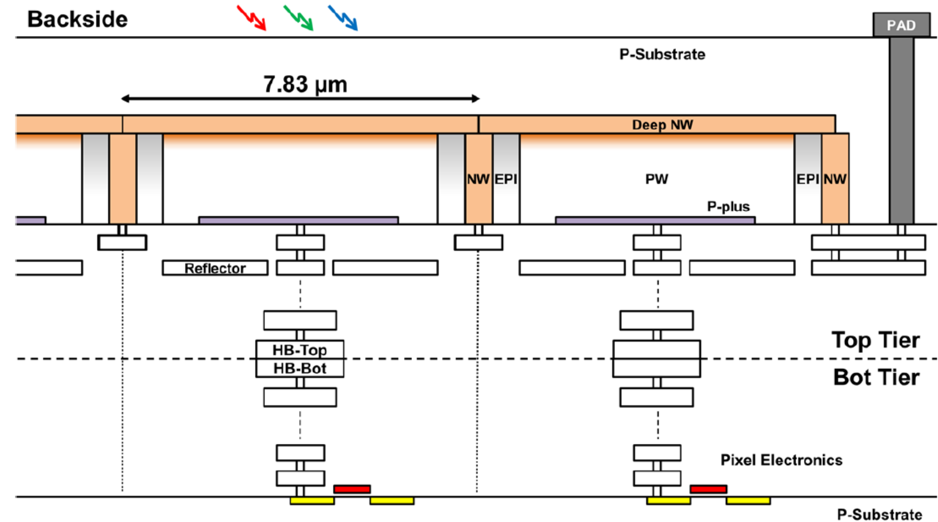
3D-integrated SPAD image sensor 2

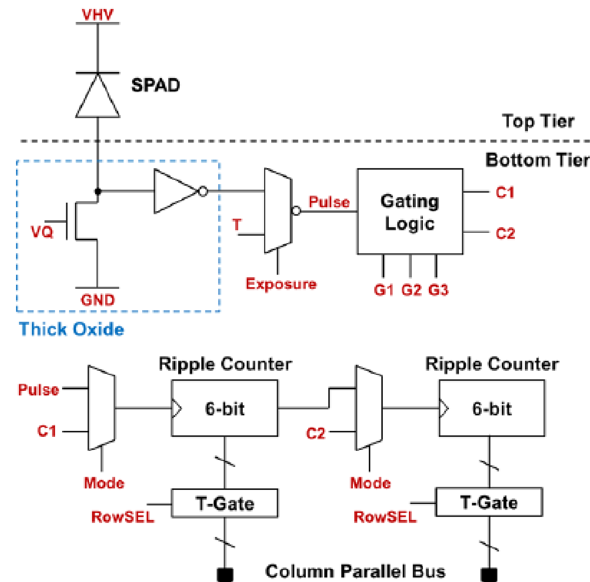
- 7.83μm pitch
- 65nm CMOS (top) + 40nm CMOS (bottom)
- 2 6-bit counters/pixel
- Backside illumination



45% Fill Factor

T. Al Abbas et al., IEDM 2016





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APiX particle detector concept

particle

e h
e h
e h
e h

Avalanche detector

e h
e h
e h
e h

Quenching

Discriminators

Coincidence detector

OUT

Particle detection

Dark counts

- Two Geiger-mode avalanche detectors in **coincidence**:

$$DCR = DCR_1 \times DCR_2 \times 2\Delta T$$

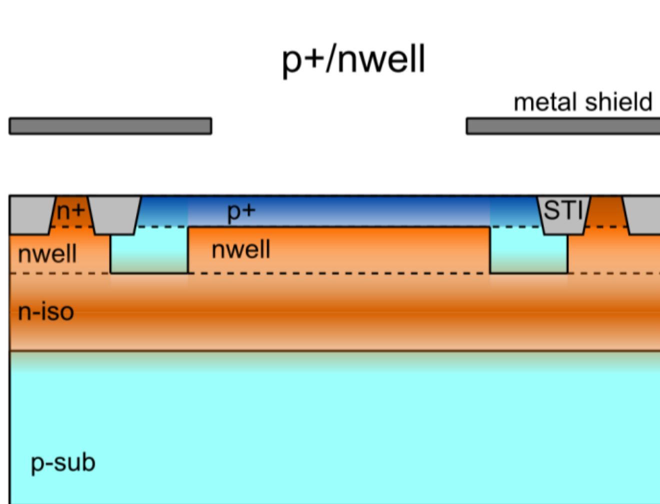
- In-pixel coincidence: integrated electronics is needed: **CMOS avalanche detectors**

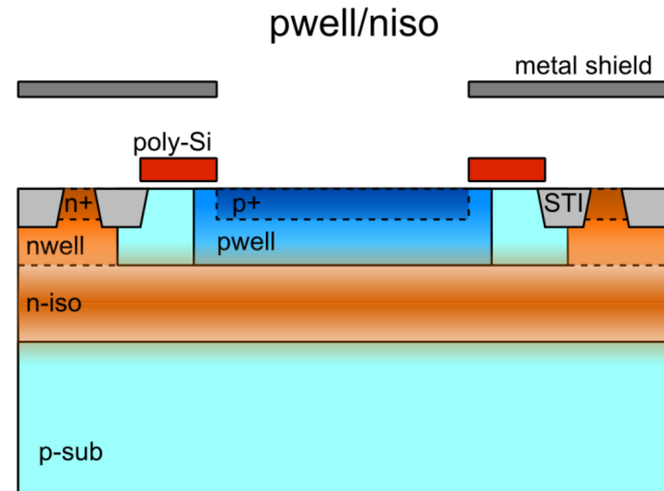
V. Saveliev, US Patent. 8,269,181, 2012

N. D'Ascenzo et al., JINST 2014

SPADs in 150nm CMOS process

- **Standard CMOS** process – no modifications
- Avalanche diodes in deep nwell: **isolated from substrate**





Type 1:

- Shallow step junction
- Active thickness ~ 1μm

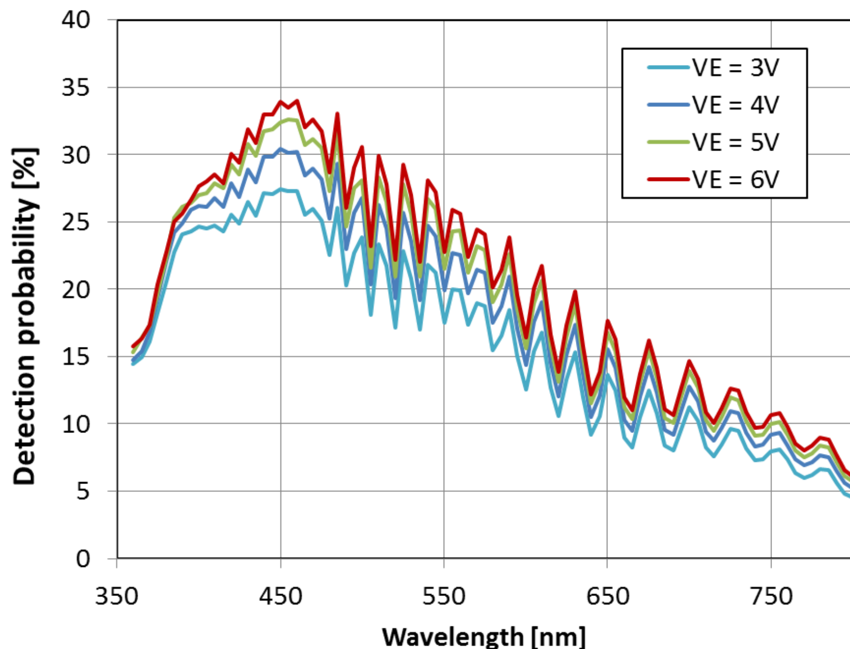
Type2:

- Deep graded junction
- Active thickness ~ 1.5μm

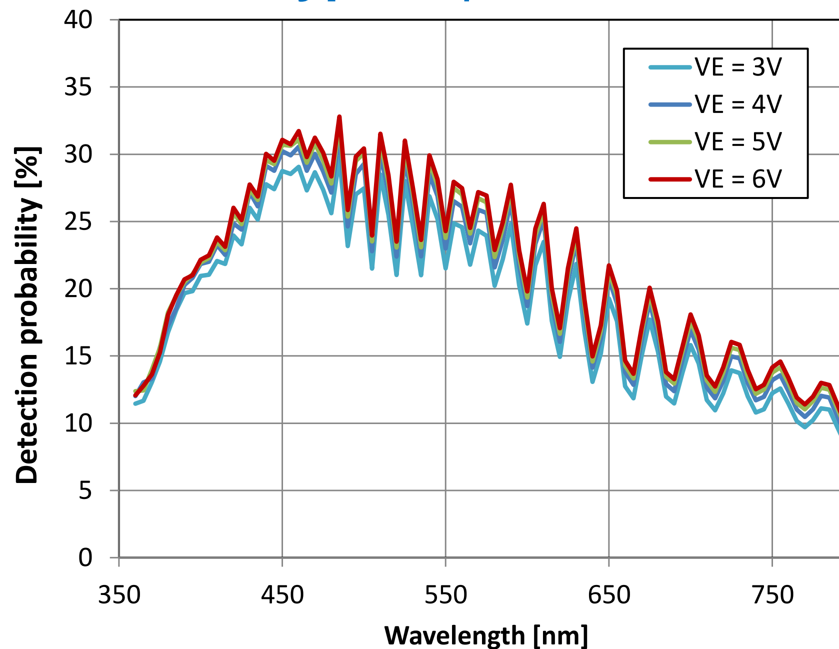
L. Pancheri, D. Stoppa, ESSDERC 2011

Photo-Detection Efficiency

Type 1: p+/nwell



Type 2: pwell/niso



Shallower junction:
better NUV – Blue efficiency

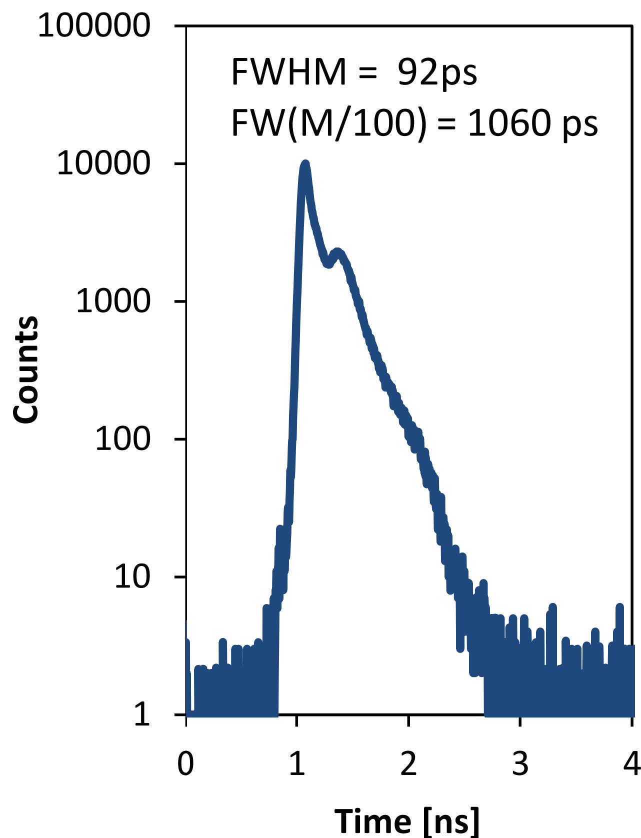
Wider depletion region:
Better red-IR efficiency

L. Pancheri et al., J. Selected Topics in Quantum Electron, 2015

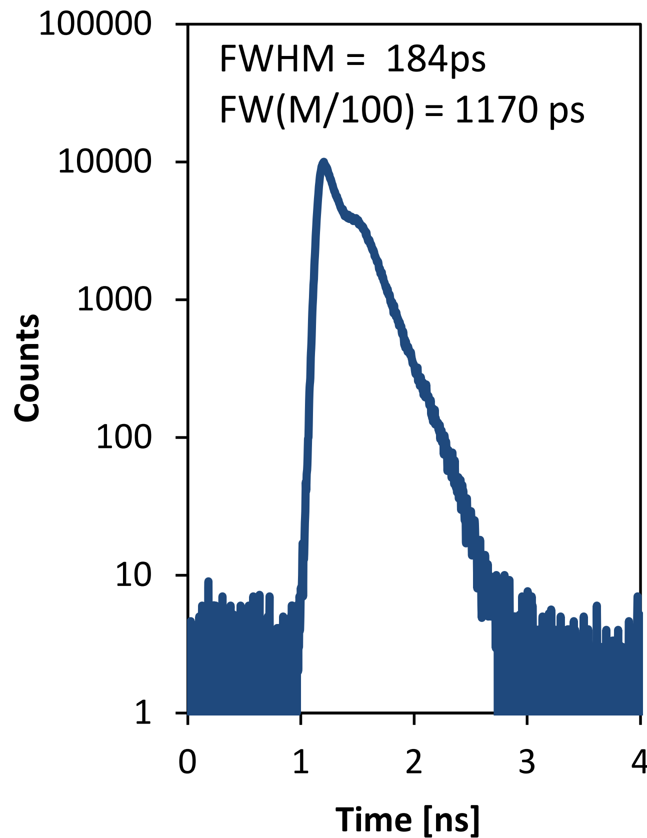
Single-photon timing resolution

Measured on 10-μm devices, with blue laser (470nm), 70ps FWHM

Type 1: **60ps FWHM**



Type 2: **170ps FWHM**



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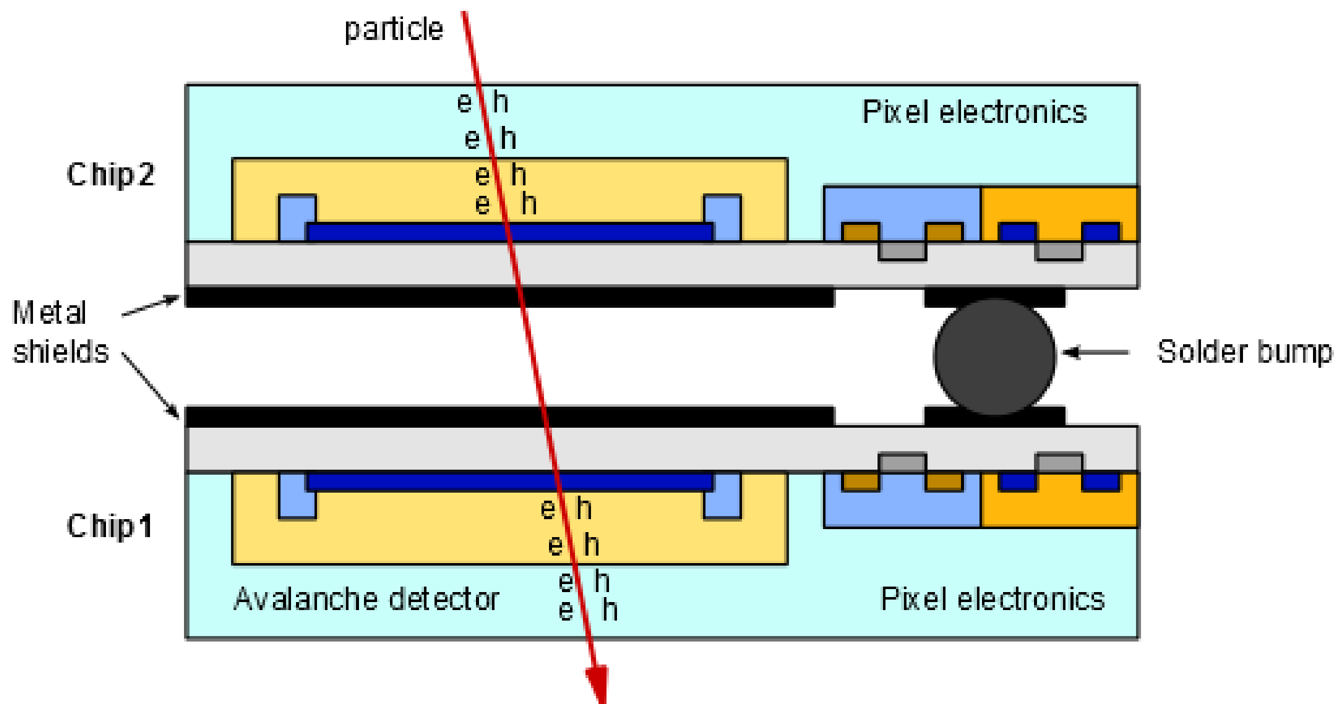
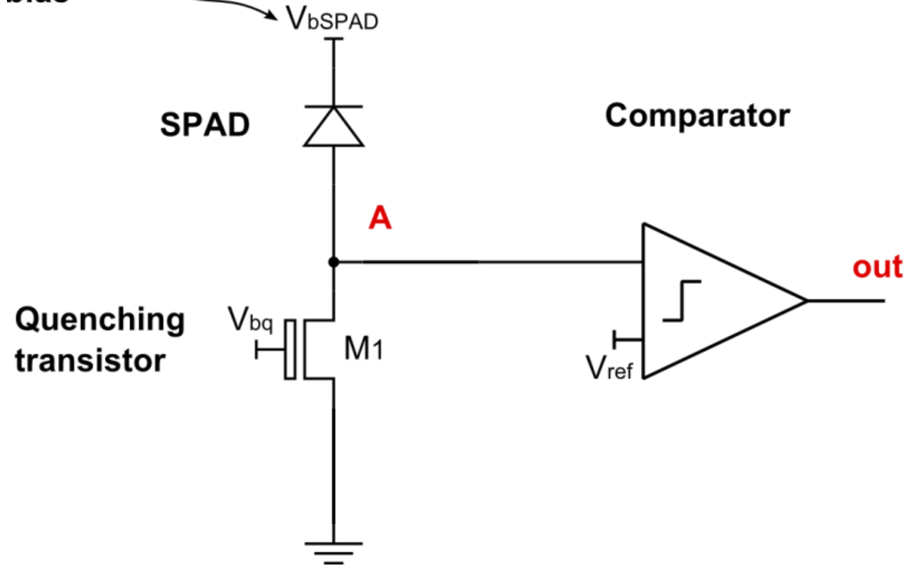
Proof-of-concept demonstrator

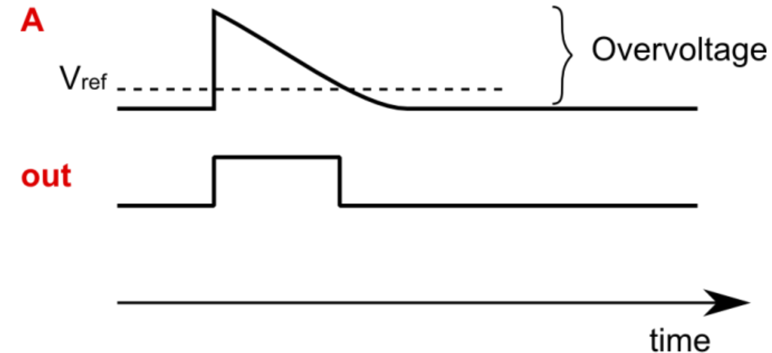


2-layer pixel cross section:

- Electronic readout on both layers
- **Metal shielding** from optical cross-talk
- Vertical interconnection by **bump bonding**

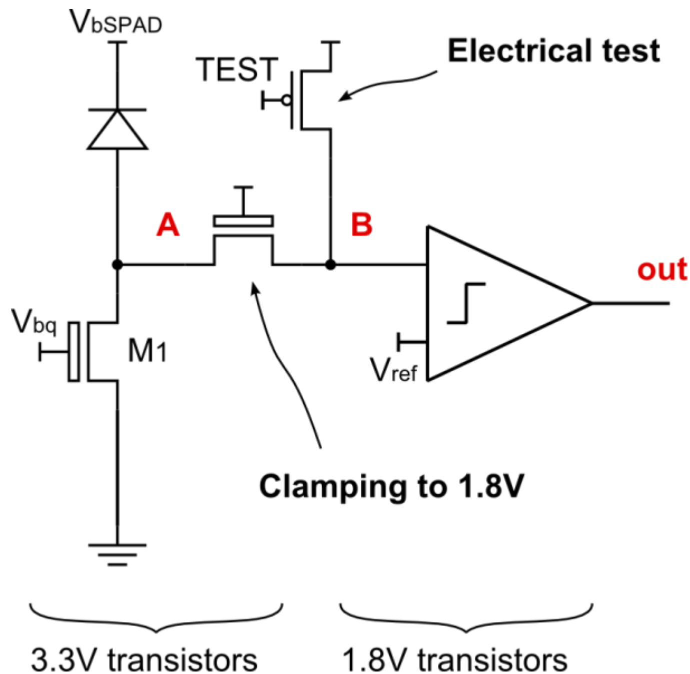
Pixel architecture

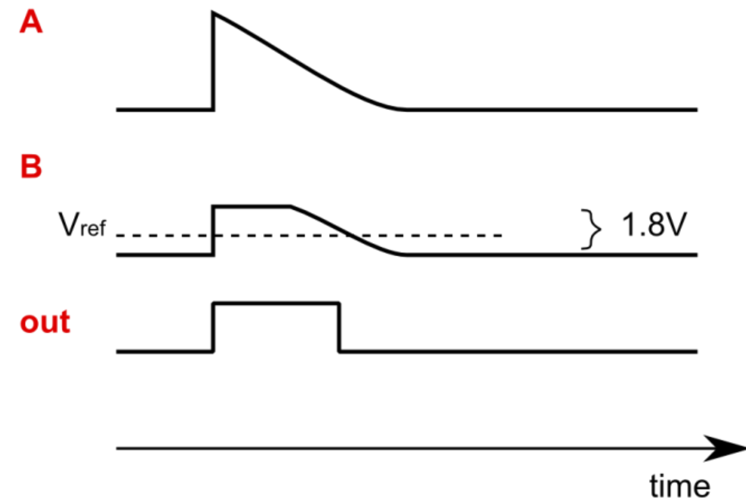




- **High voltage** V_{bSPAD} applied at nwell
- Maximum voltage at node A: $V_{ov} = V_{bSPAD} - V_{BD}$
- **Small capacitance** at node A
- Passive quenching with constant current recharge

Pixel architecture





- Front-end transistors: 3.3V → Maximum overvoltage 3.3V
- **Digital circuitry: 1.8V** compact – fast – low-power

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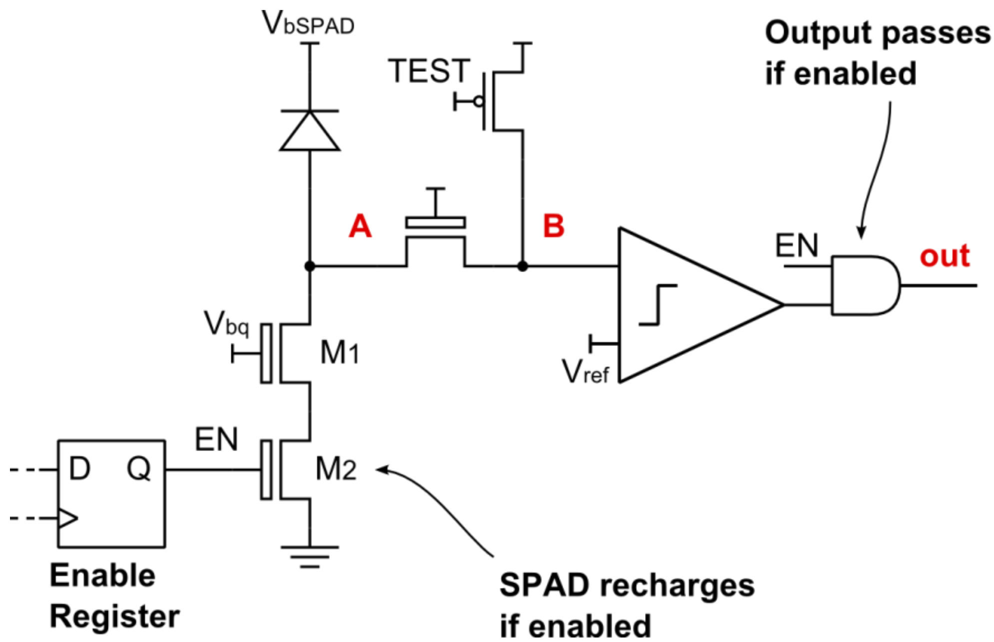
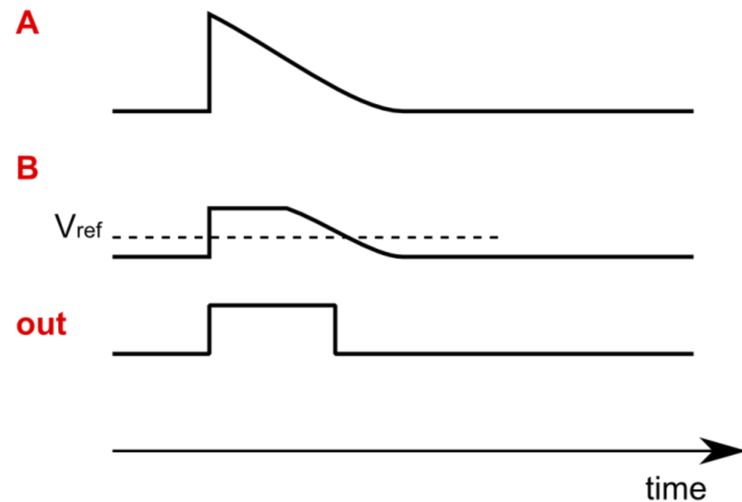
Pixel architecture: enable register





Pixels can be **individually disabled**:

- M_2 disables recharge
- Output and gate blocks output pulses

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Pixel architecture: coincidence

Vertical interconnection to top pixel

Coincidence detection

- Coincidence with top-layer pixel

Pixel architecture: coincidence

VbSPAD

TEST

A

B

Vbq

M1

EN

D Q

M2

Vref

EN

out1

out2

out

Vertical interconnection to top pixel

Coincidence detection

out1

out2

out

time

Real coincidence

Accidental coincidence

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Pixel architecture: monostable

VbSPAD
TEST
A
B
Monostable for pulse shortening
PROG
Vertical interconnection to top pixel
out2
out1
out
EN
V_{bq}
M1
V_{ref}
EN
D Q
M2
Coincidence detection
out1
out2
out
time

- Pulse shortening: reduces the rate of accidental coincidence
- Programmable pulse width: **750ps, 1.5ns, 10ns**

Pixel architecture: storage

VbSPAD
TEST
A
B
PROG
EN
out1
out2
out
1 bit Memory
HI
D Q
MRES
Vbq
M1
Vref
EN
D Q
M2
TX
D Q
CK
RES
Output Register

- **Global shutter** operation:
  - Fast transfer from memory to output register
  - Simultaneous accumulation and data output

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2-level pixel schematic

Top pixel: subset of bottom pixel

Pixel in chip 2 (top)

Detector + front end

Pulse shrinking

EN

D Q

Enable register

Vertical interconnection

Pixel in chip 1 (bottom)

Detector + front end

Pulse shrinking

Coincidence detector

EN

D Q

Enable register

HI

D Q

1-bit Memory

TX

D Q

Out

Output register

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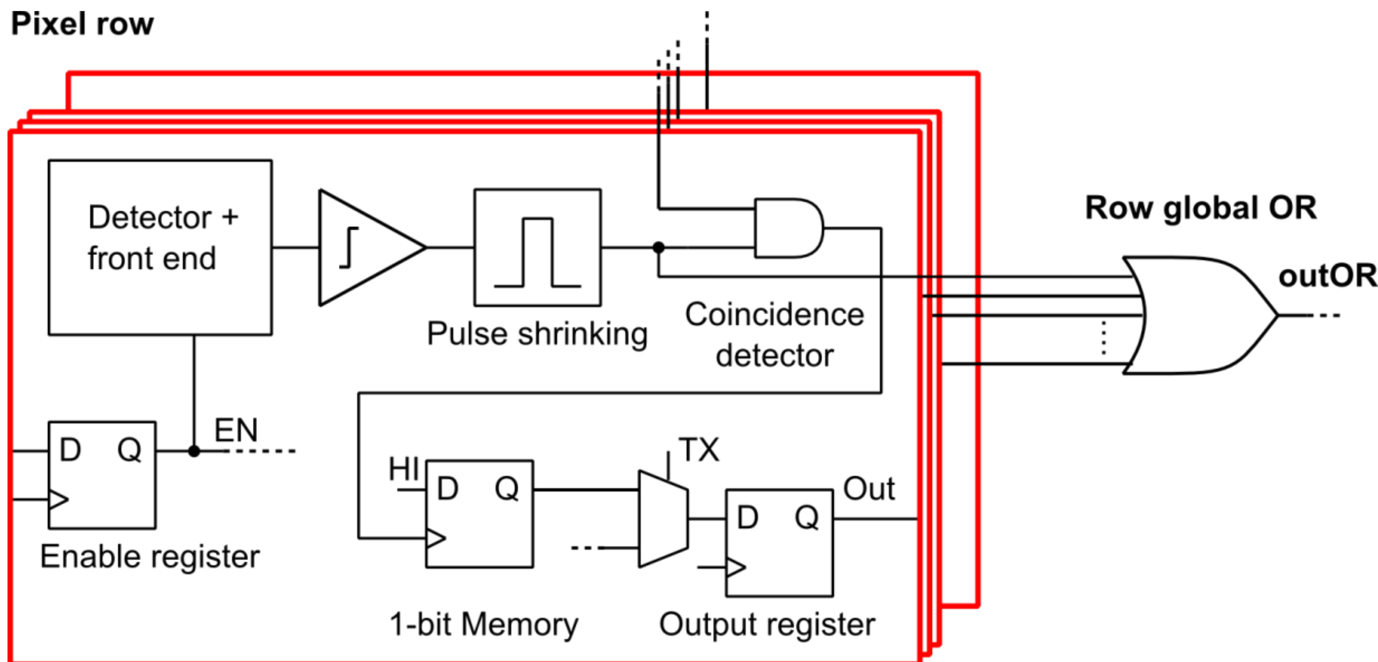
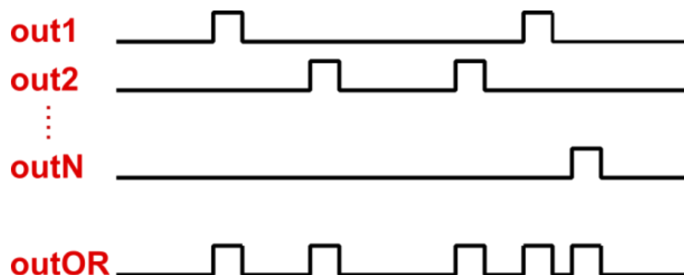
Sensor architecture: row-wise OR



Test output outOR: combination of all the active (enabled) pixels in the row



Row-wise coincidence circuit

Pixel row m

Detector + front end
Pulse shrinking
Coincidence detector
EN
D Q
Enable register
HI
D Q
TX
Out
D Q
1-bit Memory
Output register

outOR n

Row coincidence detector

outCOINC

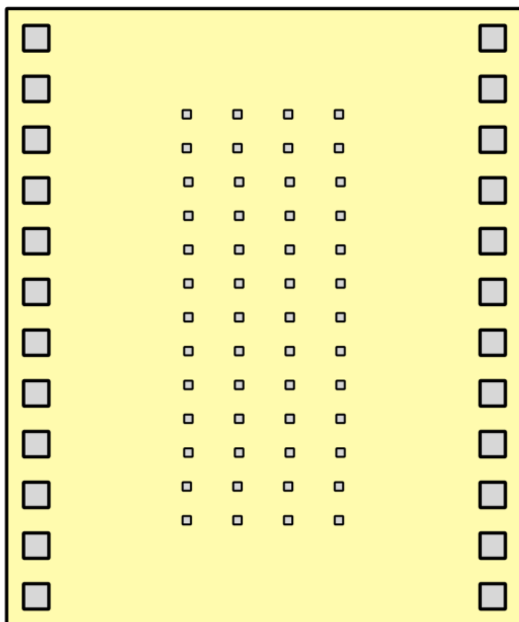
Pixel row n

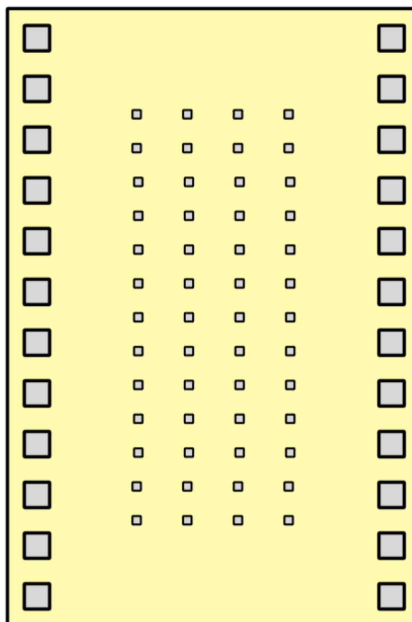
Detector + front end
Pulse shrinking
Coincidence detector
EN
D Q
Enable register
HI
D Q
TX
Out
D Q
1-bit Memory
Output register

outOR m

- Test coincidence in the sensor plane
- m and n can be arbitrarily selected

Sensor floorplan

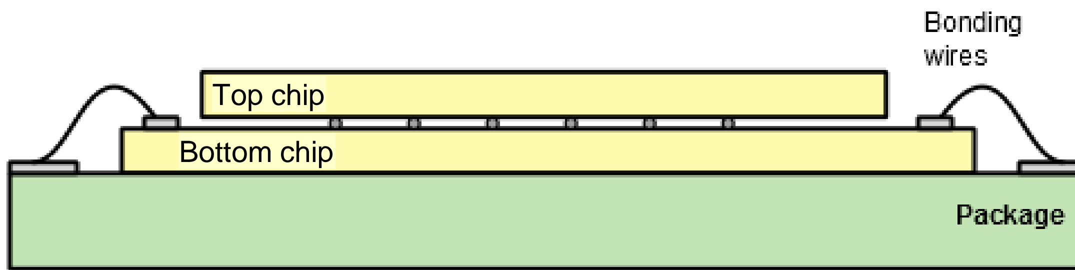




Pads for wire bonding

Pads for bump bonding

Wire bonding pads on chip 2: pre-integration test.



Final assembly

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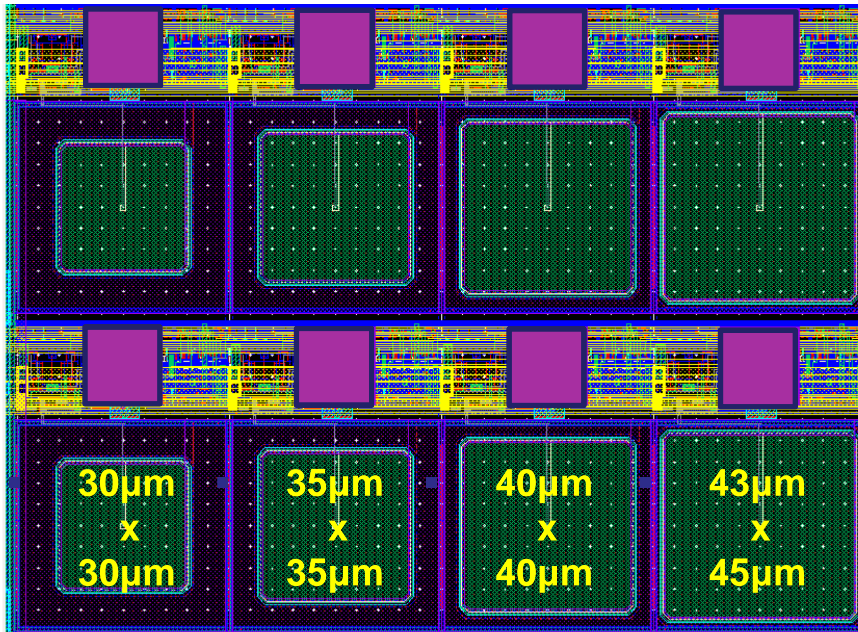
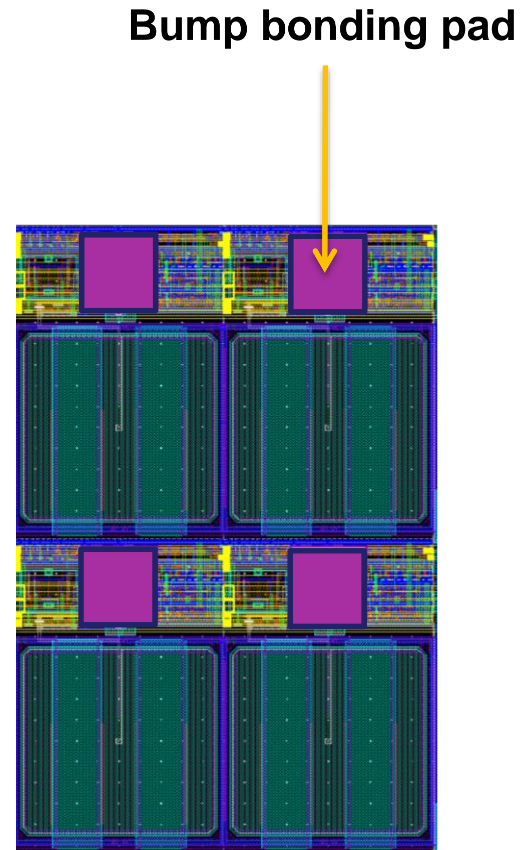
Pixel array

- 16 x 48 pixel array
- Pixel size: 50μm x 75μm
- Splittings in detector type and area



Pixels with different detector area (unshielded)



Pixels with shielded detectors

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Bottom chip - Micrographs

Shielded

Unshielded

APiXC1 - LP

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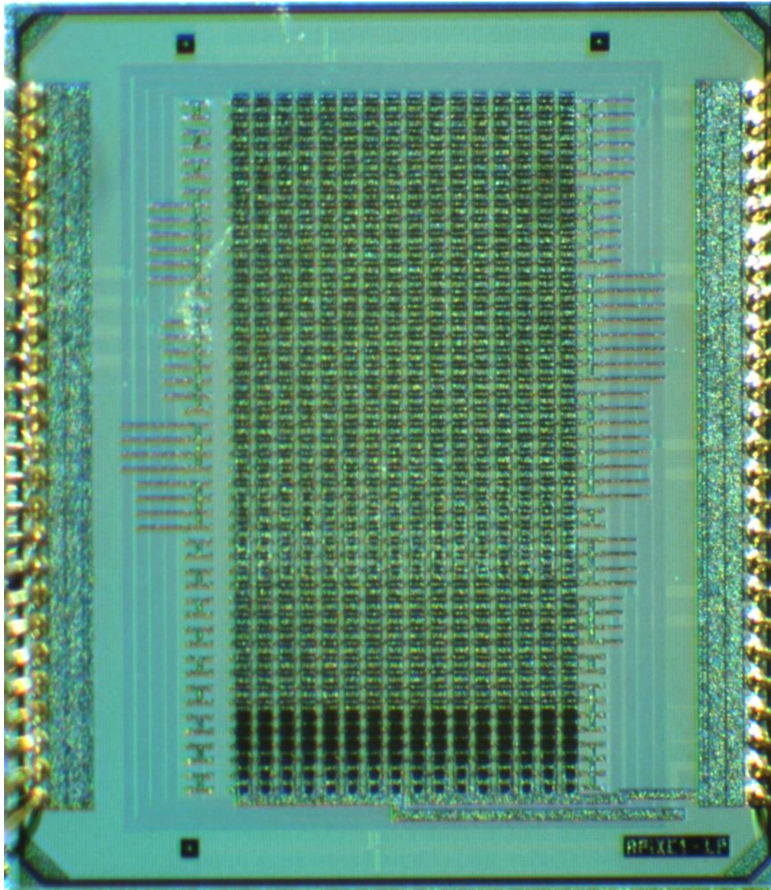
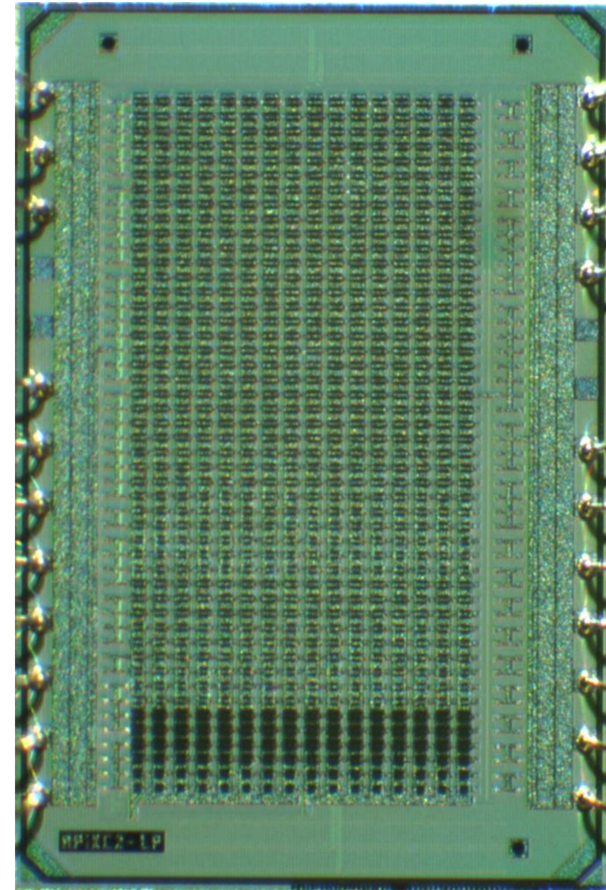
Sensor micrographs

Bottom chip



Top chip



Experimental results - summary

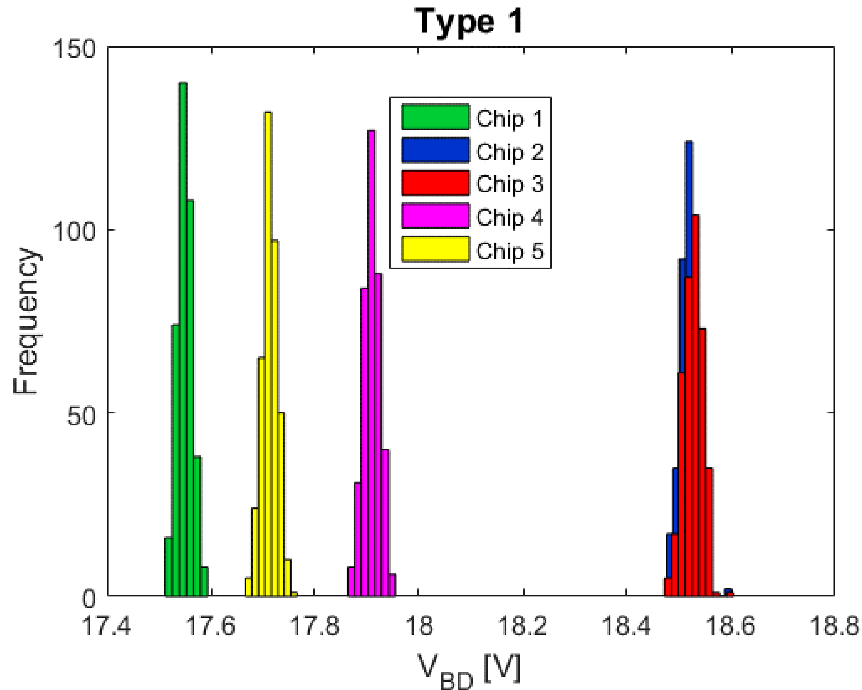
Characterization of **single-layer sensors**:

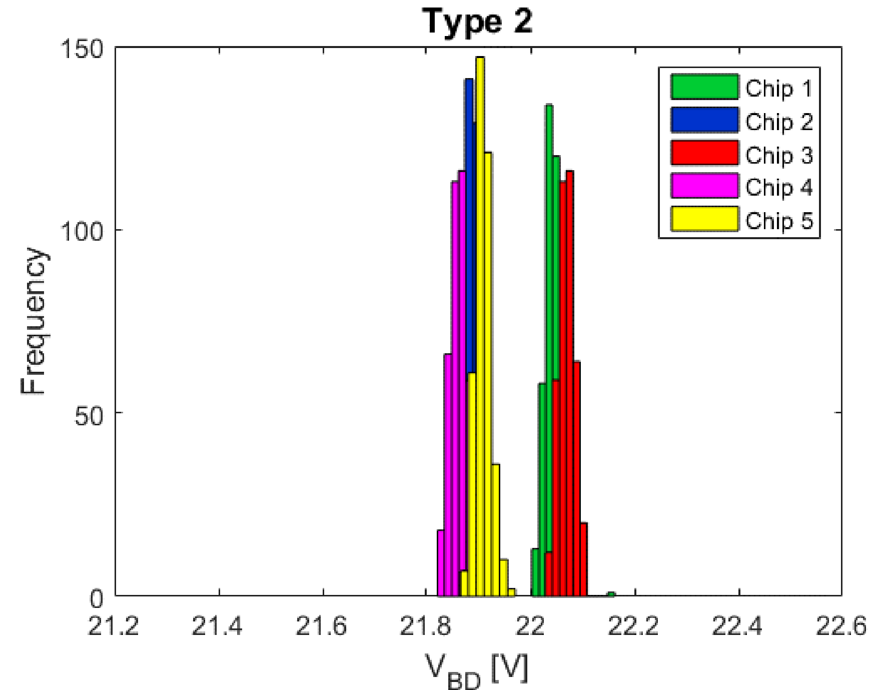
- **Core supply current (at 1.8V): 8mA**
- Breakdown voltage uniformity
- Dark count rate
- In-plane coincidence
- Timing resolution
- Cross-talk

Vertically integrated sensors with bump bonding (IZM):

- Coincidence dark counts
- Test with beta source
- Test beam

Breakdown voltage uniformity





- Measurements on
  5 sample chips x 2 types x 196 devices per chip
- Very good uniformity on-chip (**σ < 20mV**)
- Large difference (1V) between different chips for type 1

DCR distribution

Active area: 43μm x 45μm

Dark count rate [Hz]

10^6, 10^4, 10^2, 10^0

0, 20, 40, 60, 80, 100

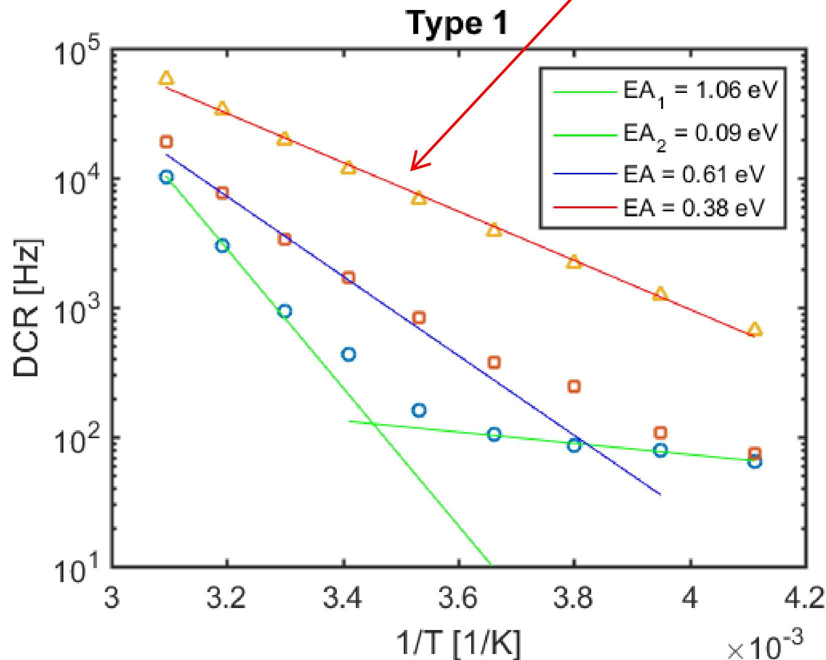
% devices

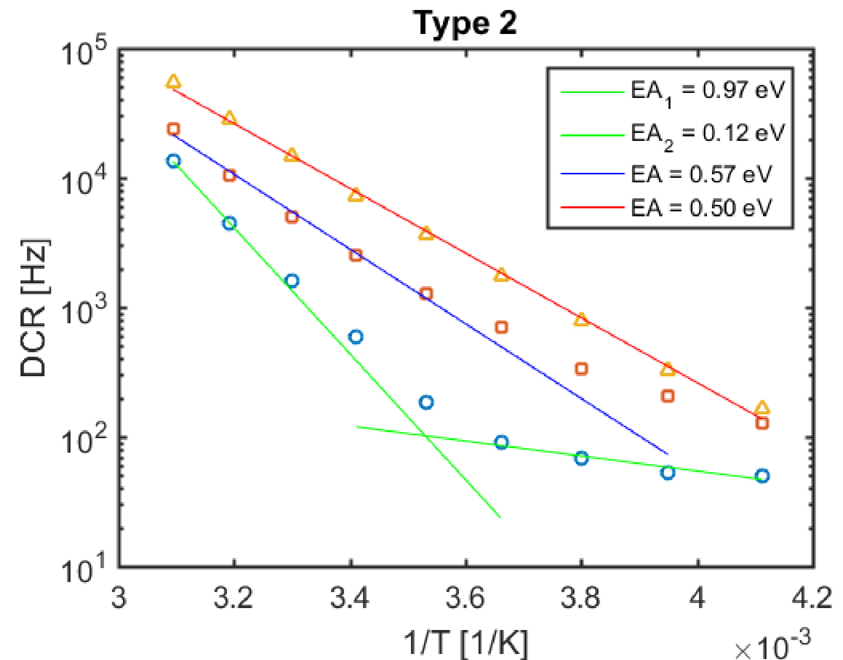
-30°, -20°, -10°, 0°, 10°, 20°, 30°, 40°, 50°

- DCR distribution spans 2 orders of magnitude at RT
- Median value at 20°C: 2.8kHz - MHz/mm^2

DCR temperature dependence

Trap-assisted tunneling: $E_A < E_G/2$





- Devices with 43μm x 45μm active area, but different DCR
- Measurements from **-30°C to 50°C** with 10°C steps
- Overvoltage: V_{OV} = 3.3V

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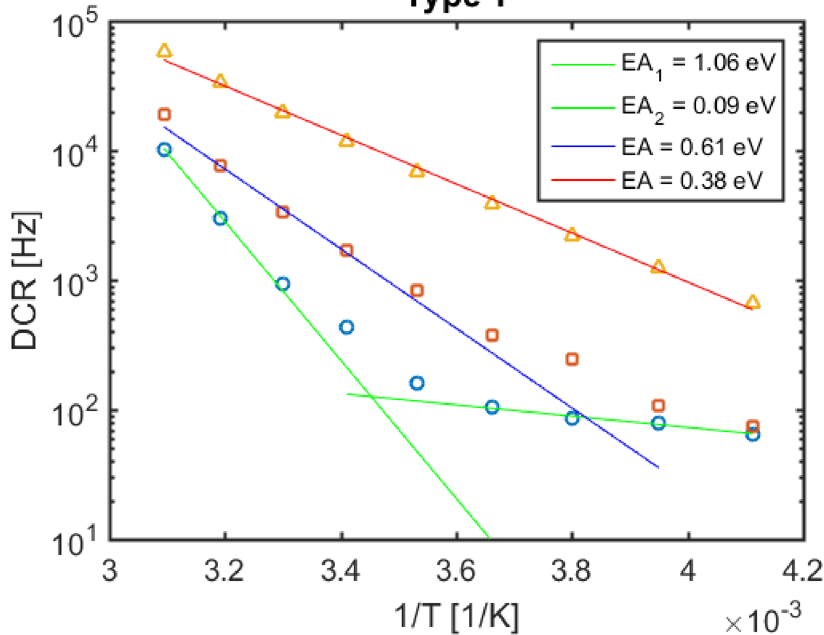
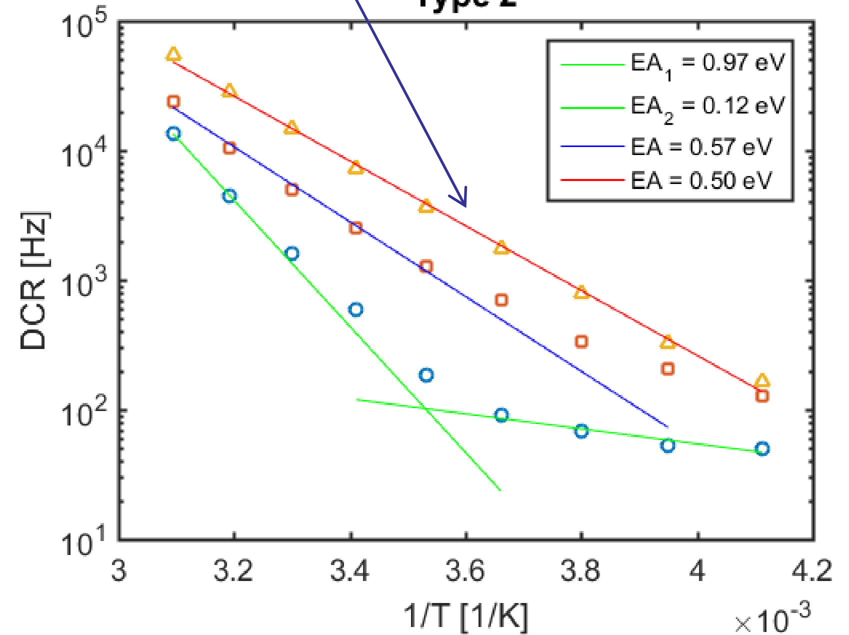
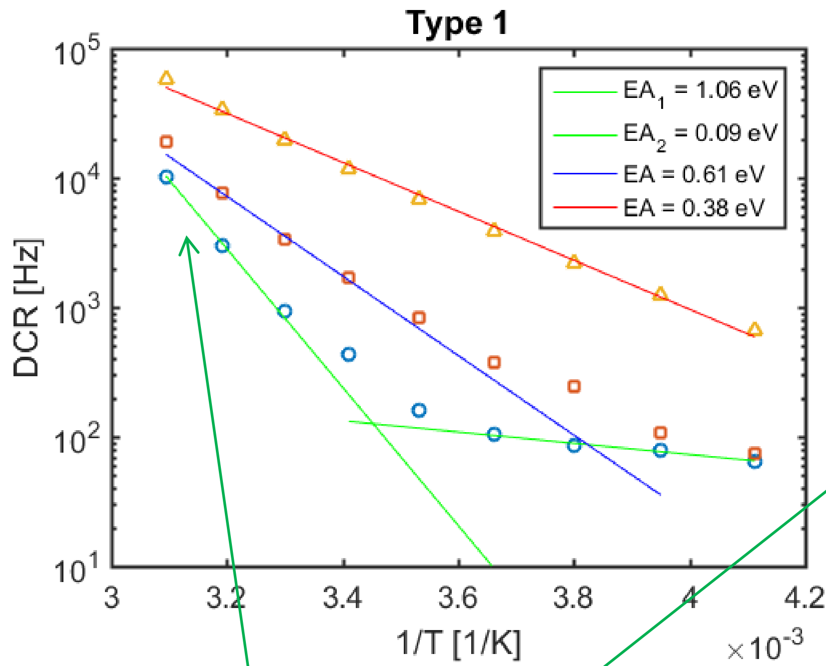
DCR temperature dependence

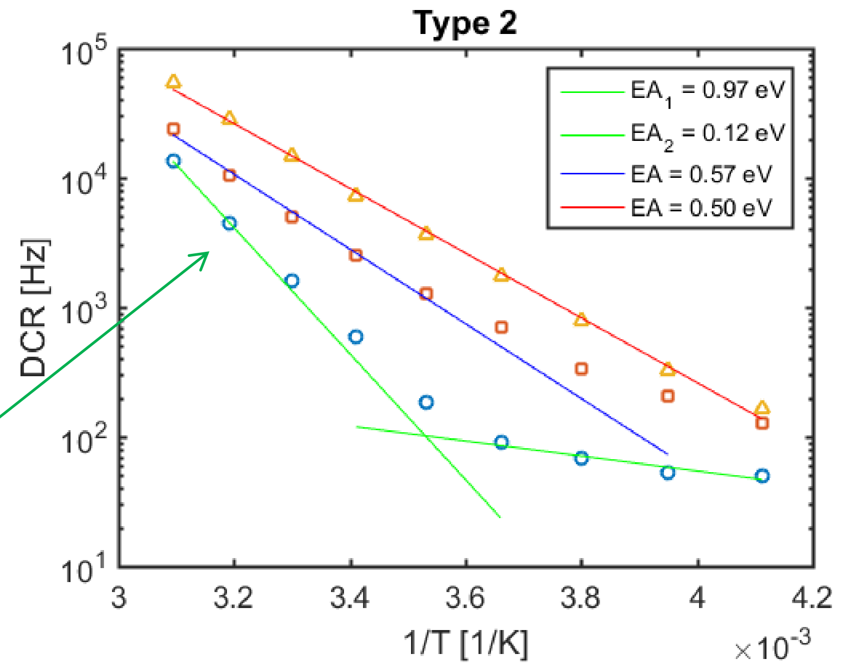
SRH generation $E_A \sim E_G/2$





DCR temperature dependence





Injection from neutral regions: $E_A \sim E_G$

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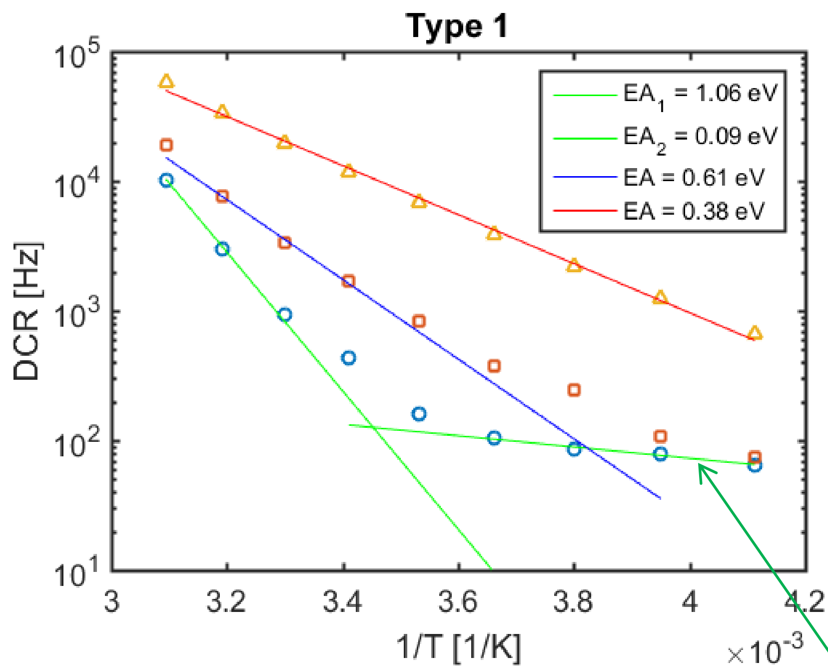
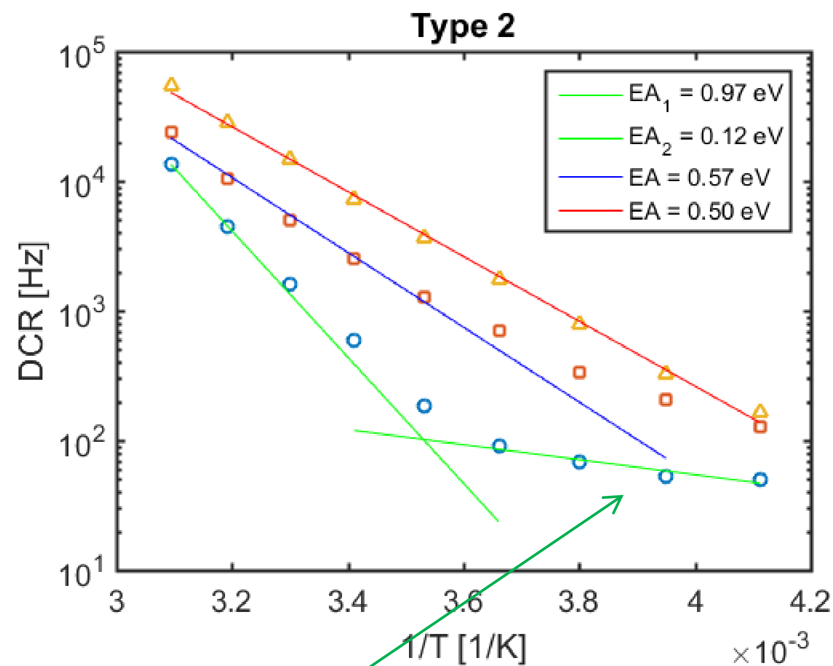
DCR temperature dependence





Band – to – band tunneling: $E_A \rightarrow 0$

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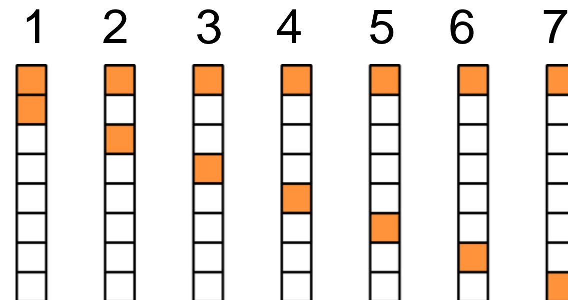
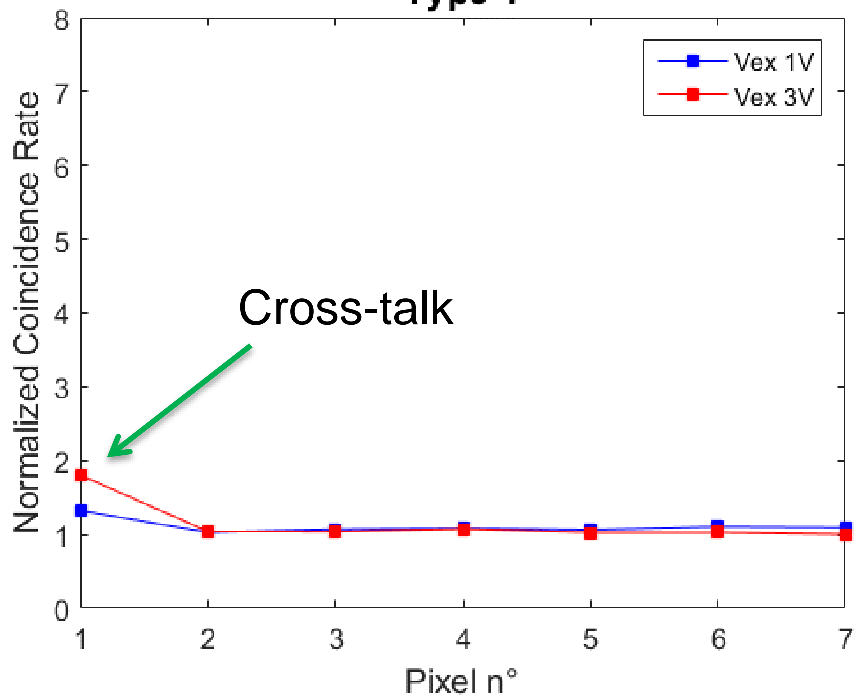
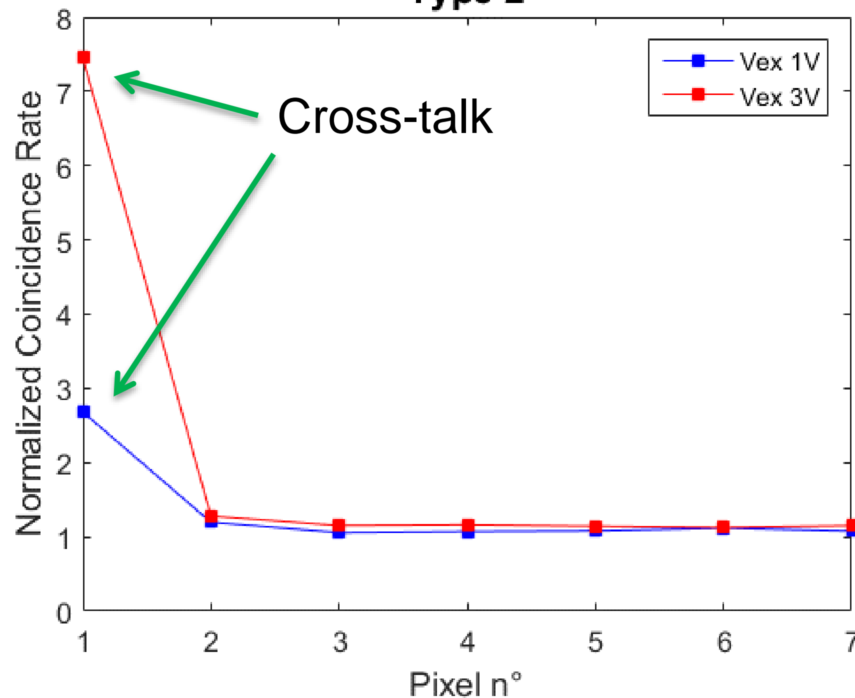
Coincidence detection

Count rate in coincidence between two pixels in the same column

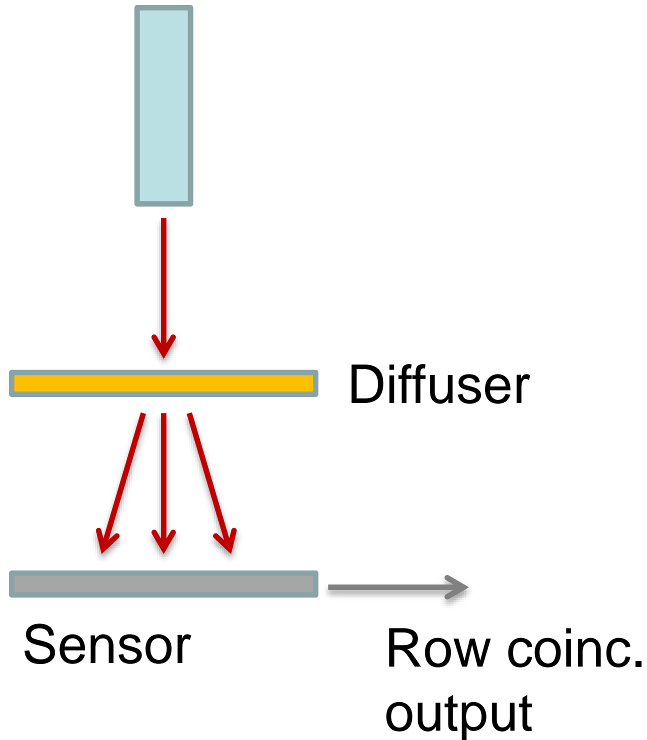
Normalized rate: $$\frac{CR_{Meas}}{2 \cdot CR_1 \cdot CR_2 \cdot \Delta T}$$

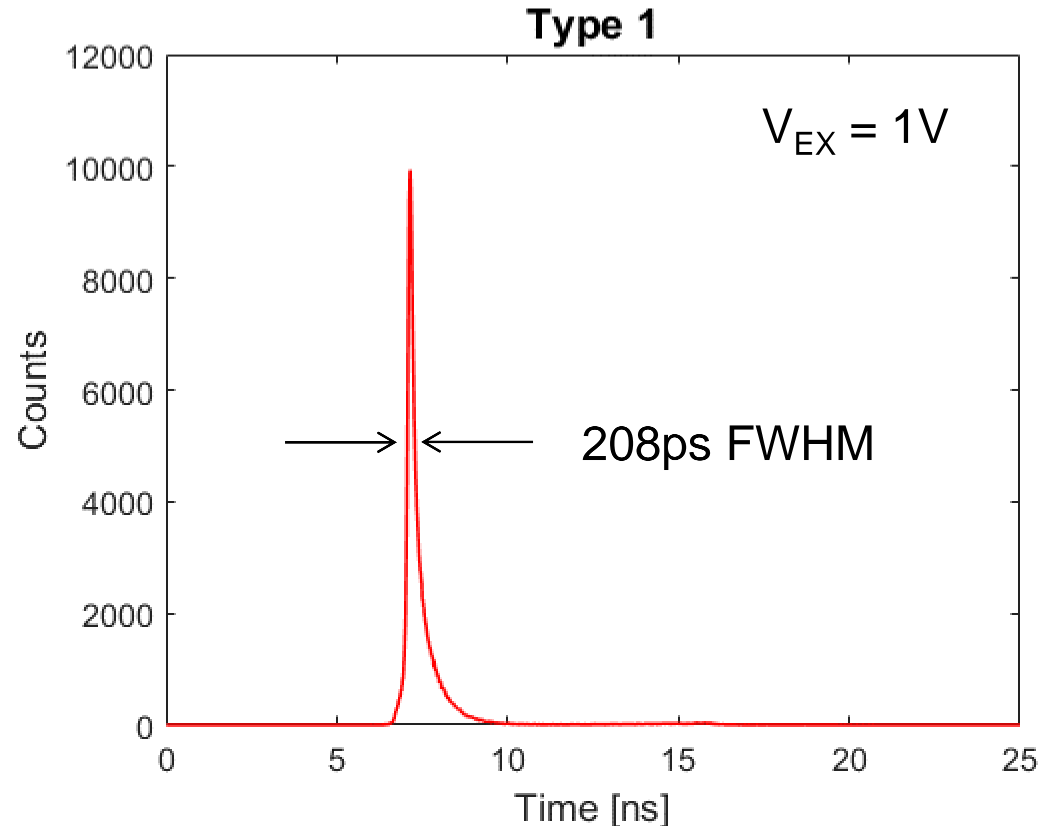






Timing resolution



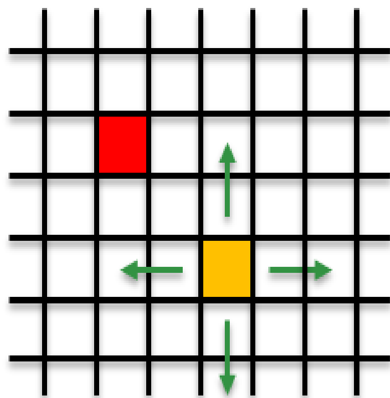


Timing histogram between laser trigger and sensor coincidence output

2 pixels enabled

N.B. Design not optimized for timing

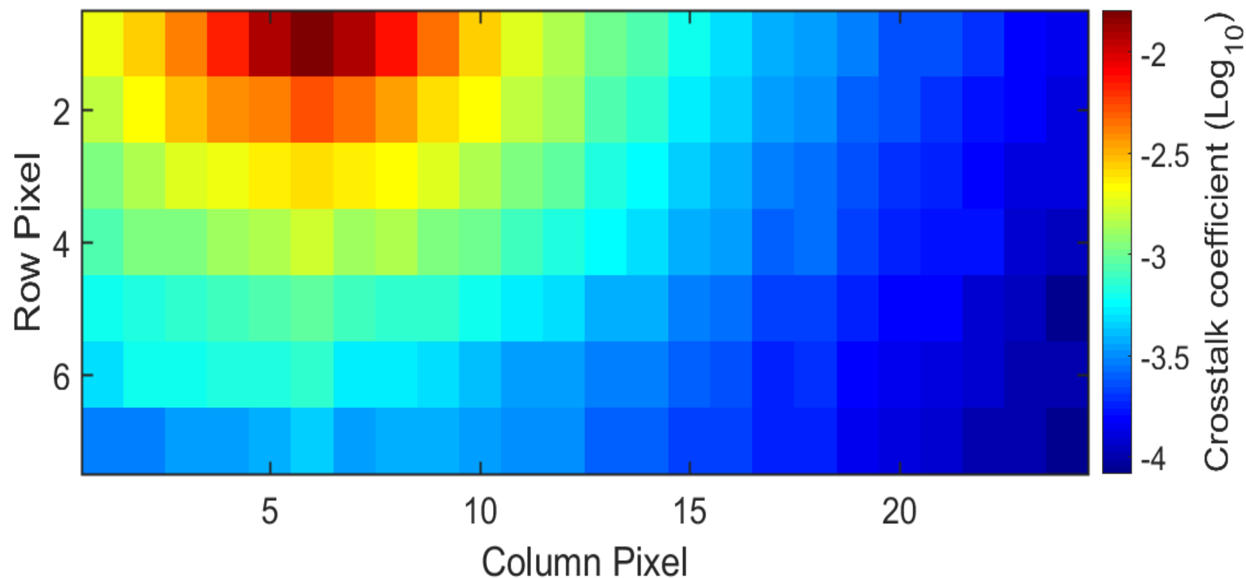
Crosstalk characterization



- Crosstalk coefficient

$$CR_m = DCR_e \cdot DCR_d \cdot 2\Delta T + \mathbf{K} \cdot (DCR_e + DCR_d)$$

- **Emitter** (fixed)
- **Detector** (scan)



Crosstalk map – Type 1, 25μm thickness

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Crosstalk vs substrate thickness

Crosstalk coefficient vs. Distance [mm]

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Dark Count Rate and cross-talk

Single pixel on
All matrix on

Die thickness: 280 µm

Large detectors
T = 20°C
V_{EX} = 3.3V

DCR [Hz]

Pixel

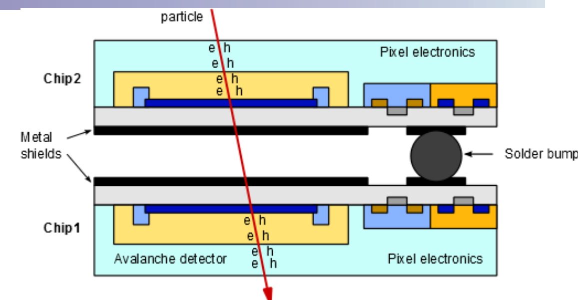
Median DCR increase of 70% due to cross-talk: from 2.8kHz to 4.8kHz

A. Ficorella, et a., Proc. IEEE ESSDERC, 2016

Vertically-integrated assembly

Dark Count Rate vs. coincidence time ΔT

$$DCR_{COINC} = DCR_1 \times DCR_2 \times 2\Delta T$$



Distribution comparison - Type 2

DCR C1
DCR C2
10 ns
1.5 ns
0.75 ns

T = 20°C

Coincidence Rate [Hz]

Pixel

ΔT = 1.5ns

ΔT = 10ns

ΔT = 0.75ns

DCR_{COINC} = 27 counts/s mm²

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β-source measurements

^{90}**Sr** β source – 37kBq at 2mm distance from sensor

V_{EX} = 2V   T = 5°C   Δt = 0.75ns

No Source
With β source

β count rate **~10,7 Hz/mm²**

~ 40 mHz/pixel

Coincidence Rate [mHz]

10^0 10^1 10^2 10^3 10^4

0 20 40 60 80 100

% devices

particle
Pixel electronics
Chip2
Metal shields
Solder bump
Chip1
Avalanche detector
Pixel electronics

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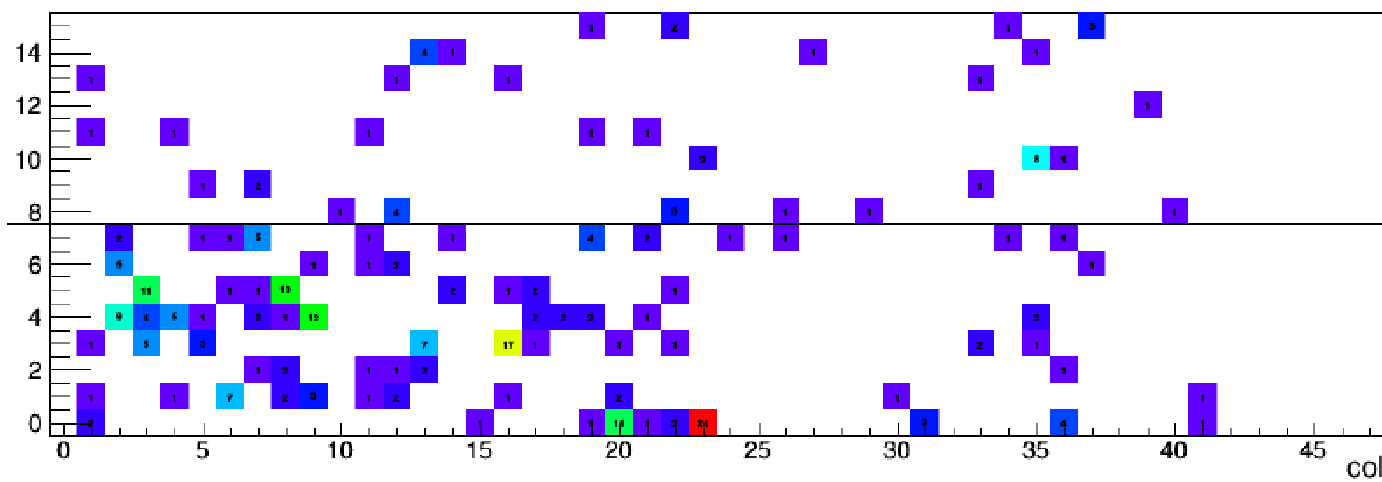
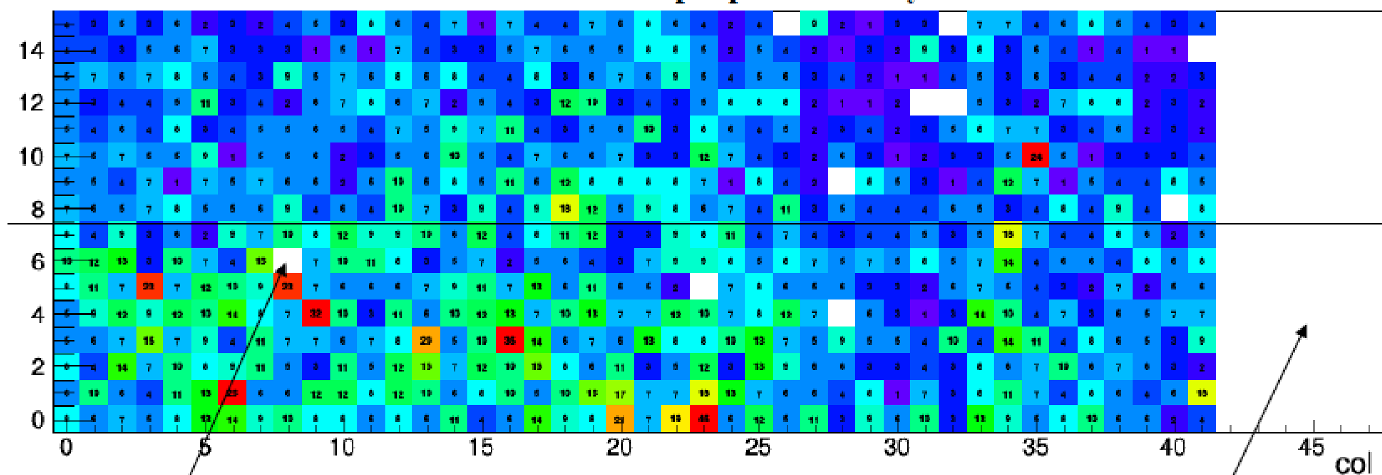
Test beam at CERN

- Test at CERN SPS north area facility (H4 beam line)
- Two APIX under test + auxiliary Beam Tracker detector
- Positrons and π^+ beams at 50, 100, 150, 200 and 300 GeV

Test beam – hit maps





Noisy pixel disabled

Unshielded pixels disabled

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APiX - Summary

Strengths:

- Can be thinned to a **few microns**: low material budget
- **Timing resolution**
- Low **power consumption**
- Early signal digitization

Weaknesses:

- Radiation tolerance (still to be assessed)
- Efficiency: guard ring and in-pixel electronics
- Cost and availability of 3D integration technologies

Current - future work

- Current prototype:
  - **Test beam** data analysis (in progress)
  - Radiation hardness studies
- Design of **new prototype**:
  - Improved fill factor
  - Larger array
  - Optimized timing
  - Optimized power consumption

Summary

- Higly parallel SPAD systems require high-density digital circuit for high efficiency
- SPAD technology in **deep sub-micron** processes is evolving driven by consumer applications: investments
- Maximum efficiency: **3D integration.** Optical cross-talk is still an issue in systems with very high FF
- Concept of charged-particles direct detection with Geiger-mode detectors in coincidence is feasible
- Efficiency is still an issue, but **timing** can be very good
- Development in deep-submicron SPADs and 3D integration can the key for a full exploitation of this concept

Acknowledgements

APiX2 project

“Development of an Avalanche Pixel Sensor for tracking applications”

Funded by **INFN** – CSN5

Project coordinator: Pier Simone Marrocchesi, INFN Pisa and University of Siena

Partners:

- TIFPA and University of Trento,
- INFN Pavia and University Pavia,
- INFN Padova and University of Padova,
- Laboratoire APC, Université Paris-Diderot/CNRS