X-ray Correlation Spectroscopy: the VIPIC 3D-IC Project

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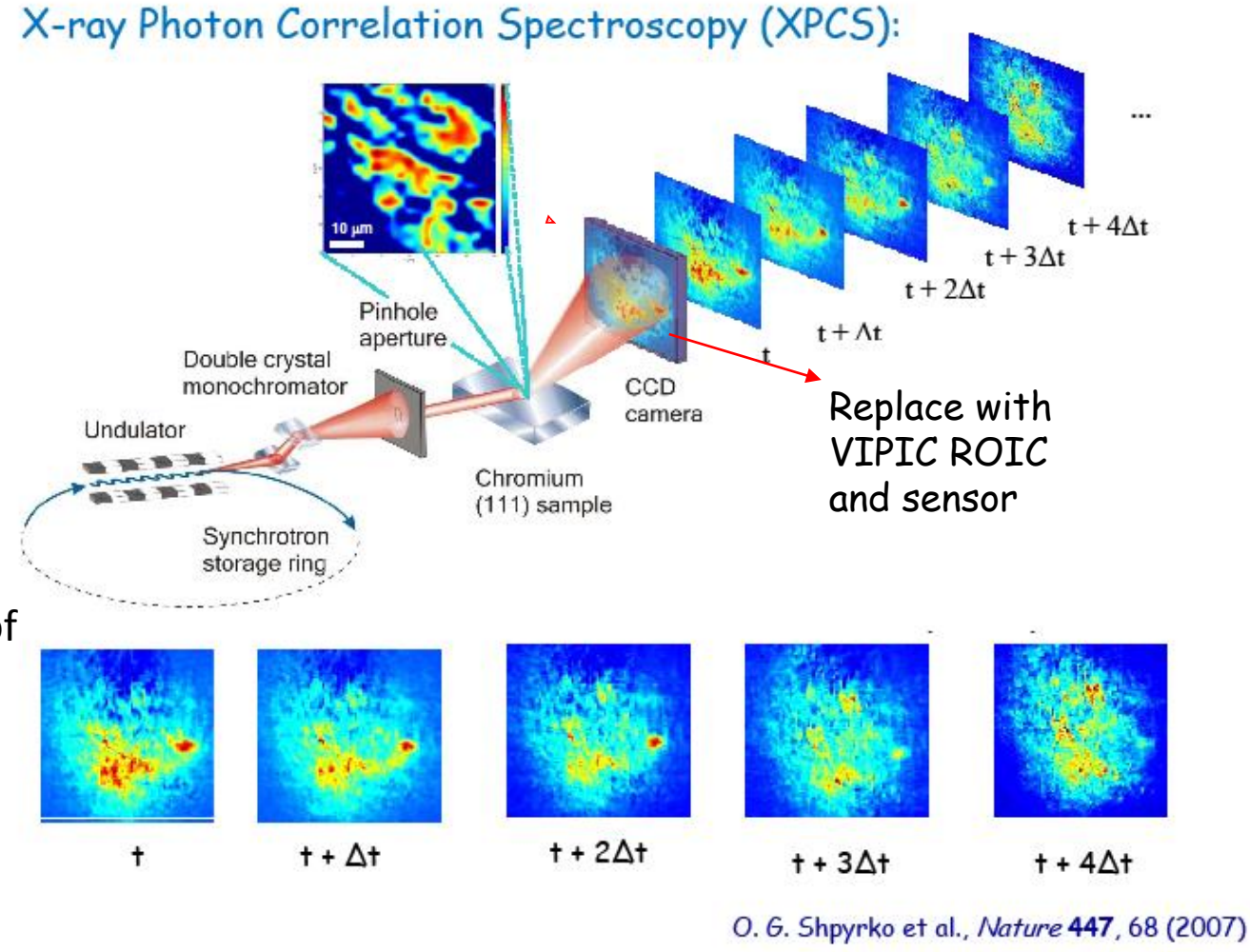
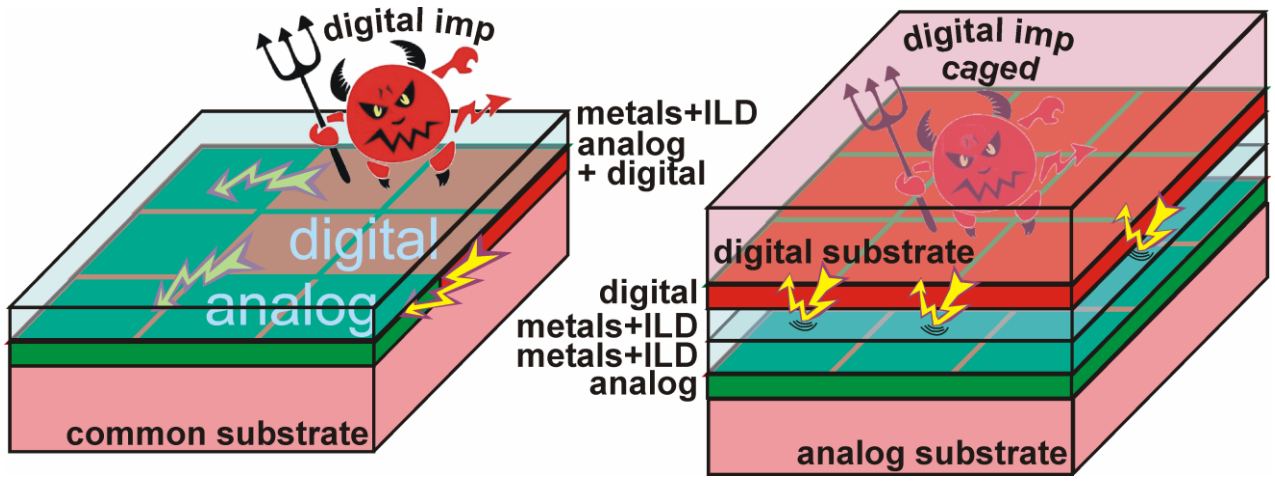
- XCS requires timestamping of each detected photon to high resolution
- Intensities are rather low
- Full-frame readout is wasteful, since most of pixels contain no hits.
- Sparsified readout essential.



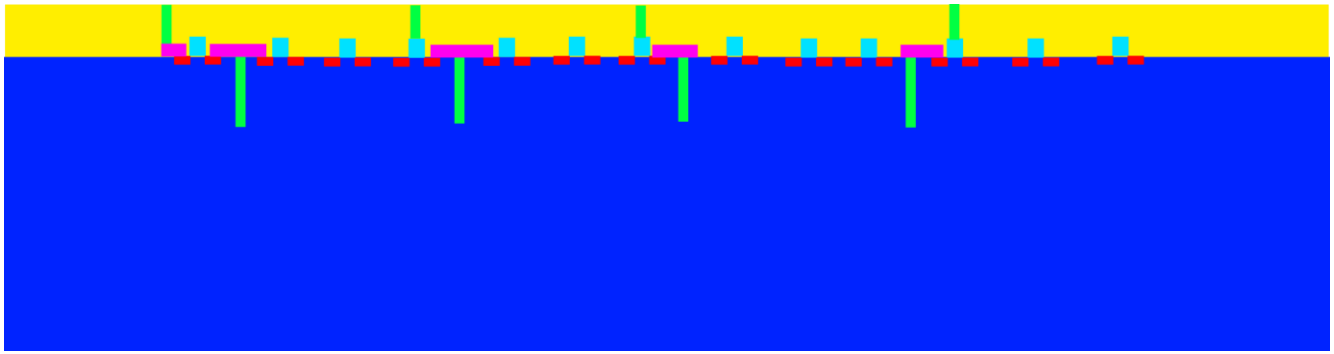
3D integration: What and Why?



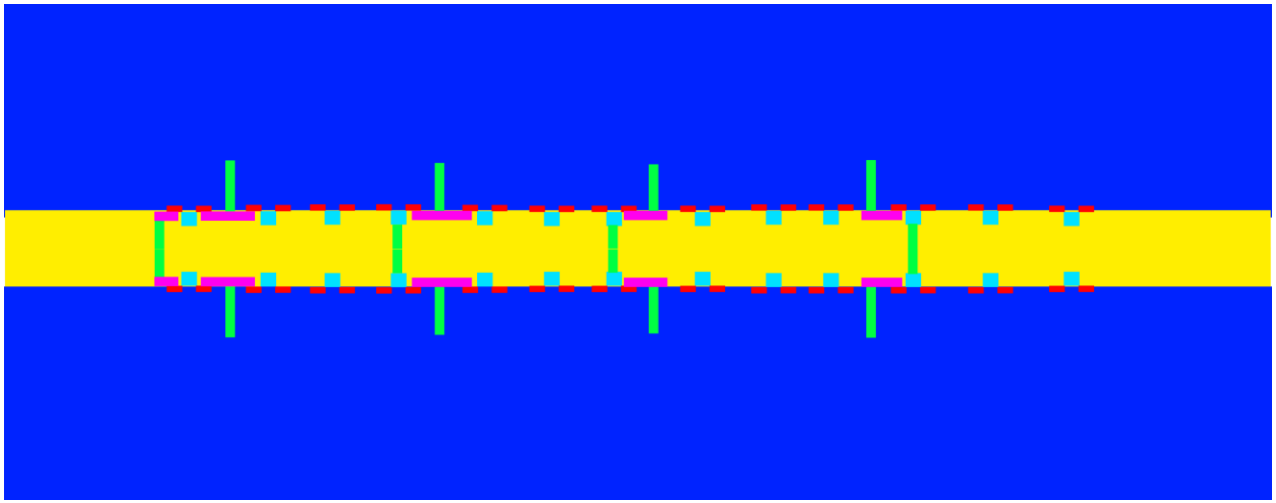
- 3D integration refers to the stacking of CMOS circuits in the third dimension as a way to increase device complexity without heroic measures with device feature size.
- Now in production for memory applications, but VIPIC is the first successful mixed-mode design for photon science applications.
- True separation of digital and low-noise analog circuits
  - Allows choice of technology node which is optimal for each function
  - Provides screening of sensitive, low-noise circuits from digital noise
  - Allows easy power distribution to large-area ASICs.

Via-middle process flow

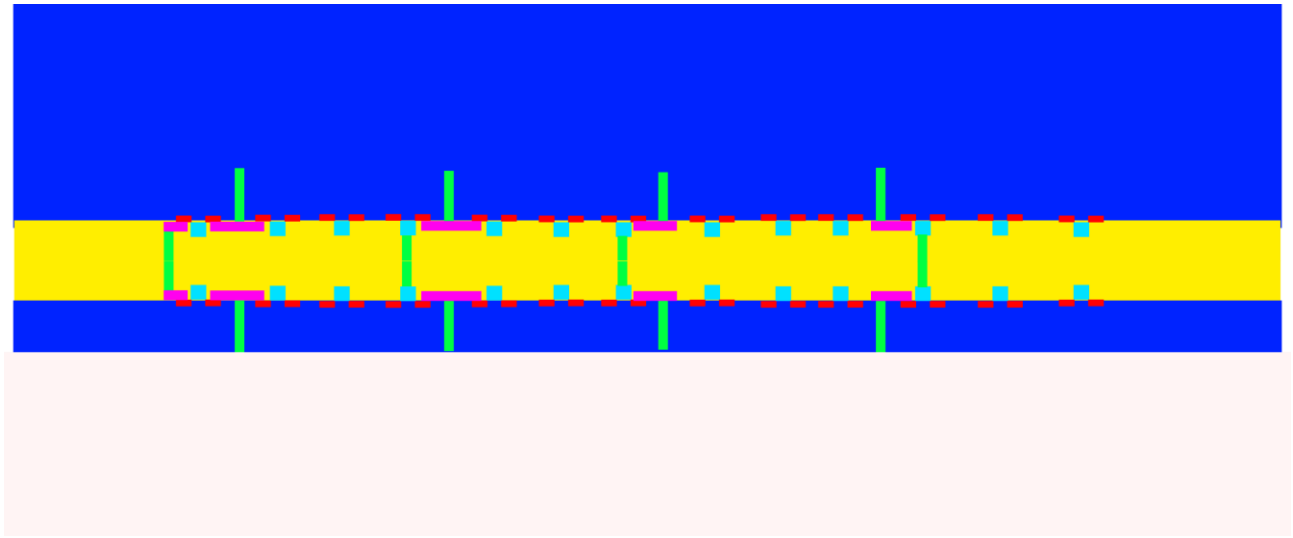
Conventional CMOS process flow
Two extra steps between front-end and back-end processes:
Etch vias into silicon of wafer
Passivate via walls
Fill vias with conductor
Then process all interconnect layers as usual



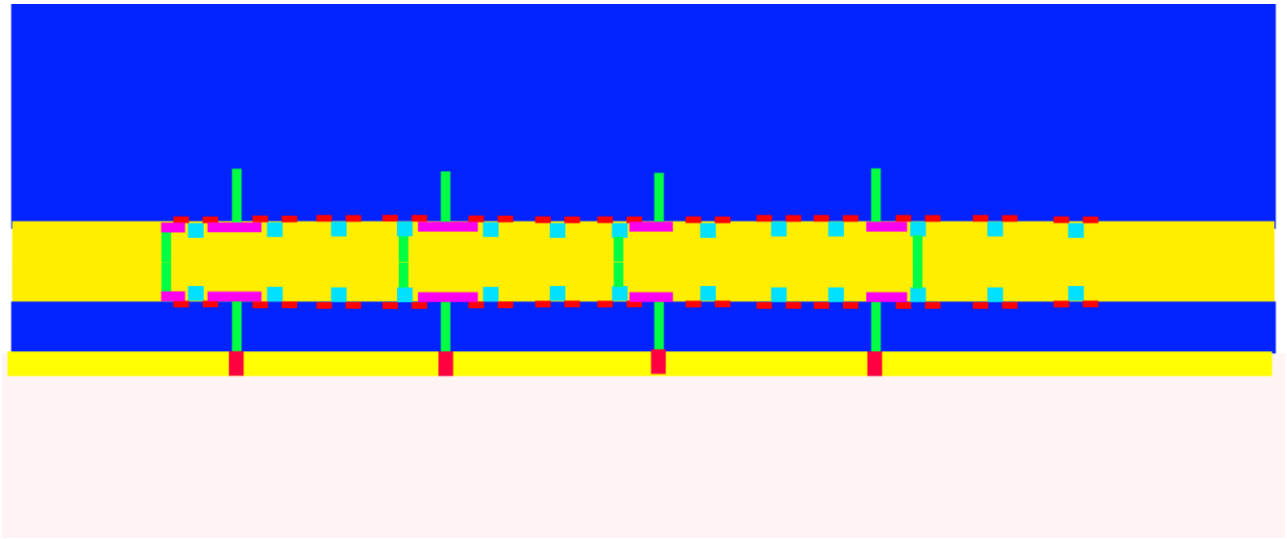
Flip second layer and oxide-bond to first, aligning contacts.



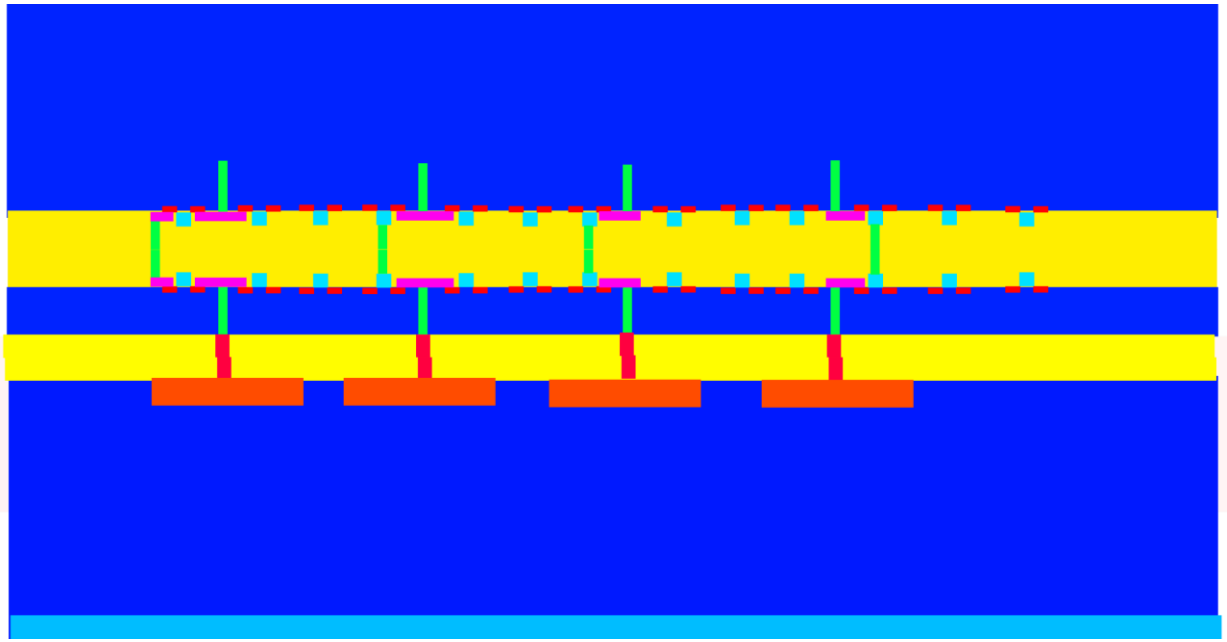
Grind off bottom wafer to expose TSVs



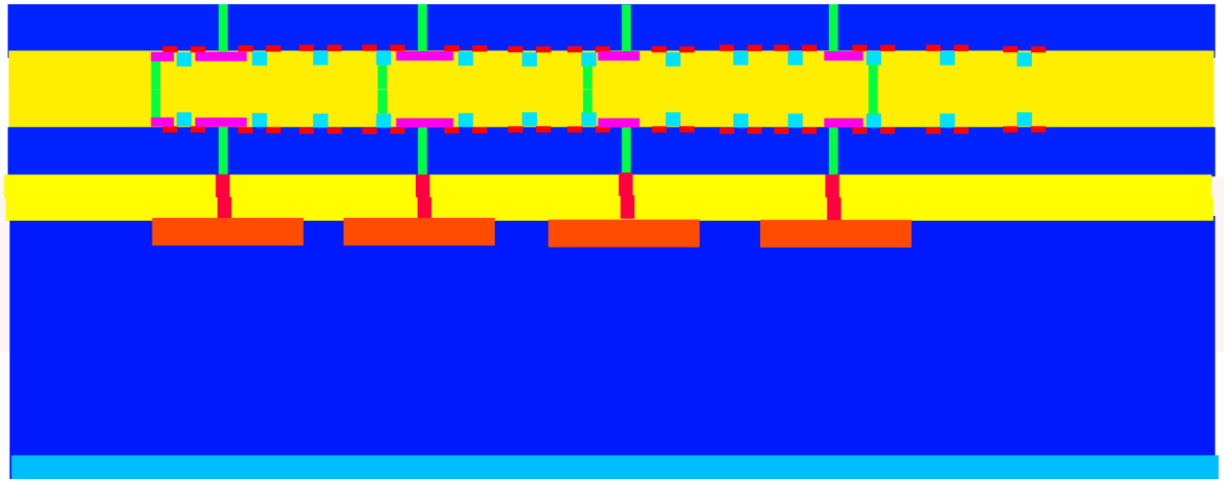
Deposit oxide layer and make contacts



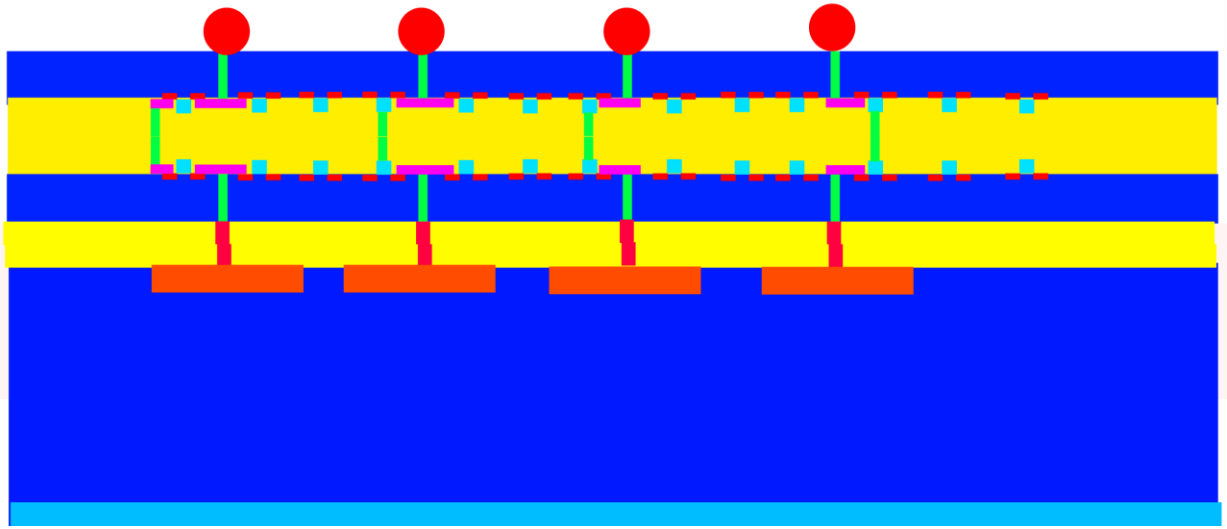
Oxide-bond detector to 2-layer ASIC



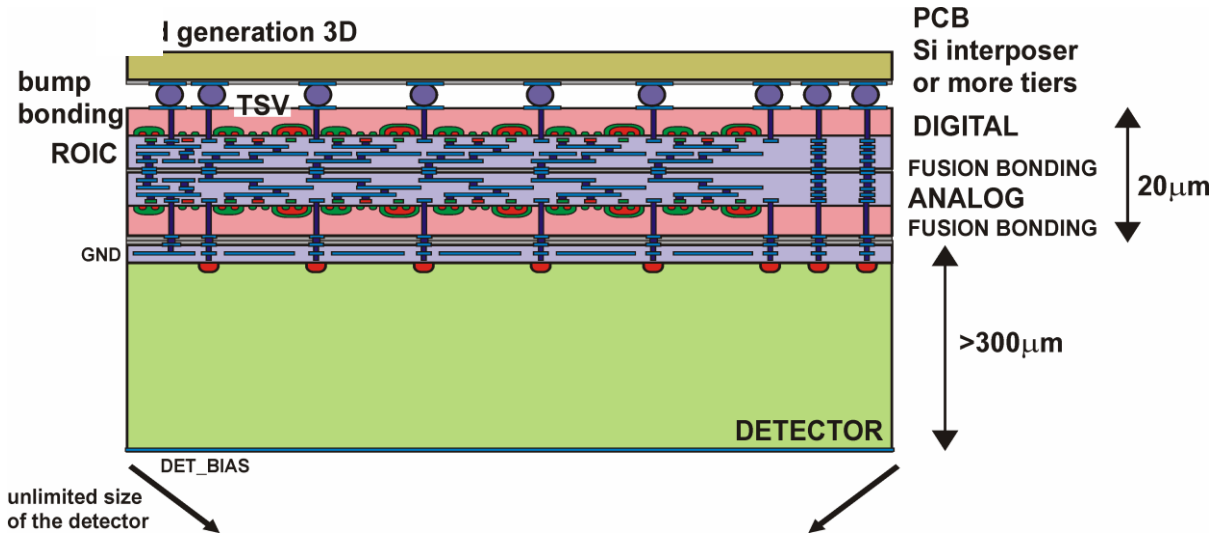
Grind off top layer to expose TSVs



Attach bumps for Flip-Chip mounting to PCB



3D opens the door to truly gap-free large-area detectors



- The availability of Through-Silicon Vias (TSVs) allows direct contact to the circuitry from any point on the device
  - Allows dense interconnection to sensor
  - Allows dense interconnection to outside world
- No need to leave edge-space for wire-bonding and its resulting gap in active area of detector.

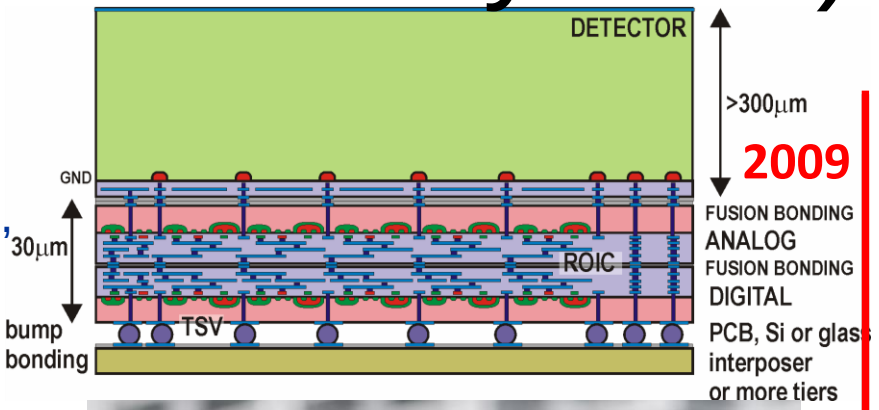
VIPIC1 (1st 3D MPW run by HEP)

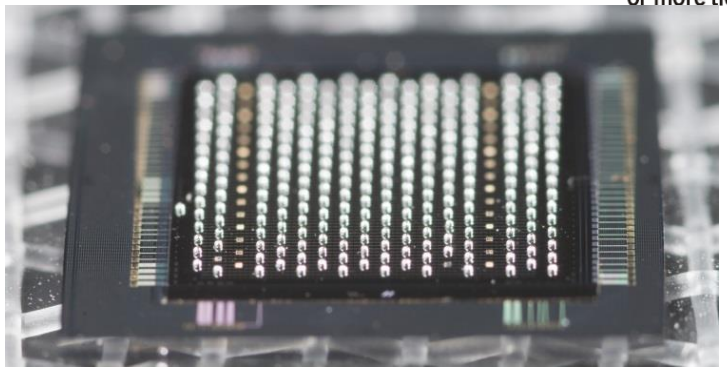
Vertically Integrated Photon Imaging Chip

Small prototype: 64 × 64 pixels, 80 μm pitch, Si 500+ μm thick sensor

measure time-of-arrival (ToA) for 2D autocorrelation @ <10 μs

develop practices and techniques applicable later in devices for HEP and Photon Science





APS beam tests

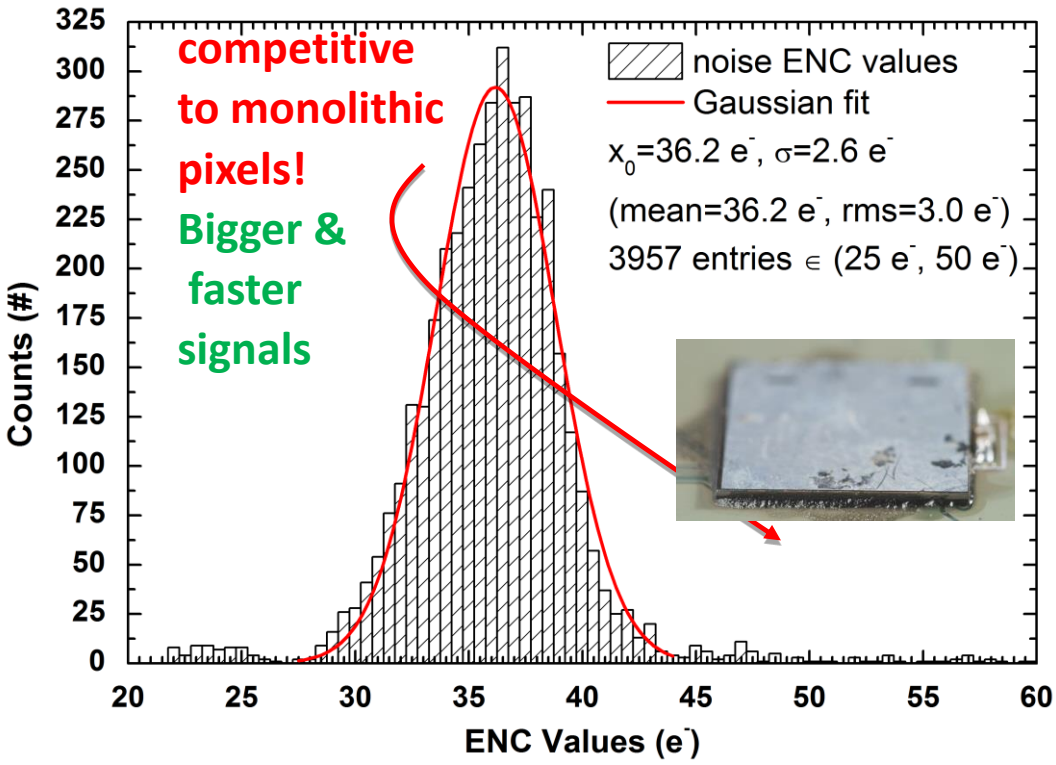
July and October 2014

Samples of nanoparticle colloids and standard XCS analysis (multi-tau correlator) allowed observation of dynamics with sub-millisecond relaxation times

VIPIC1 Noise Performance

3D integrated pixels merge good features of monolithic (noise) and hybrids (functionality rad hardness, sensor optimization)

ENC on fusion bonded device is close to that measured for floating inputs!



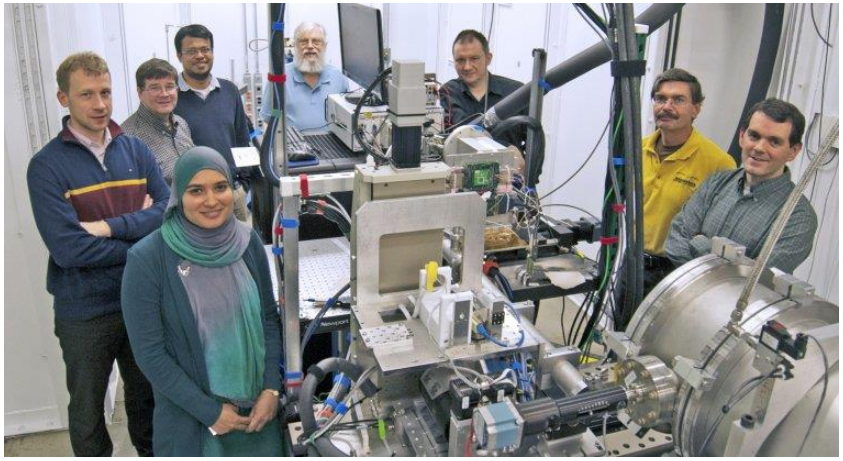
ENC=36.2 e⁻

symmetrical noise distribution with

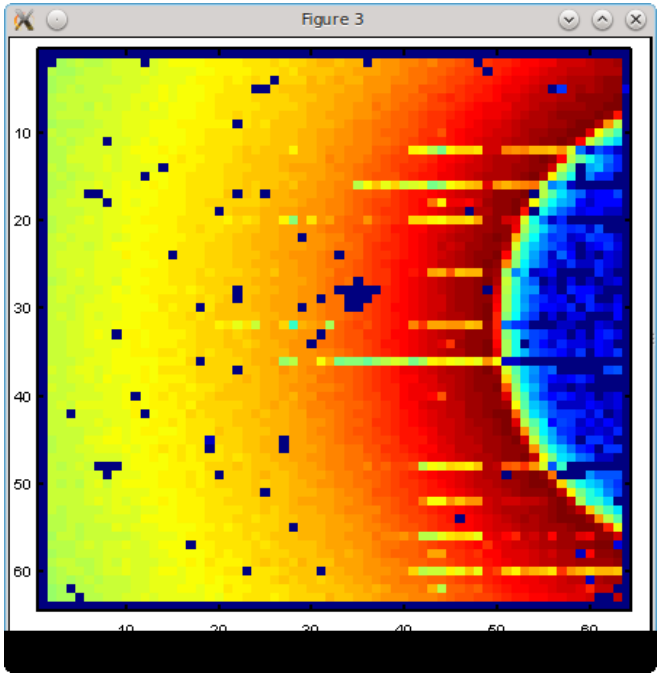
<3.4 % of pixels outside of ±3 σ

VIPIC1 XCS results

Tests performed at 8ID-I beamline at the APS in July and October 2014



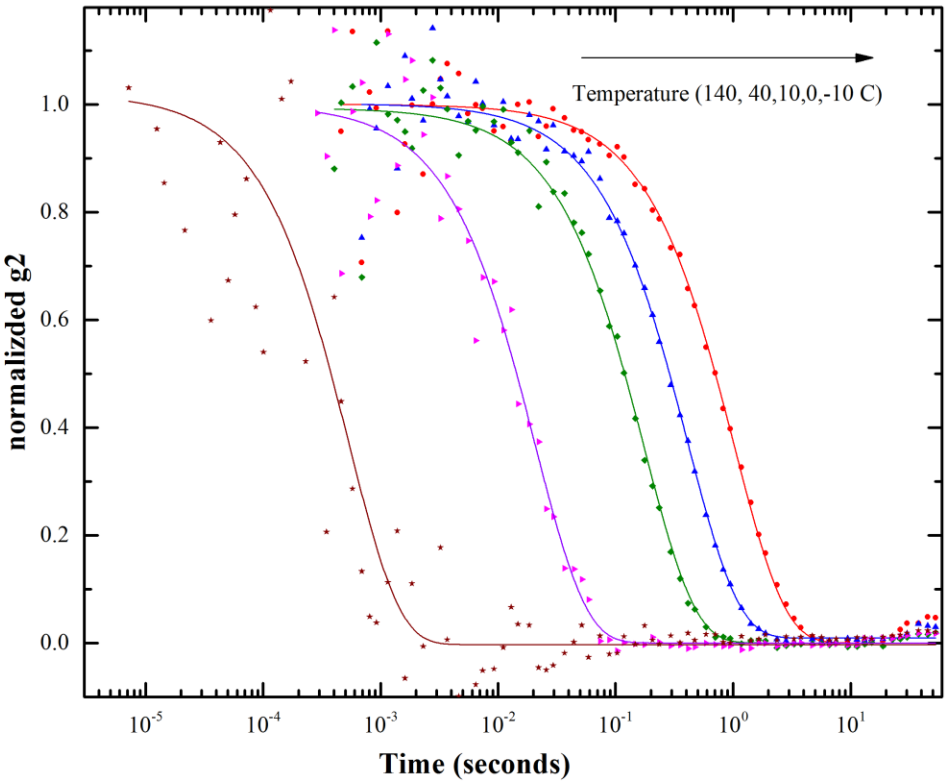
Microsecond-scale relaxation times, which are inaccessible by conventional frame oriented detectors, were measured using VIPIC1. Given sufficient intensity, it is now possible to collect data continuously from the microsecond time scale up to minutes, which opens up the XCS field to a much wider range of scientifically interesting experiments.



Time-integrated image of scattering pattern recorded by VIPIC

Temperature changes of Latex spheres in Glycerol

This data shows the autocorrelation function of a sample of latex spheres suspended in a glycerol solution. The different curves show the result for several temperatures. The samples were sealed in a glass capillary to prevent evaporation at high temperature. The data is continuous from a few microseconds to a few minutes, and represents several times 10^8 time intervals.



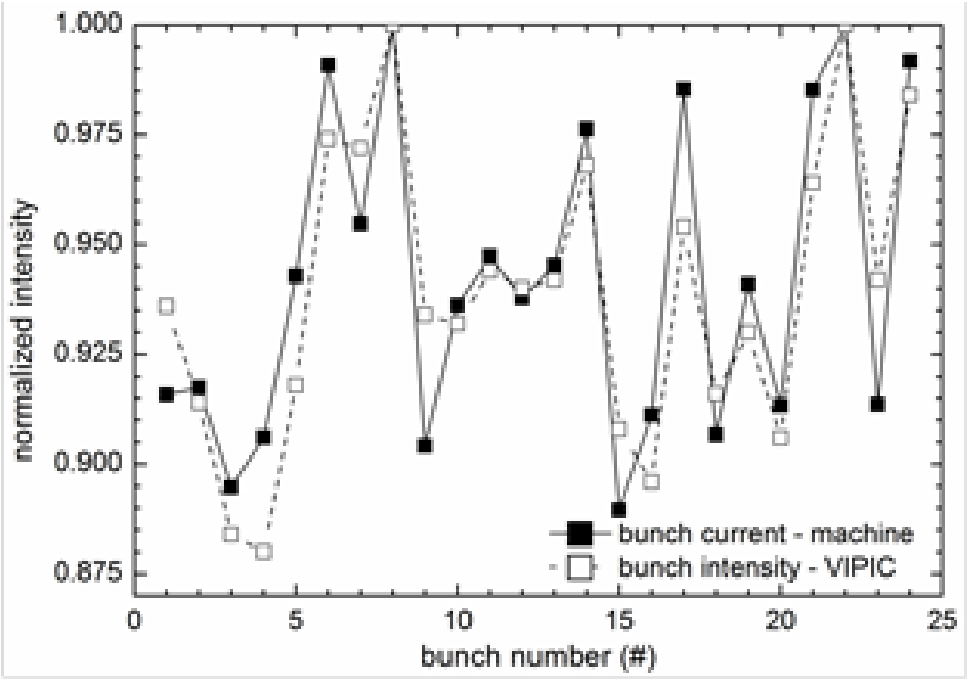
intensity autocorrelation function of polystyrene particles suspended in glycerol at different temperatures

Bunches

Data was collected with a frame time of 153 ns, synchronized to the APS ring round-trip time.

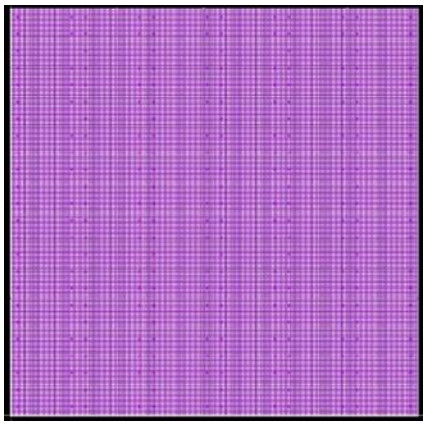
The graph shows this data plotted over the accelerator bunch current

The close correspondence between our data and the independent measurement by the storage ring diagnostic system shows that the detector functions correctly down below 1 microsecond.

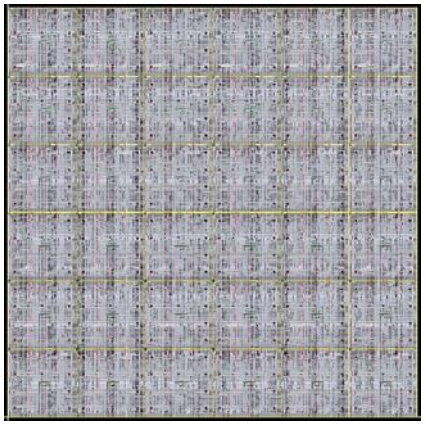


VIPIC-L ASIC

- Building a full-scale (1 Mpixel) version
- Smaller pixel (65 microns)
- Large ASIC; >100M transistos
- 192 x 192 pixels each 65um^2
- 12.85 mm x 12.85 mm
- 36 LVDS data lines per chip
- 400 Mbs serial rate -> 14.4 Gb/s
- Sparsified readout or full-frame readout @ 50k frames/sec.

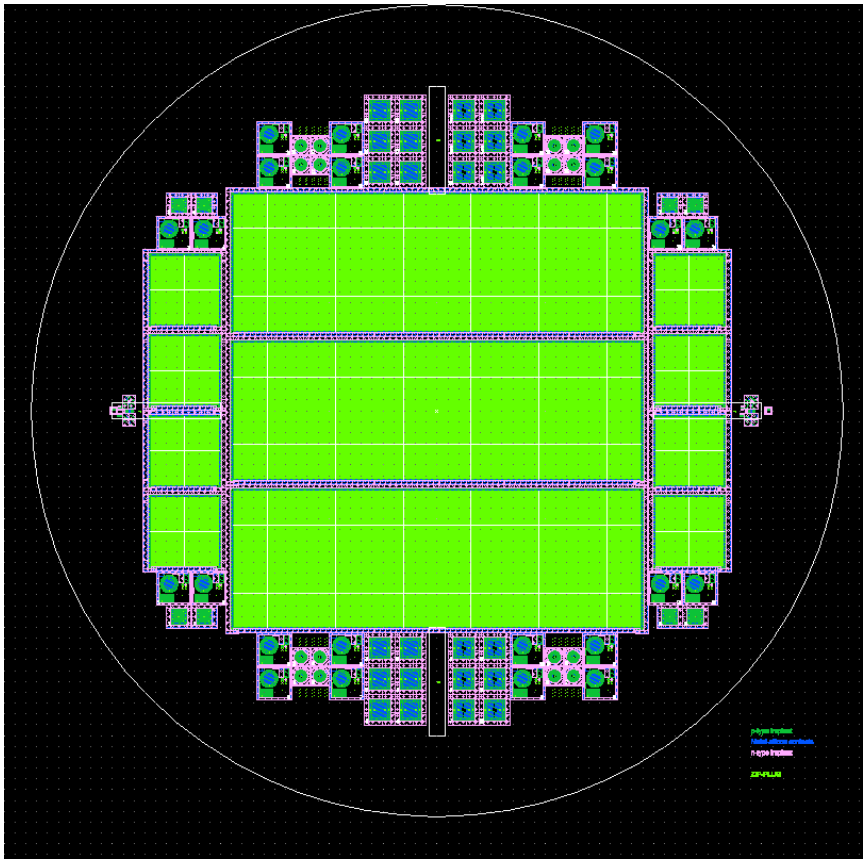


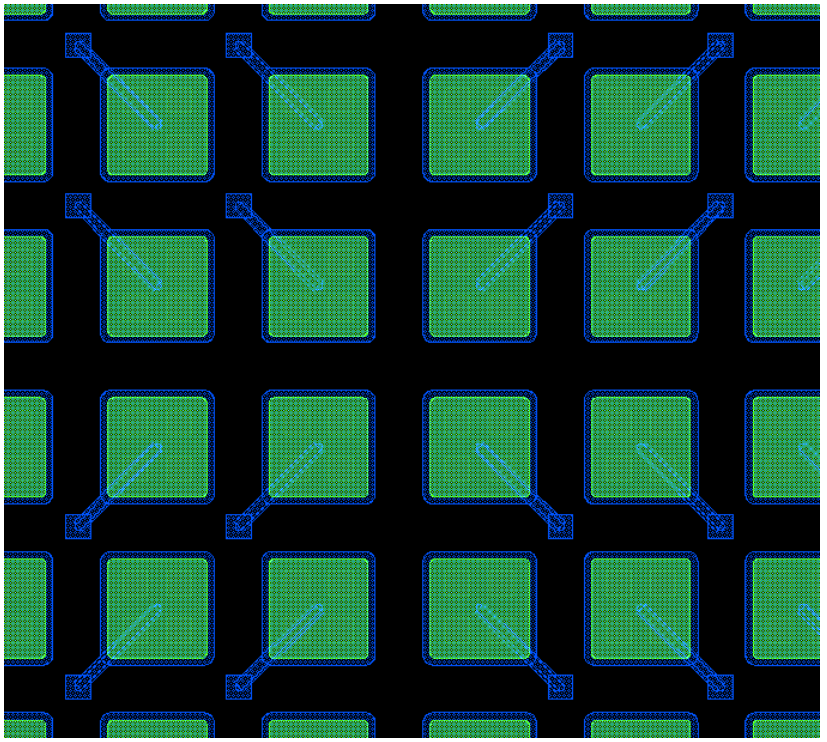
Analog tier



Digital tier

Sensors



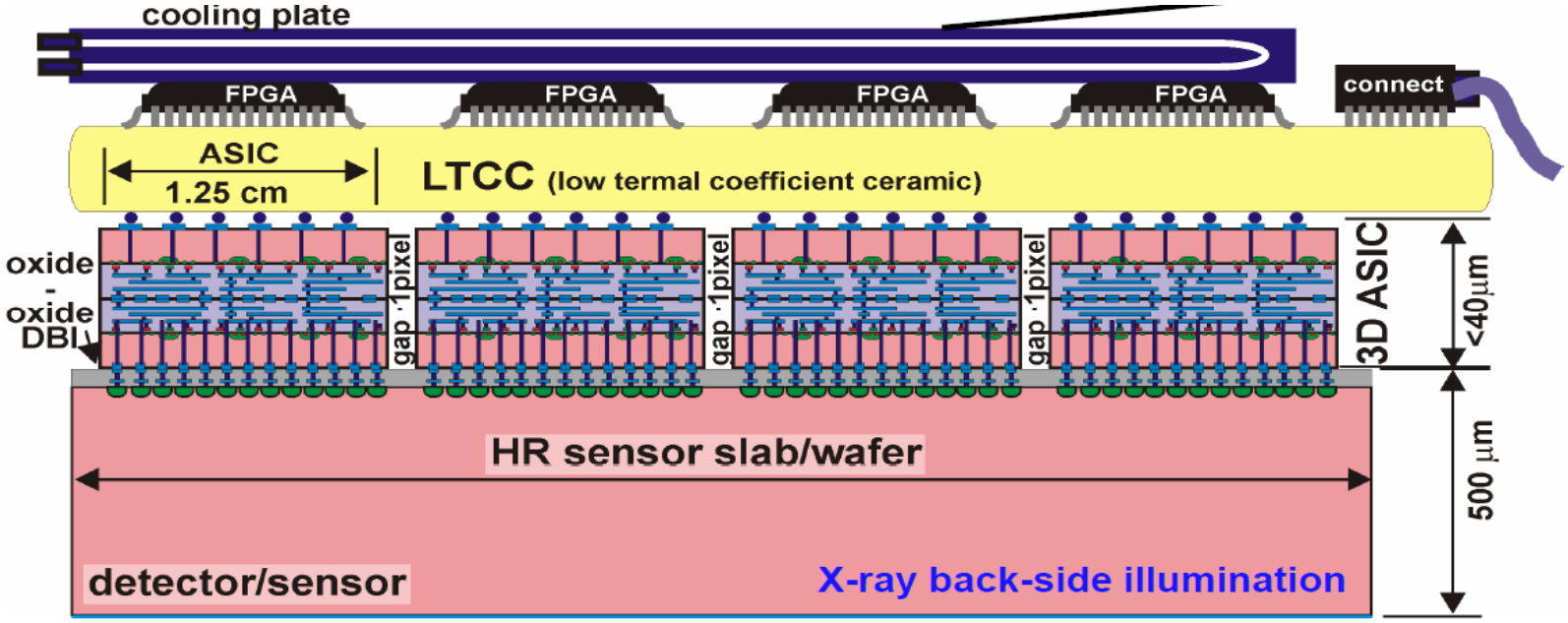


P-in-N diodes on 6” wafers. Each wafer carries three 2x6 blocks plus 8 single-ASIC blocks for initial testing. (a) shows the wafer level, (b) shows pixel details..

VIPIC: >1MPixel 3D Camera

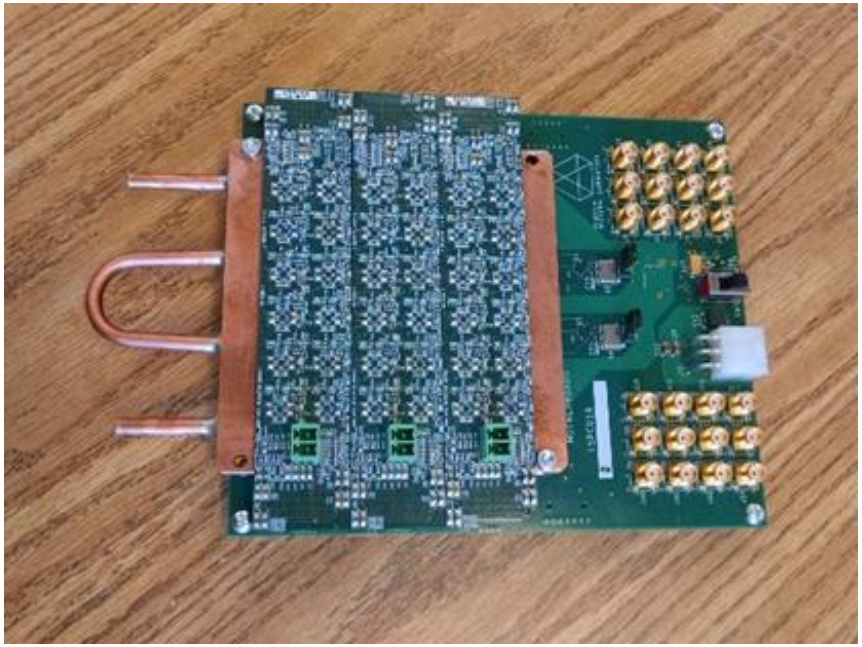
Ultimate GOAL: To build a single module 3D camera with minimal gap

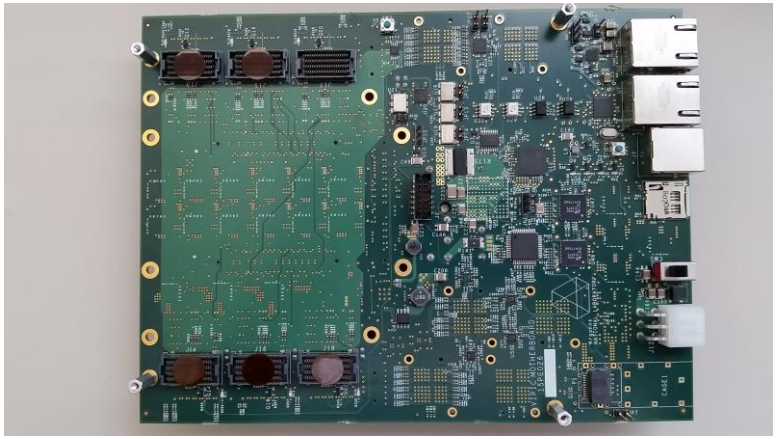
- Contains three 2x6 arrays of large ASICs each with ~37000 pixels
- (1.3Mpixel camera module)
- LTCC hosts FPGA based processing units
- Approximately 1 FPGA per chip.
- No dead space between ASICs within 2 x 6 array.



Front-end motherboard

- Three modules, each 2 x 6 ASICs
- Monolithic sensor per module, no gaps
- Water-cooling.
- Zynq processor to handle slow controls and data flow via FPGA fabric.





Summary

- We have built the first fully-functional mixed-mode 3D integrated circuit for photon science
  - The technology opens the door for more functionality per pixel with optimized processes for each tier
  - It allows much better power distribution to a large-area ASIC
  - It provides a lower-noise sensor interconnect than bump-bonding
  - It shows the way towards zero-gap tiling of detectors since there is no need for an exposed ASIC edge for wire-bonds
- We have tested a prototype detector at beamline 8-ID at APS using samples with a range of dynamic behaviour, showing that it performs as expected down to at least 10 microsecond intervals, and even into the 100 nanosecond regime.

Acknowledgments

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