Analytical Expressions for Noise and Crosstalk Voltages of the High Energy Silicon Particle Detector

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Abstract

This work presents design and implementation of a silicon particle detector array with the derived closed form equations of signal-to-noise ratio (SNR) and crosstalk voltages. The pixel array has been designed and simulated in a 180 nm BCD technology of STMicroelectronics. The technology uses the supply voltage (V_{DD}) of 1.8 V and the substrate potential of -50 V. The area of a unit pixel is 250 × 50 μm^2 with the substrate resistivity of 125 Ωcm and the depletion width of 30 μm. This work compares the results of noise and crosstalk analyses from the proposed mathematical model with the circuit simulation results for a given simulation environment. The results show excellent agreement with the circuit simulations and the mathematical model. The average relative error generated for the noise spectral densities with respect to the simulations and the model is 12 % whereas the comparison gives the errors of 3 % and 11.5 % for the crosstalk voltages and the SNR results respectively.

1. Analog Chain of a Unit Pixel

- The presented noise analyses and SNR calculation consider the center pixel with its eight nearest neighbouring pixels, coupled with interpixel capacitances (IPC). The adjacent pixels of the neighbouring pixels have been replaced with a single equivalent capacitance.
- For simplicity, all the pixels in the array are assumed to be identical and have similar front end electronics. The noise model is shown in Figure 1(b)[1, 2].

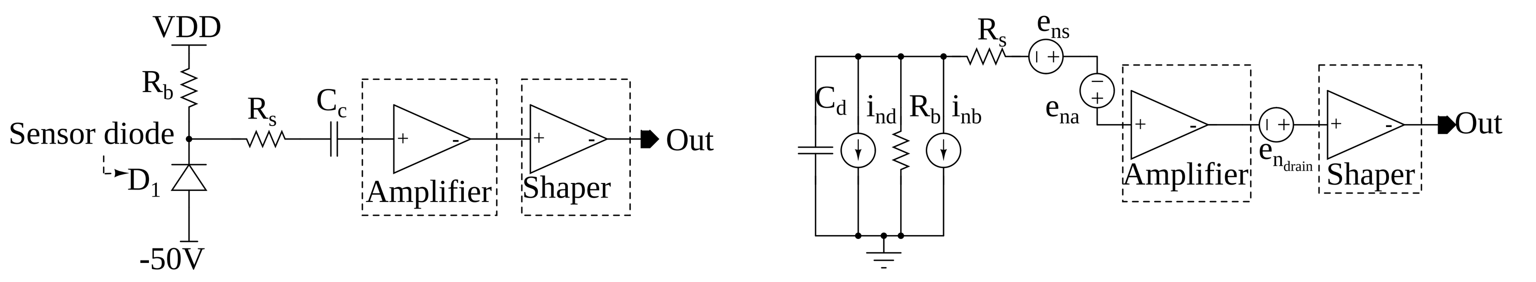

Figure 1: *(a) Detector front end circuit for a unit pixel, (b) The equivalent small signal circuit of Figure 1(a) to calculate noise.*

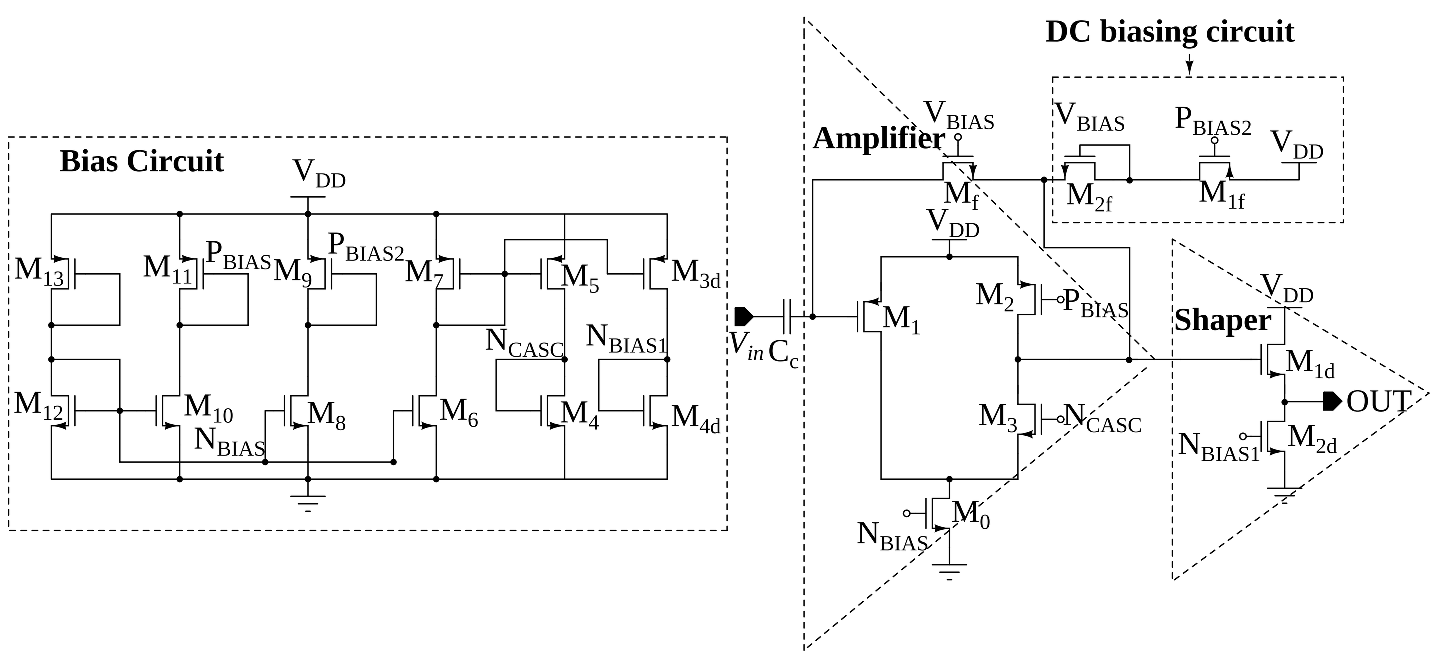

Figure 2: *Amplifier and shaper configurations in cascade.*

2. Closed Form of Equations of Noise and Crosstalk Voltages

Figure 3(a) shows the arrangement of pixels considered for analysis.

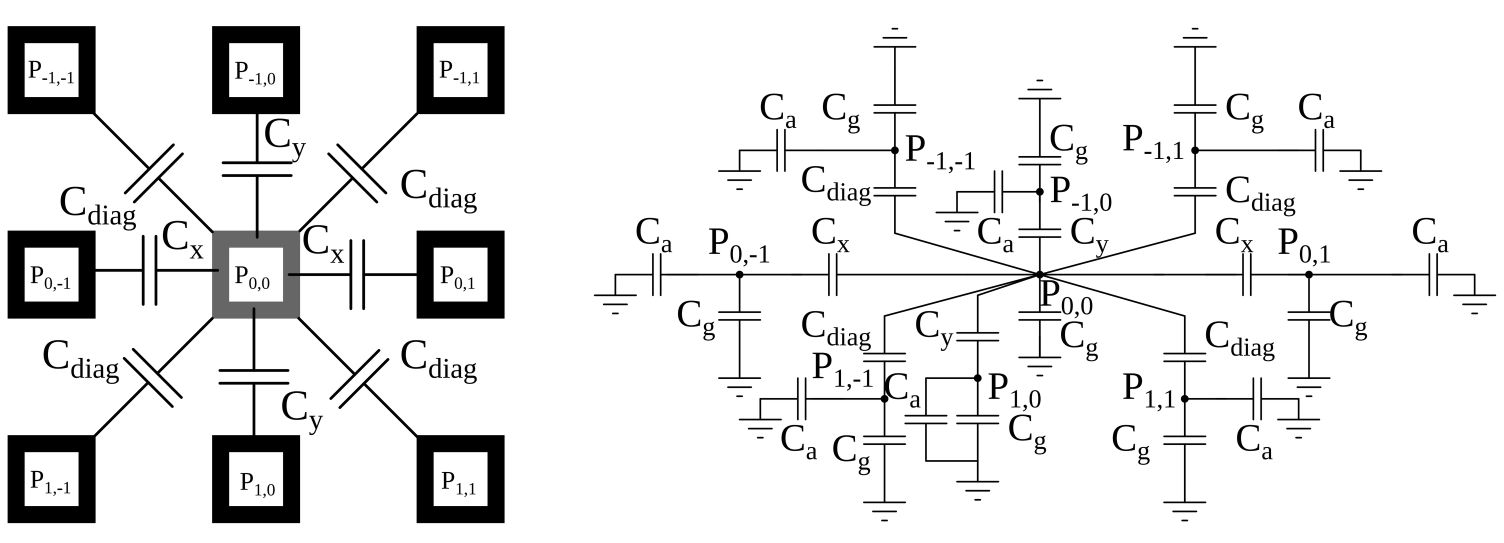

Figure 3: *(a) Center pixel ($P_{0,0}$) with its nearest neighbours, (b) Circuit for the calculation of capacitance, $C_{apparent}$.*

- Total root mean square (rms) noise voltage at the output of shaper for a given band of frequency with ω_l and ω_h as lower and higher corner frequencies, is given by following equation:

$$V_{rms}^{n} = \sqrt{\frac{1}{2\pi}\int_{\omega_l}^{\omega_h}(e_n^2(\omega)|A_v(\omega)|^2 + e^2_{n_{drain}}(\omega)|A_{shaper}(\omega)|^2)\,\mathrm{d}\omega} = \sqrt{\frac{[e'^2_{nd} + e'^2_{nb} + e'^2_{ns} + e'^2_{na} + e'^2_{n_{drain}}]_{\omega_l}^{\omega_h}}{2\pi}}$$

- $e'^2_{nd}, e'^2_{nb}, e'^2_{ns}, e'^2_{na}, e'^2_{n_{drain}}$ are integrated noise spectral density of diode (due to shot noise), bias resistance, parasitic resistance, amplifier and shaper respectively.
- A_v is total gain of configuration shown in Figure 2 and A_{shaper} is the gain offered by the shaper.
- When charge, $Q_{injected}$ is injected on $P_{0,0}$, a crosstalk voltage is generated on neighbouring pixel due to IPC is:

$$V_{crosstalk} = \frac{C_{ipc}}{C_{ipc} + C_a + C_g}\cdot\frac{Q_{injected}}{C_{apparent}},$$

where, C_{ipc} is the respective IPC for neighboring pixel, C_a is the equivalent of all the adjacent capacitances of neighbouring pixel, C_g is the equivalent capacitance of $P_{0,0}$ to ground including the junction capacitance of sensor diode, input and feedback capacitance of the charge sensitive amplifier.

- The voltage signal at the input of the center pixel ($P_{0,0}$) is given as:

$$V_{sig}^{in} = \frac{Q_{injected}}{C_g} - 2V_x - 2V_y - 4V_{diag}, \quad V_{sig} = V_{sig}^{in}|A_v|,$$

where, V_x, V_y and V_{diag} are the crosstalk voltages generated on neighbour in x, y and diagonal directions respectively and V_{sig} is the voltage signal at the shaper output of $P_{0,0}$.

- SNR expression at the shaper output of $P_{0,0}$ is given as:

$$SNR = 20\log\left(\frac{V_{sig}}{V_{rms}^{n}}\right).$$

3. Simulation Results

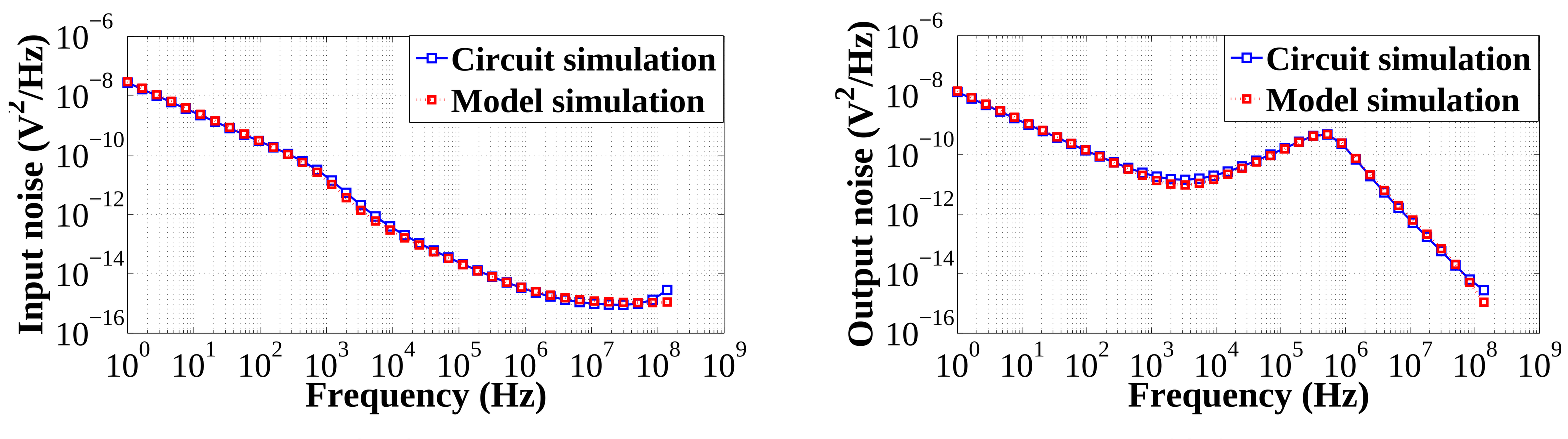

Figure 4: *(a) Input noise voltage spectral density, (b) Output noise voltage spectral density.*

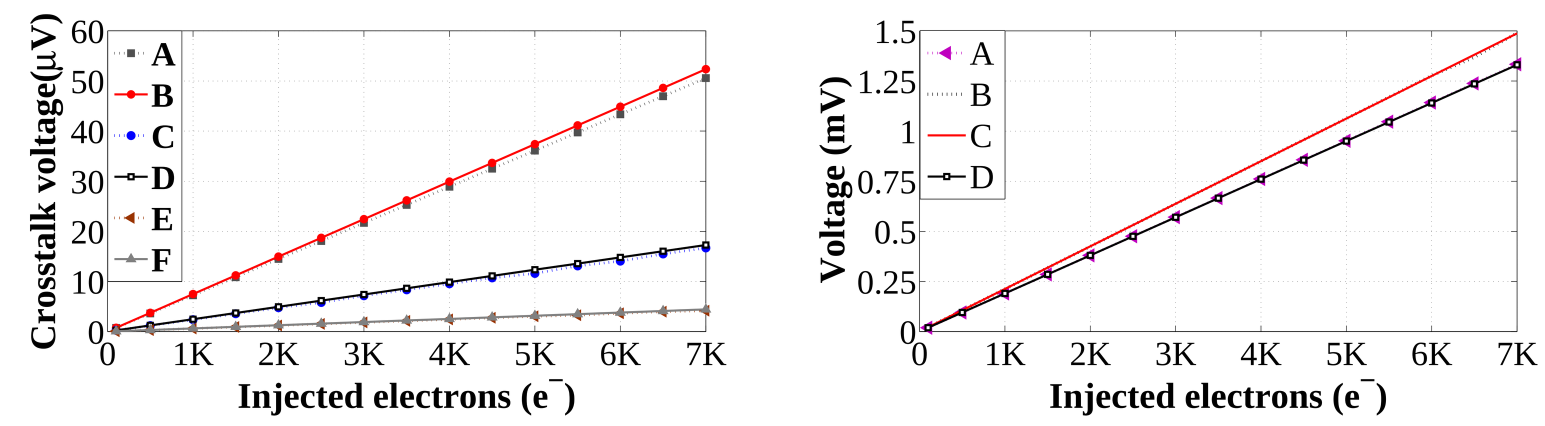

Figure 5: *(a) Crosstalk voltage generated on neighbours when electrons are injected on center pixel ($P_{0,0}$), where A, C and F are circuit simulations for $P_{0\pm1,0}$, $P_{0,0\pm1}$ and $P_{0\pm1,0\pm1}$ respectively; B, D and E are model simulations for $P_{0\pm1,0}$, $P_{0,0\pm1}$ and $P_{0\pm1,0\pm1}$ respectively, (b) Voltage generated on center pixel ($P_{0,0}$) when electrons are injected, where A and D are circuit and model simulations with crosstalk respectively; B and C are circuit and model simulations without crosstalk respectively.*

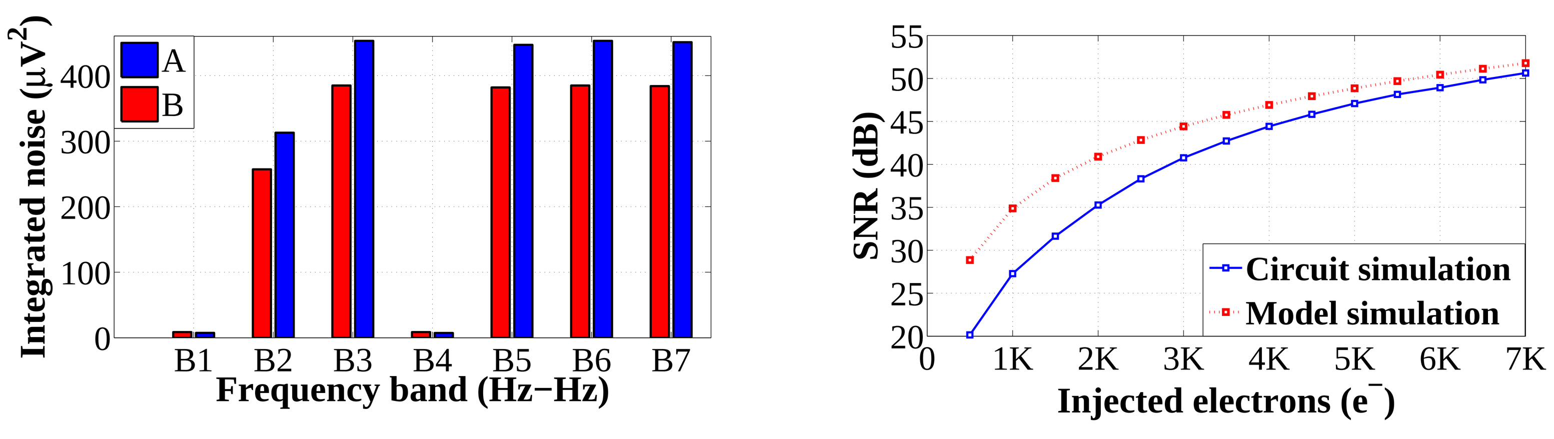

Figure 6: *(a) Integrated output noise,where A and B are circuit and model simulations respectively; B1 = 1–0.1M, B2 = 1–1M, B3 = 1–100M, B4 = 1K–100K, B5 = 1K–10M, B6 = 1K–1G and B7 = 5K–22M bands, (b) SNR at the shaper output of the center pixel in the presence of low and high frequencies noise and, crosstalk.*

4. Conclusions

- The results obtained from MATLAB model follow circuit simulations..
- As shown, the voltage signal at center pixel and the SNR are reduced because of IPC. Hence, capacitive crosstalk has a significant affect on noise performance in large area detectors.
- The presented SNR and noise voltage expressions can be further useful to design these kind of detectors with improved noise and crosstalk performance.

References

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[2] R. Kleczek and P. Grybos, *FSDR16–fast and low noise multichannel ASIC with 5th order complex shaping amplifier*, *IEEE Transactions on Nuclear Science* **60** (June, 2013) 2188–2195.