Design of a Charge Sensitive Amplifier for Particle Detection Application in BCD 180 nm Technology

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Abstract

This paper presents a design of charge sensitive amplifier (CSA) for silicon particle detection. This is the first attempt to design an analog processing circuit of the 47 X 6 silicon detector matrix in BCD 180 nm technology. A unit sensor pixel is realized as a diode with a dimension of 250 X 50 µm^2 and the analog front end of the sensor is confined in the sensor diode itself to achieve 100% fill factor. A single stage, single ended, low power and area efficient folded cascode amplifier is designed as a basic building block of the CSA. Further, a on-chip corner control circuit is designed to achieve cross-corner (process variations) functionality. The proposed corner control circuit is kept outside the sensor matrix and reduces the power consumption in CSA. The complete CSA and the corner control circuit occupy 65 X 25 µm^2 and 38 X 21 µm^2 area per pixel respectively. Noise floor of the CSA within the signal band is 201 nV/√Hz and it typically consumes 11 µA from a 1.8 V of supply voltage (V_{DD}).

Introduction

- Capacitively coupled pixel detector: a CMOS sensor whose output is captured by an analog front end and it is then coupled to readout chip through a thin dielectric layer using hybrid IC design techniques [1].
- STMicroelectronics 180 nm BCD8 technology is a triple well process. It is particularly attractive for particle detectors since it is possible to obtain 100% fill factor theoretically [2].

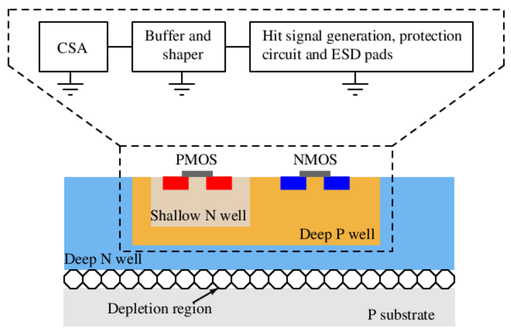


Fig 1: Simplified section of a triple well showing an embedded unit pixel cell and the block diagram of analog signal processing circuit.

- Challenging tasks:
  - Achieving 100% fill factor while maintaining signal integrity.
  - Design of the CSA: single ended architecture is prone to process variations and common mode noise.
  - The simulation environment to emulate the effect of particle injection.

Charge Sensitive Amplifier

- In the case of particle hit, the detected transient signal at the n-well of the sensor diode is amplified by the CSA.
- CSA is a single stage amplifier with negative capacitive feedback. It consists of a gain stage, a DC blocking capacitor and a DC biasing circuit.
- A resistive feedback formed by the transistor M_F provides the DC bias to the input transistor.
- A common drain buffer (not shown here for simplicity) is connected at the output of CSA to drive 1 pF load and bandlimit the signal.
- pMOS input stage helps to reduce cross-talk and improve noise performance.

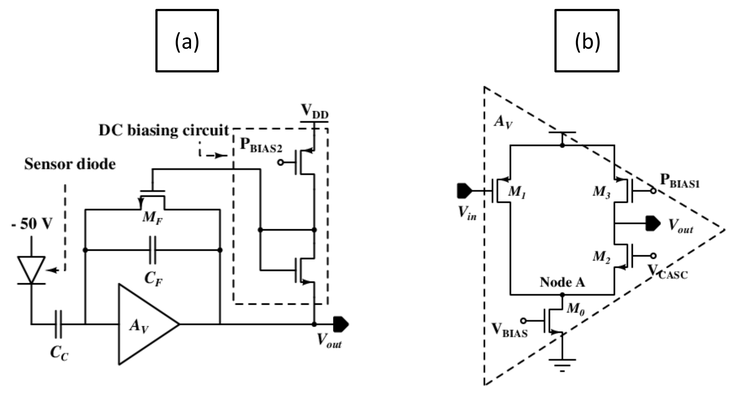


Fig 2: (a) The schematic of charge sensitive amplifier including the DC biasing circuit for resistive feedback, (b) schematic of single stage single ended folded cascode amplifier used in the CSA.

Analysis of the CSA

- In Fig. 2 (b), $R_{OUT} \gg R_A$ and $C_L \gg C_A$ the amplifier can be reduced to first order system with voltage gain given as:

$$A_V(s) = \frac{-A_{dc}}{\left(1 + \frac{s}{\omega_{p1}}\right)}$$

where, $\omega_{p1} = \frac{1}{R_{OUT}\, C_L}$, $R_{OUT} = g_{m2}\, r_{o2}\, (r_{o1} \,||\, r_{o0}) \,||\, r_{o3}$, $C_L = C_{GD2} + C_{GD3} + C_{IBUFF}$ and A_{dc} is the DC gain of the amplifier.

- The closed loop transfer function ($\frac{v_{out}}{v_{in}}$) is:

$$A_{CL}(s) = \frac{-s\, R_F\, C_C\, A_{dc}}{\left(1 + \frac{s}{\omega_{p1}}\right)(1 + s\, R_F\, C_C) + A_{dc}}$$

- $i_{sig}(t)$ can be modelled as a δ function (refer Simulation Environment section). Therefore,

$$v_{out}(t) = \frac{-C}{p_1 - p_2}\left[e^{-p_2 t} - e^{-p_1 t}\right]$$

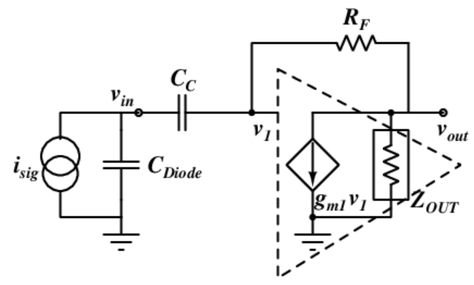


Fig 3: Equivalent model of the CSA to calculate closed loop transfer function.

Corner Control Circuit

- In single ended folded cascode amplifier, it is difficult to achieve reliable functionality across the process variations without compromising on power budget.
- To tackle this drawback, we predict the circuit operation at corners and provide a corrective measure to lift the gain whenever required.

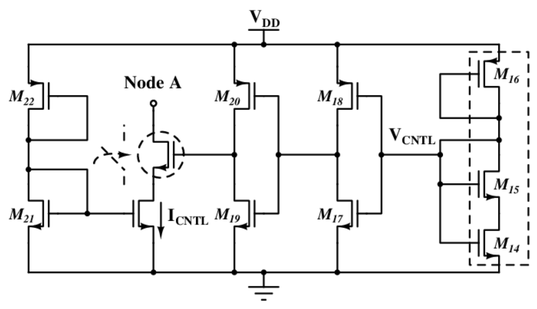


Fig 4: Corner tuning circuit used to obtain cross-corner functionality.

Current Injection Circuit

- When a charged particle crosses the depletion region, it generates a signal of 1000 e$^-$ to 20000 e$^-$ [3].
- A revere biased diode between the p-substrate and the deep n-well realizes the pixel sensor.
- Equivalent current can be injected at the cathode terminal of the diode using the dotted block in Figure 5(a) to simulate the behaviour of sensor and measure the response of its front end electronics.
- The relation between current pulse input and the number of electrons is

$$i_H \cdot t_W = n \cdot e^-$$

where, t_W is pulse width, i_H is the pulse height, e^- is the electron charge and n is the number of electrons.

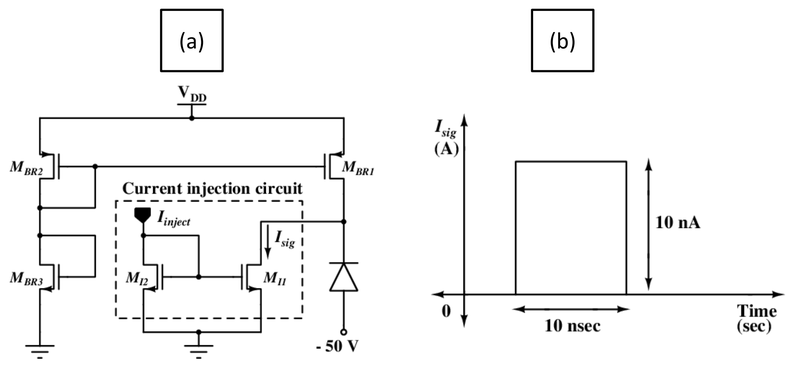
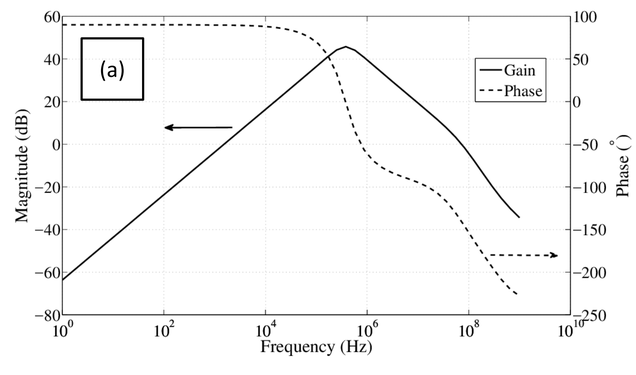
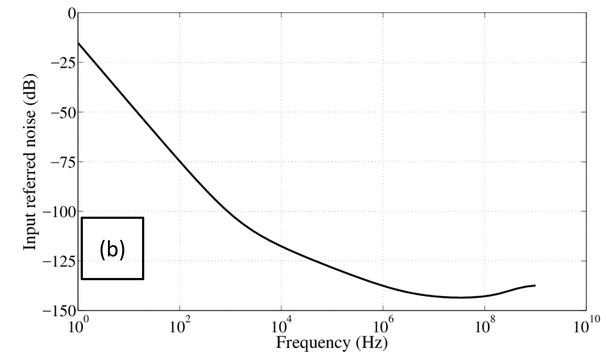


Fig 5: (a) The schematic of current injection circuit, (b) variable width injected current signal at the deep N well of the diode.

Layout and Simulation Results





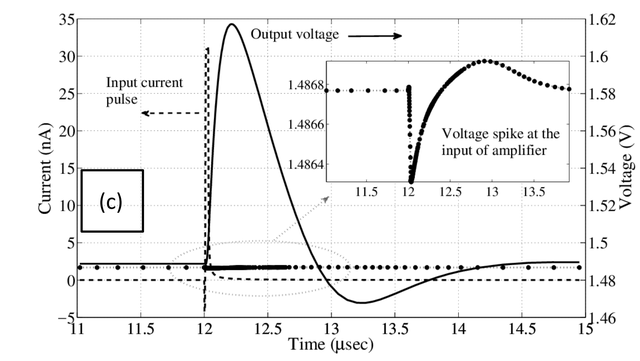


Fig 6: (a) Magnitude and phase response of the designed CSA, (b) input referred noise of the charge sensitive amplifier, (c) time response of the CSA when current pulse with amplitude of 30 nA and width of 30 ns is injected into the sensor.

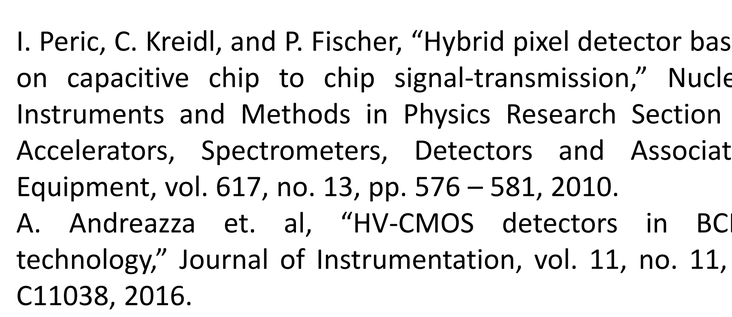


Fig 7: Layout of the CSA, Area: 65×25 µm^2

Table 1: Summary – CSA simulation results

Tech	Gain	BW	Noise	Current
BCD 180	45 dB	425 kHz	201 nV/√Hz	15.6 µA

Conclusions

- ✓ The design of analog signal processing circuit for 47 X 6 pixel detector is implemented in BCD 180 nm technology.
- ✓ The circuitry is designed to be compatible with front end I4 (FE-I4) chip of ATLAS experiment.
- ✓ Maximum fill factor is achieved by hosting the front end analog circuitry into the diode sensor area.
- ✓ The corner control circuit occupies 38 X 21 µm^2 area and reduces current consumption in the CSA from 30 µA to 15.6 µA per pixel.

References

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3. I. Peric, "A novel monolithic pixel detector implemented in high-voltage CMOS technology," in IEEE Nuclear Science Symposium Conference Record, vol. 2, Oct 2007, pp. 1033–1039.