MAPS sensor for radiation imaging

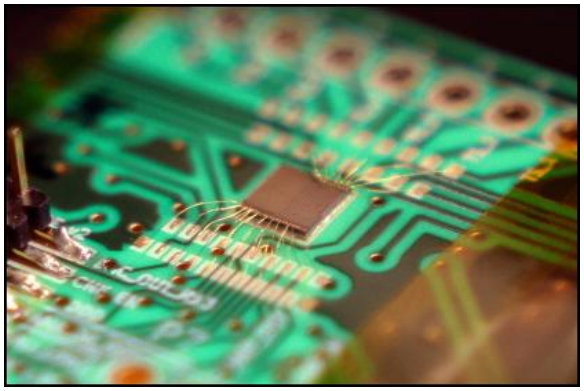
designed in 180 nm SOI CMOS technology

Tomas Benka[1], **Miroslav Havranek[1]**, Martin Hejtmanek[1], Zdenko Janoska[1], Jaromir Kopecek[2], Mahulena Kuklova[1], Maria Marcisovska[1], Michal Marcisovsky[1], Gordon Neue[1], Peter Svihra[1], Lukas Tomasek[1], Vaclav Vrba[1]

[1] **Faculty of Nuclear Sciences and Physical Engineering of the Czech Technical University**

[2] **Institute of Physics of the Czech Academy of Sciences**

3rd July 2017, iWoRiD 2017, Krakow, Poland



Email: miroslav.havranek@fjfi.cvut.cz

Outline

- Technology introduction
- Parameters of the chip
- SOI pixel
- Pixel design and simulations
- Measurement results

Poster 1: **M. Kuklová,** *Radiation Imaging with a SOI-based Monolithic Pixel Chip,*
poster session 05/07/2017, B21

Poster 2: **T. Benka**, *Characterization of pixel sensor designed in 180 nm SOI CMOS technology*,
poster session 03/07/2017, B16

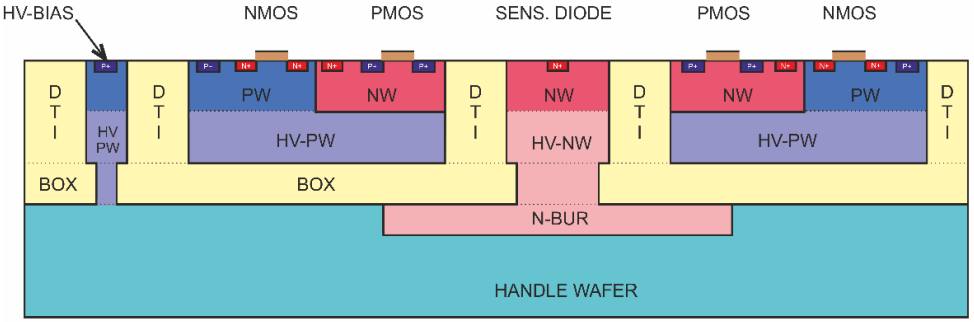
Technology introduction

- **SOI – Silicon on Insulation – “non-traditional”**
- **Non-depleted EPI-layer**
- **Medium resistivity handle wafer**
- **Deep submicron CMOS process**
- **High voltage compatible**

Technology choice inspired by:

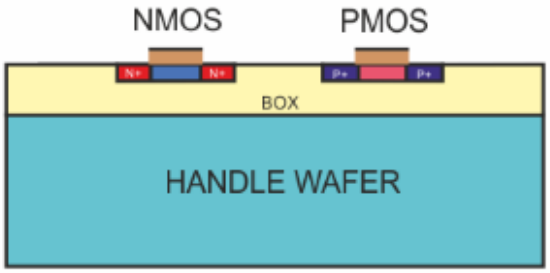
[1] T. Hemperek et al. A Monolithic active pixel sensor for ionizing radiation using a 180 nm HV/SOI process, arXiv:1412.3973

non-depleted SOI CMOS process



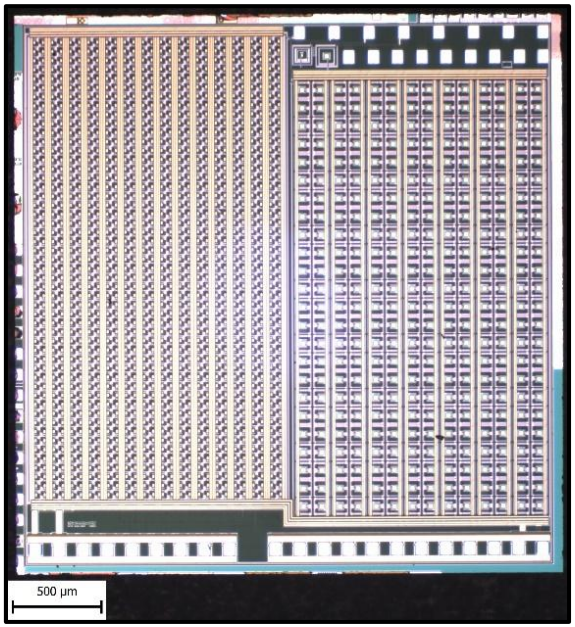
- **What does it mean for MAPS sensor:**
  - larger depleted zone (30 µm) @ 100 V → larger signal
  - sensing diode does not consume pixel area
  - full CMOS FE in pixel
  - substrate noise immunity
  - SEU immunity

FD SOI

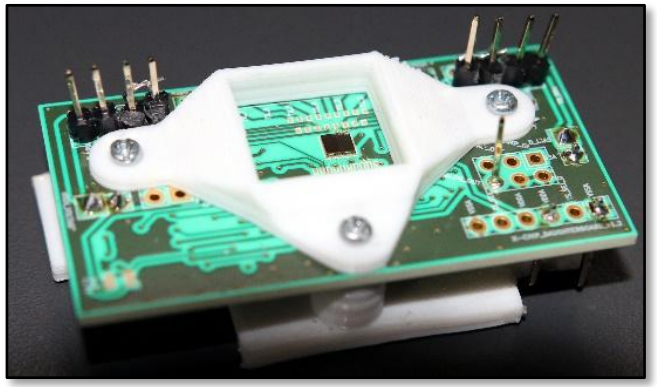


X-CHIP-02

- **Two pixel matrices:** 50 µm and 100 µm
- **Matrix dimensions:** 28×51 resp. 14×24 pixels
- **Sensitive area:** 1.4×2.55 resp. 1.4×2.8 mm^2
- **Chip thickness:** 300 µm (partially depleted)
- **Process:** 6-metal 180 nm SOI-CMOS process
- **Core voltage:** 1.8 V
- **Sensor bias voltage:** -100 V
- **Design complexity:** 880 000 transistors

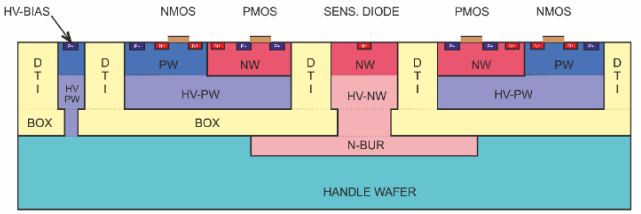


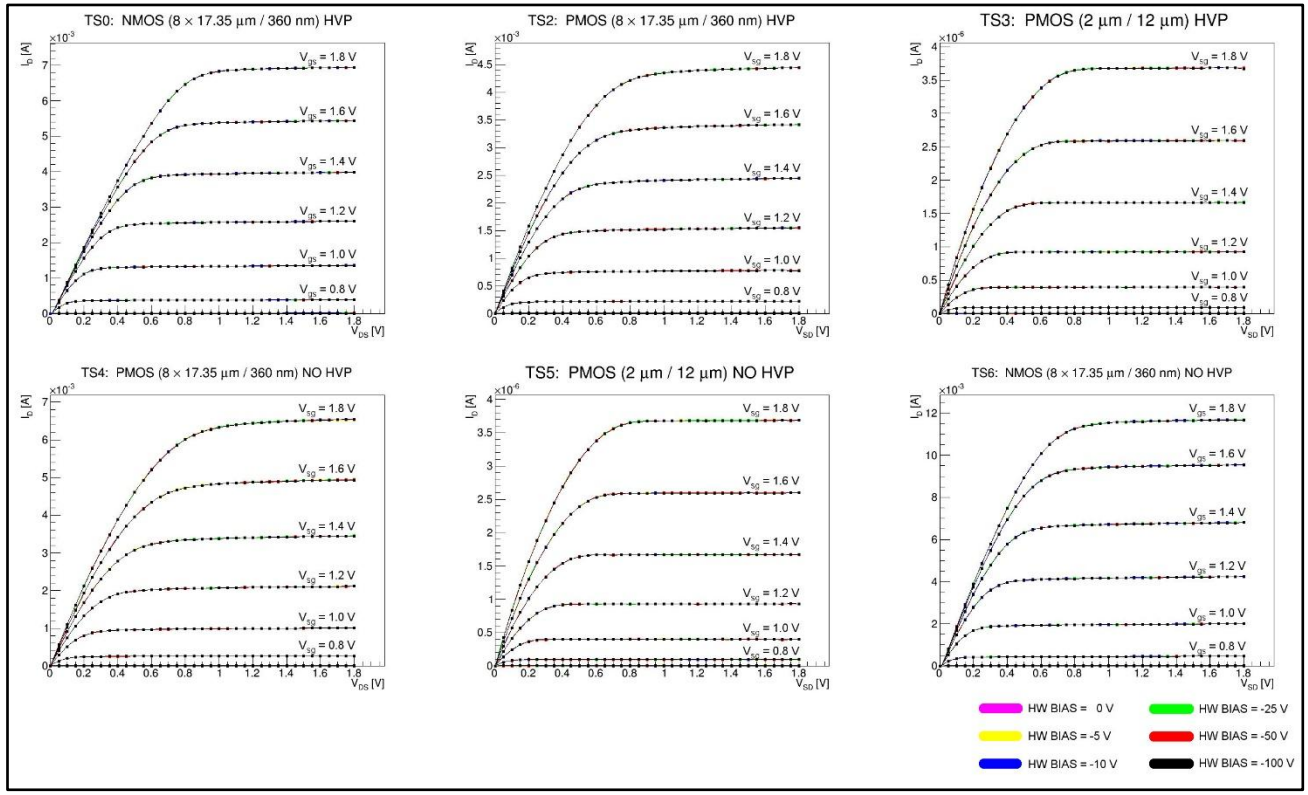
Test-pcb with X-CHIP-02

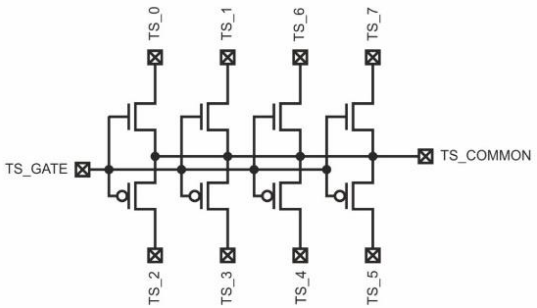


Transistors (measurement)

- Non-depleted SOI does not suffer from back-gate effect
- Possibility to bias HW without influencing pixel electronics
- Radiation tolerance (?) → see poster of **T. Benka**







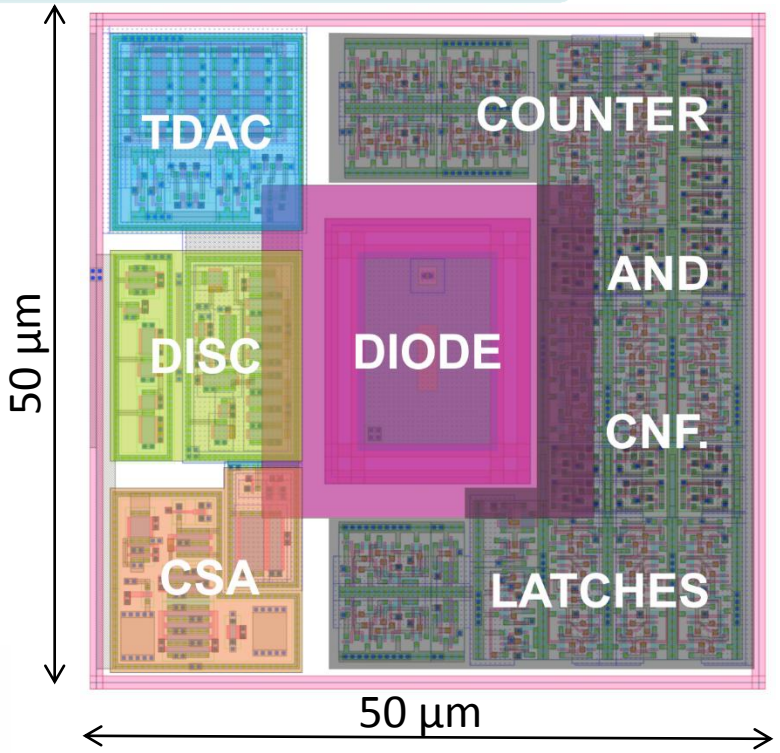
TS	Dimensions (W/L)	Type	HVP
0	17.35 µm × 8 / 360 nm	NMOS	YES
~~1~~	~~2 µm / 12 µm~~	~~NMOS~~	~~YES~~
2	17.35 µm × 8 / 360 nm	PMOS	YES
3	2 µm / 12 µm	PMOS	YES
4	17.35 µm × 8 / 360 nm	PMOS	NO
5	2 µm / 12 µm	PMOS	NO
6	17.35 µm × 8 / 360 nm	NMOS	NO
~~7~~	~~2 µm / 12 µm~~	~~NMOS~~	~~NO~~

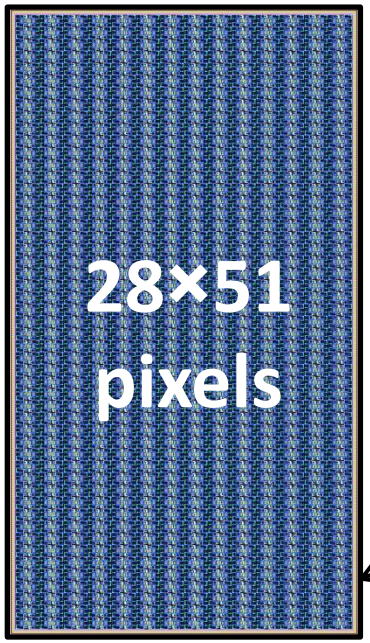
broken gate (ESD)

50 µm pixel design

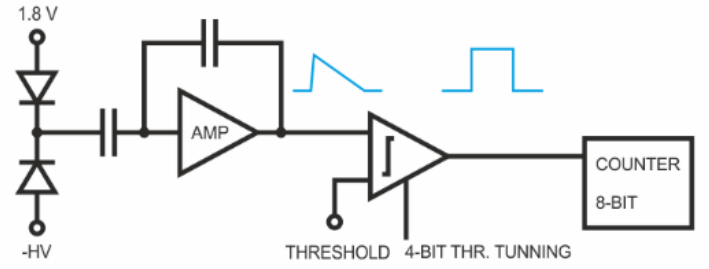
- MAPS with "*hybrid pixel like*" FE electronics
- 526 transistors per pixel
- Each pixel has "private" substrate
- Analog front-end + 8-bit hit-counter

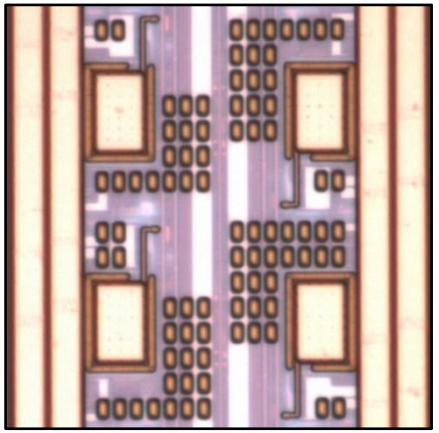
  - power consumption: 5.2 µW





common bias ring of the handling wafer



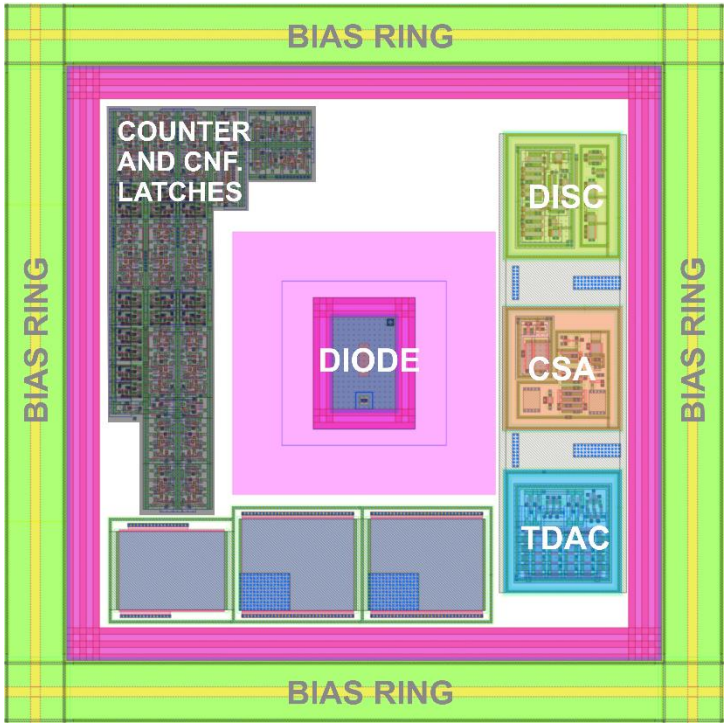


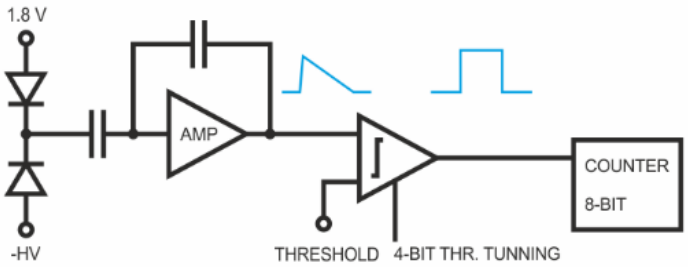
micrograph of 2×2 pixels

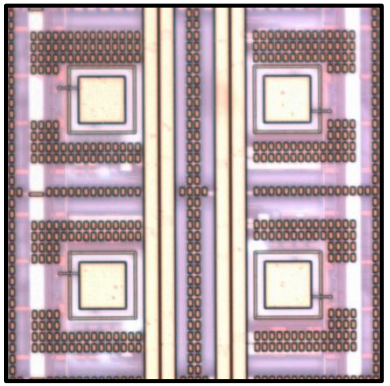
100 µm pixel design

- Pixel electronics almost identical with 50 µm pixels
- Local bias-ring
- Different coupling capacitor size:

  238 fF (50 µm pixel) vs. 642 fF (100 µm pixel)



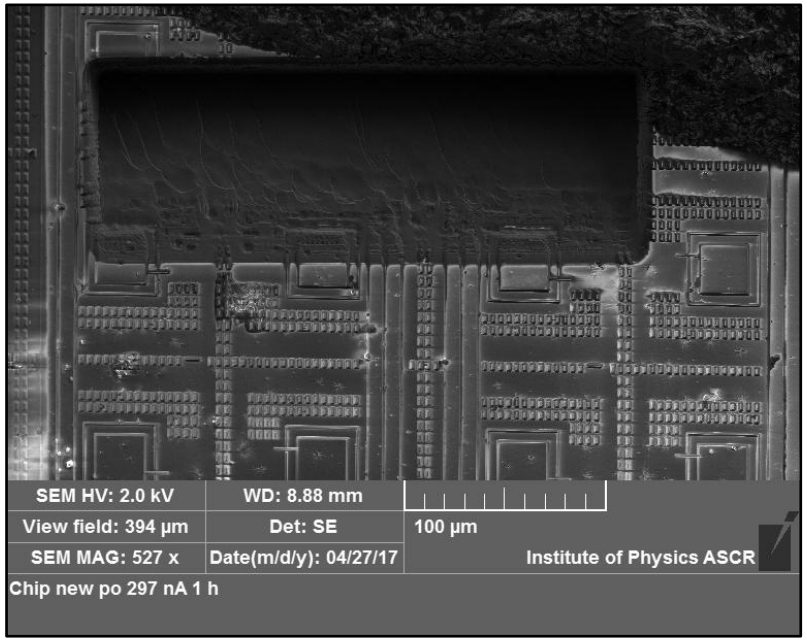


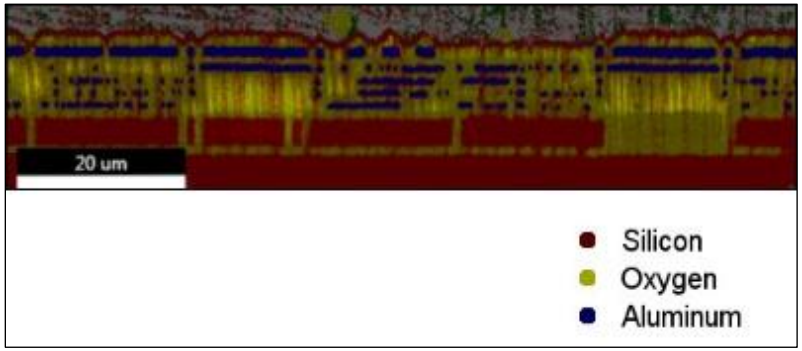


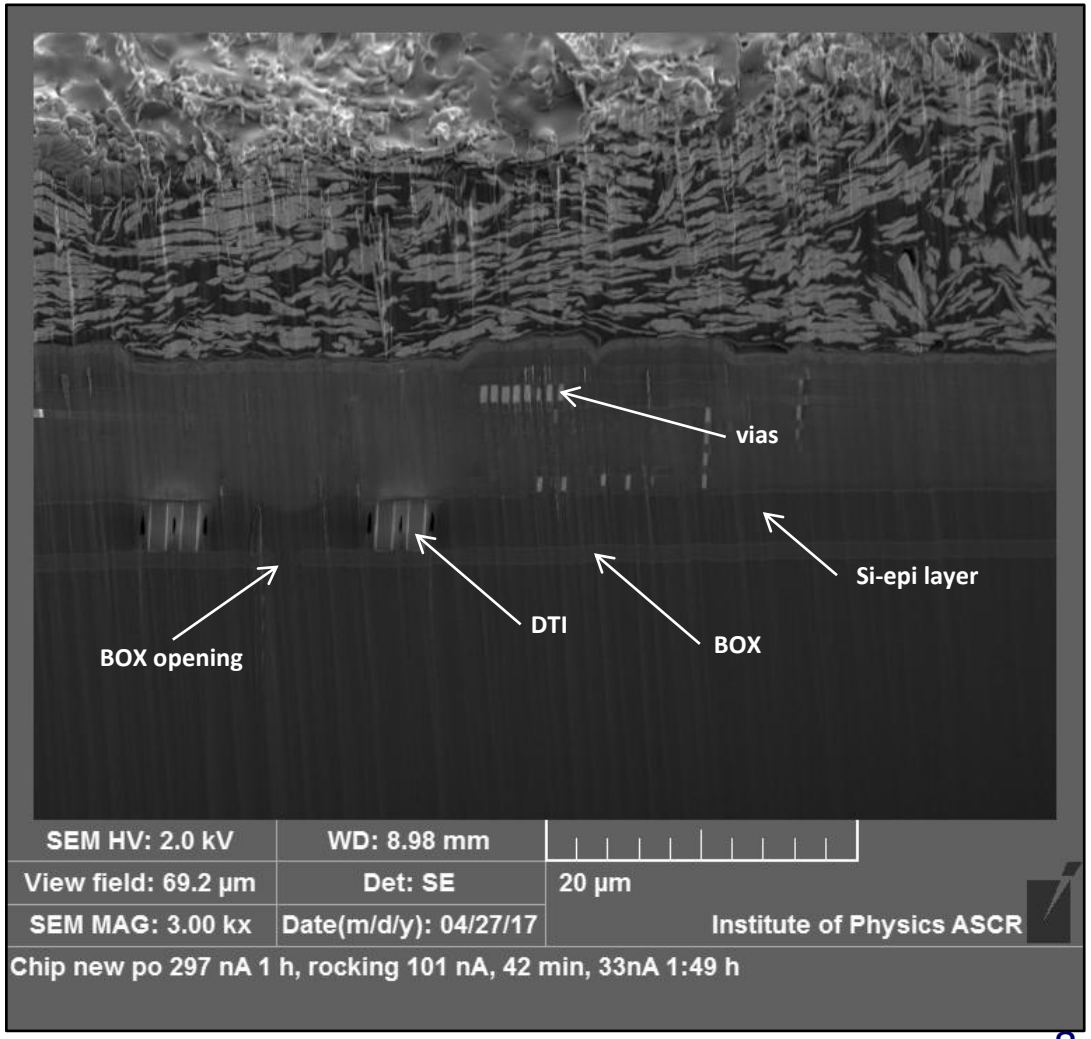
micrograph of 2×2 pixels

X-CHIP-02 disassembled

- Surface layers excavated by Focused Ion Beam (Xenon atoms)





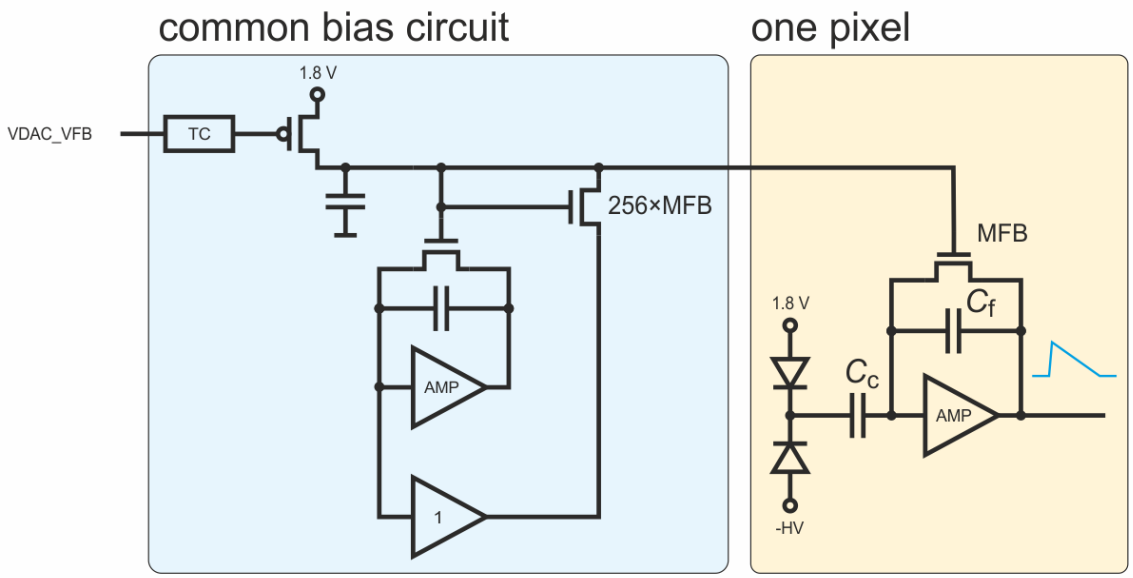


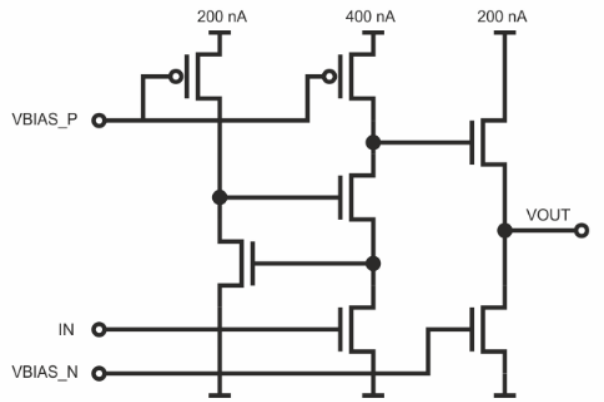
Pictures made by J. Kopecek, IoP ASCR

Analog front-end – a closer look I.

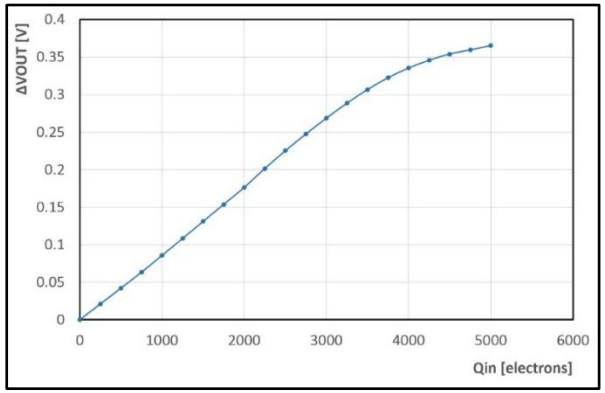
- **Charge Sensitive Amplifier (CSA):**

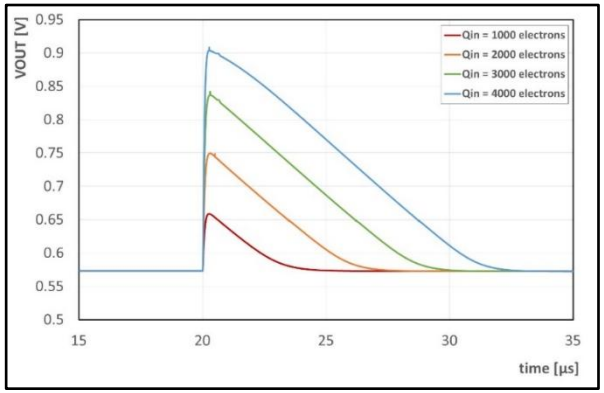
core amplifier („AMP”)

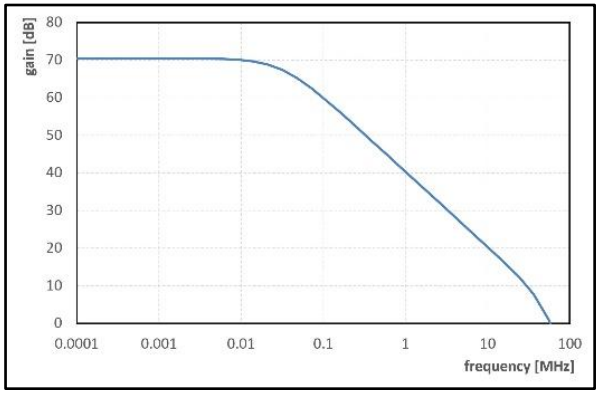




Power consumption: 1.4 µW
Gain (cl): 90 µV/e$^-$
Gain (ol): 70.4 dB (3300)
Peaking time: 150 ns (at 2 ke$^-$)

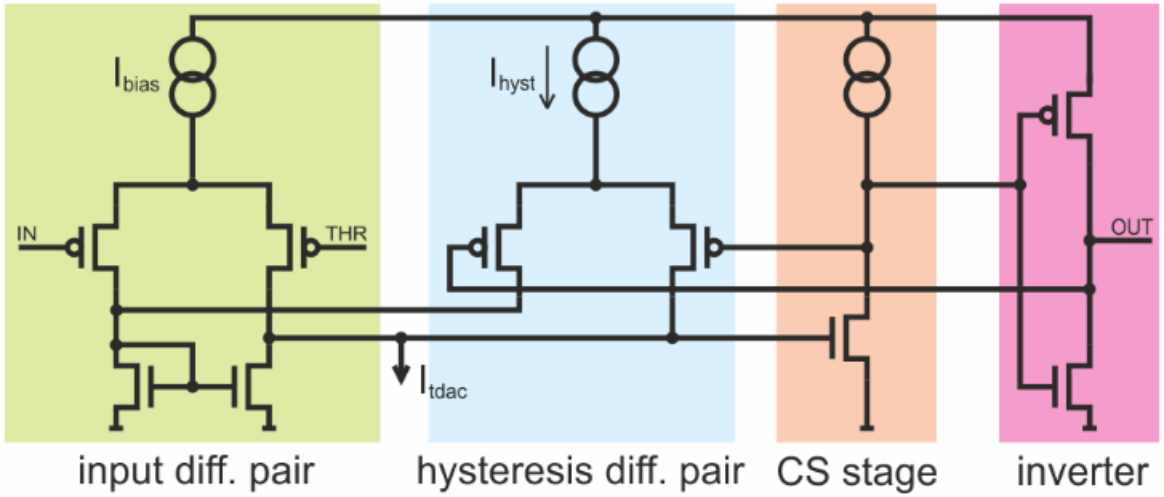




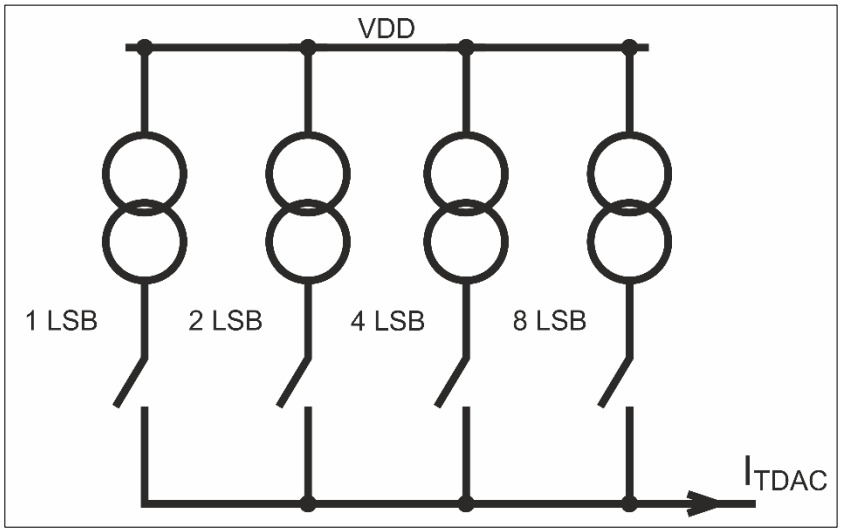


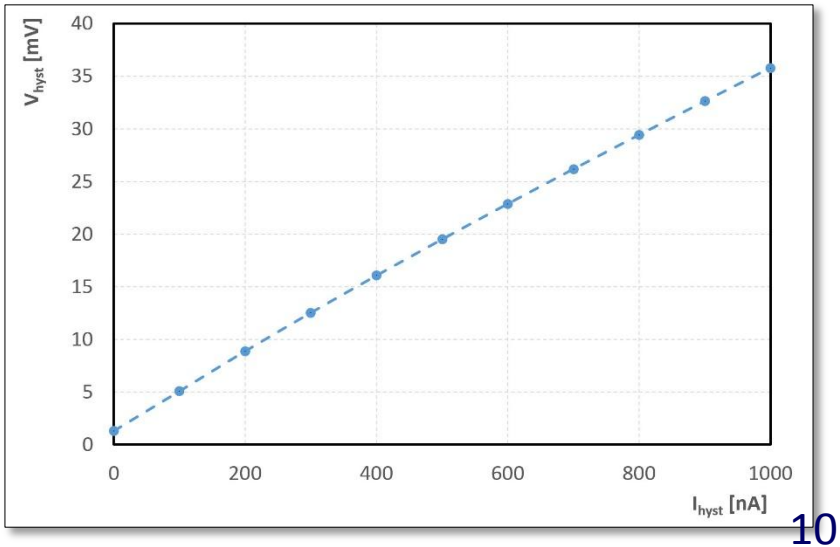
Analog front-end – a closer look II.

- **Comparator with hysteresis and TDAC**
- **Parameters:**
  - **- power** = 3.8 µW
  - **- offset:** µ = 3.1 mV
    σ = 7.74 mV
  - **- hysteresis** adjustable
  - **- delay** = 60 ns



- **Current steering TDAC**





Electronic noise simulation in time domain

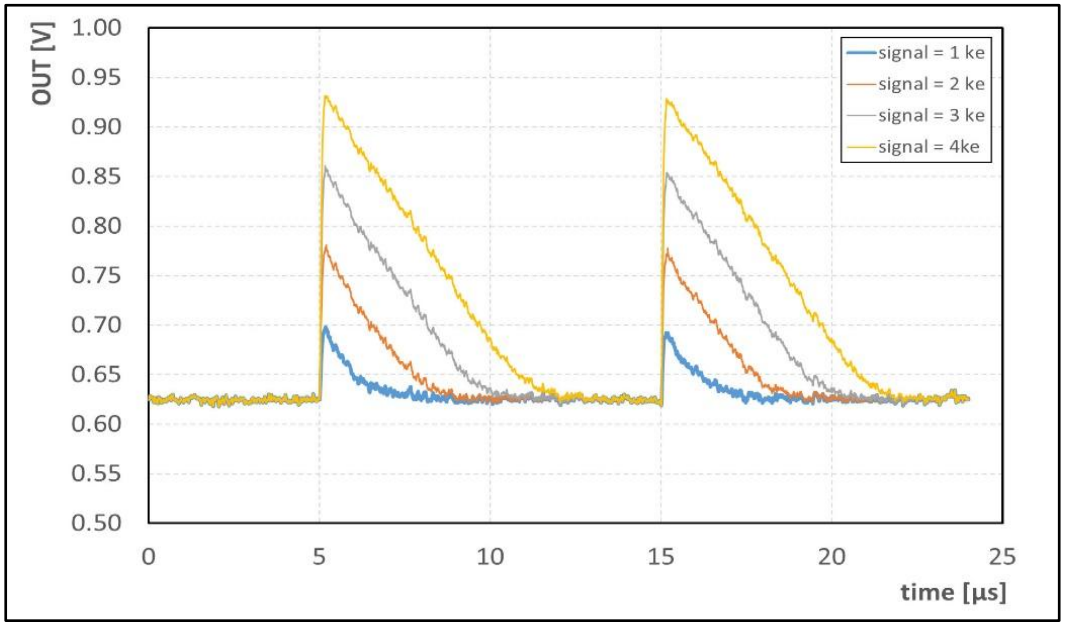
- **Electronic noise depends on many parameters**
- **Noise simulation in time domain as a function of:**

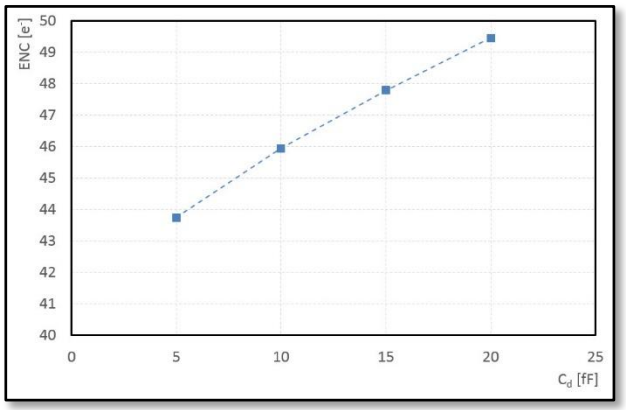
  - sensor capacitance (C_d)

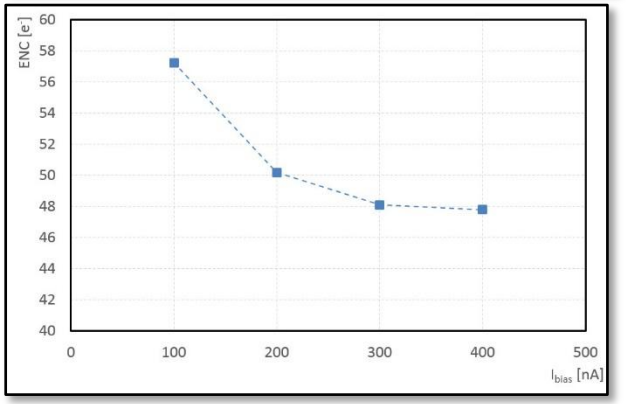
  - bias current of the CSA (I_{bias})

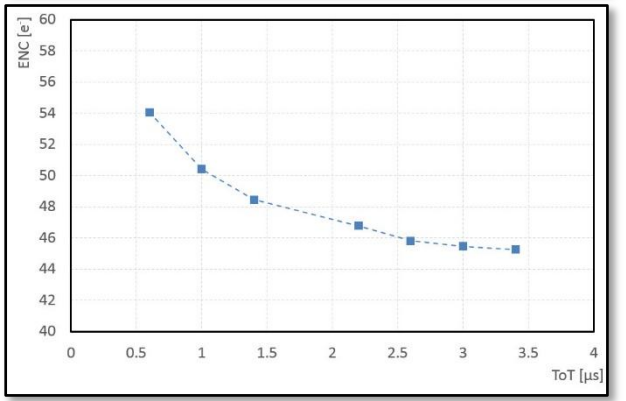
  - discharge rate of the CSA

  (ToT at threshold = 500 e^-, signal 1000 e^-)



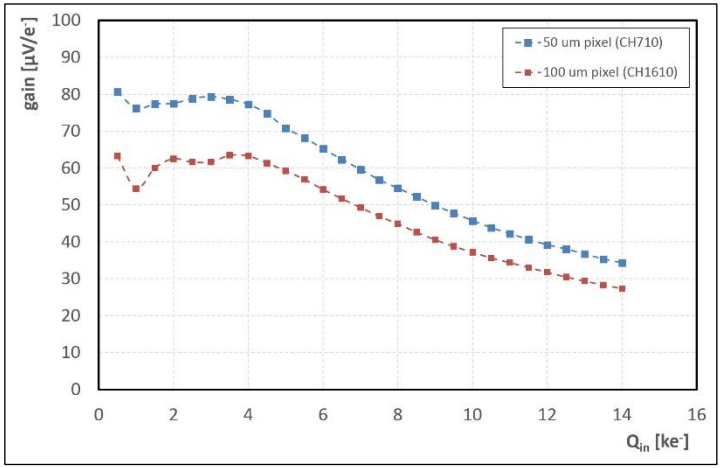






Electronic noise measurement

- ENC is always present: ENC ~ C_d ~ pixel size
- Noise determination from analog output



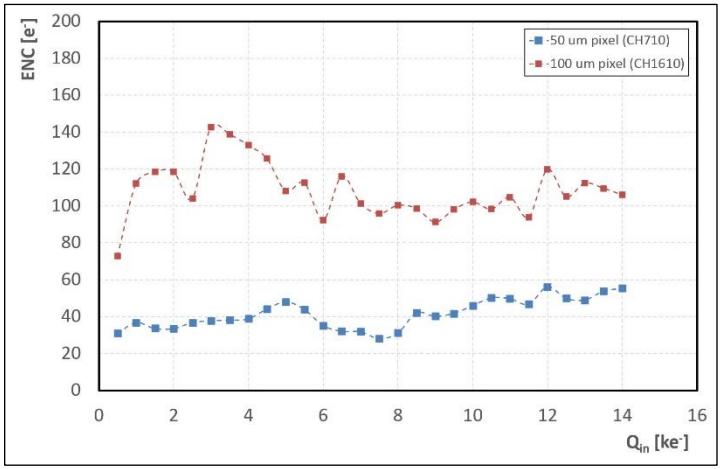
$$a_{\mathrm{CL}} = \frac{1}{C_\mathrm{f}} \cdot \frac{1}{\frac{1}{a_{\mathrm{OL}}} \cdot \frac{Cd}{a_{\mathrm{OL}} \cdot C_\mathrm{f}}}$$

a_{CL}.... closed loop gain

a_{OL}.... open loop gain

C_f.... feedback capacitance

C_d.... sensor capacitance



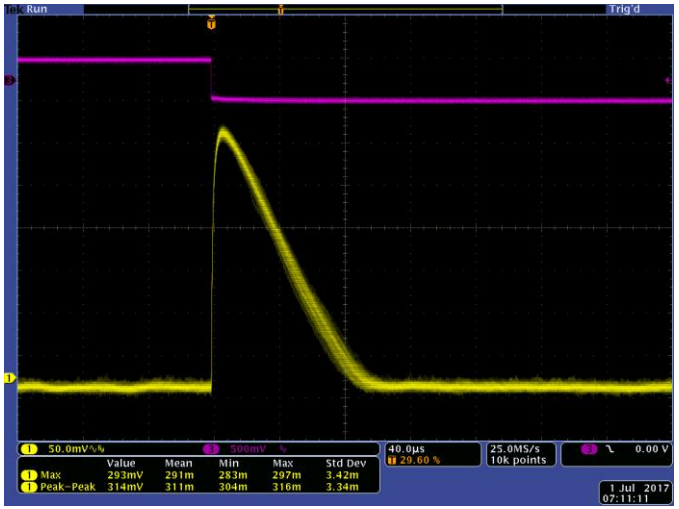
FD Hybrid pixel sensor:

C_d ~ pixel circumference

PD MAPS:

C_d ~ pixel area

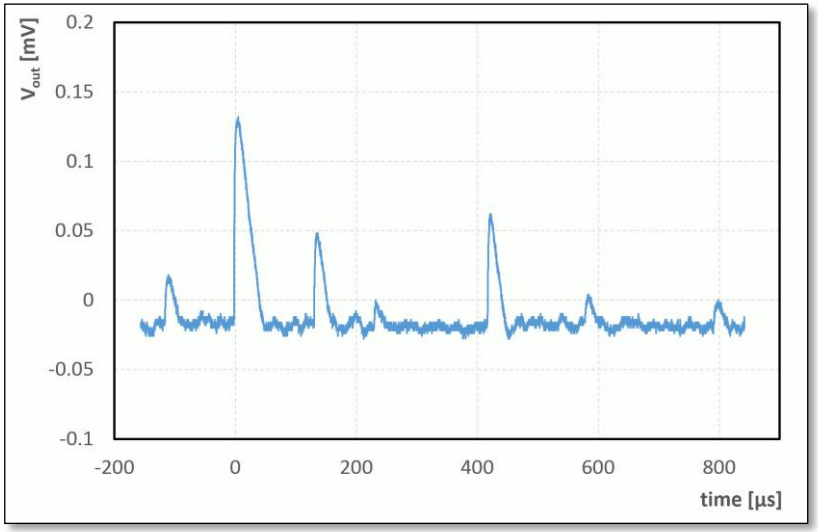
4 ke⁻ charge injection to 50 µm pixel



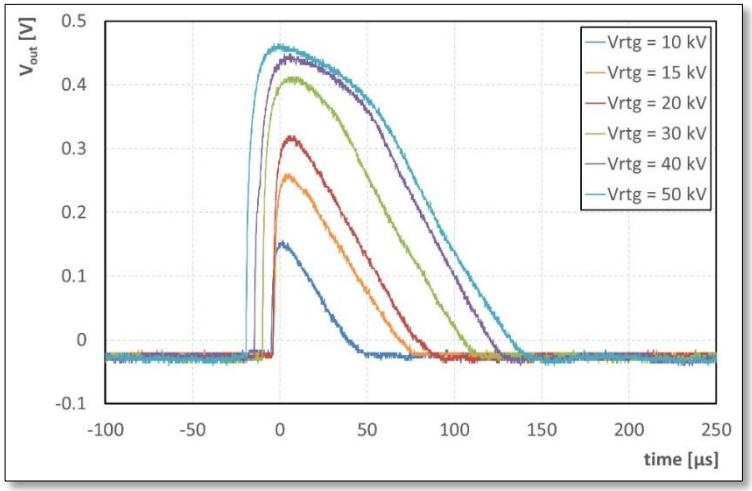
4 ke⁻ charge injection to 100 µm pixel

First light to X-CHIP

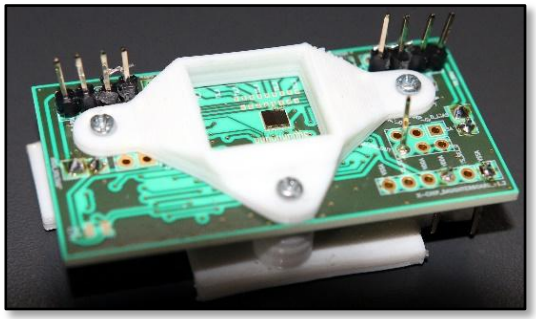
- Response to X-RAY radiation



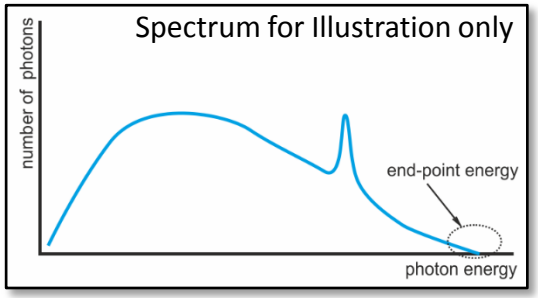
signal from “end-point” photons



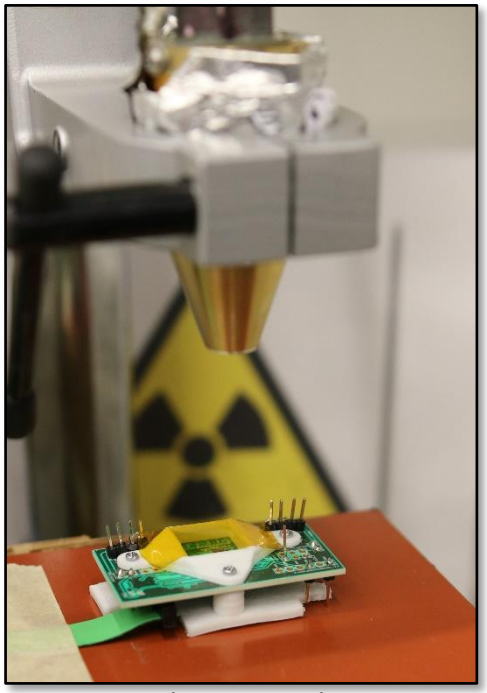
pcb with X-CHIP-02



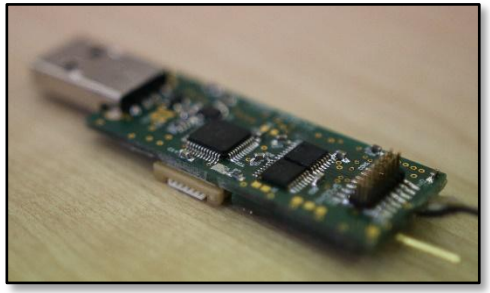
V_{rtg} [kV]	Q_{signal} [ke$^-$]	ΔV_{out} [mV]
10	2.74	179.5
15	4.11	283.1
20	5.48	318.8
25	6.75	398.2
30	8.22	438.4
35	9.59	462.9
40	10.96	458.2
45	12.33	475.8
50	13.70	490.9



X-RAY source 10-50 kV, max 200 µA, Ag anode, Be window



SURE – Simple USB Readout Equipment

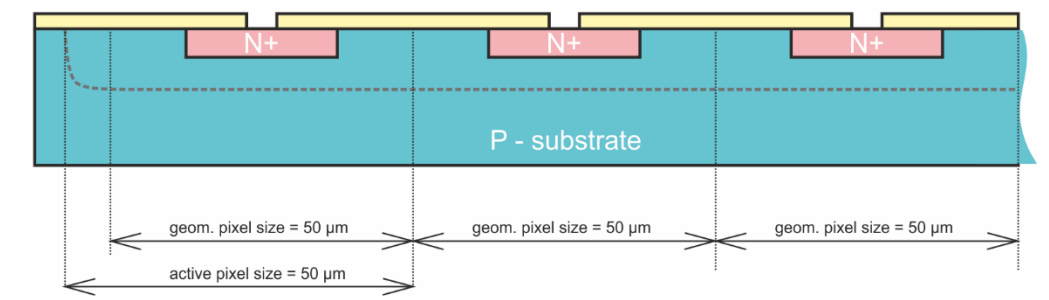


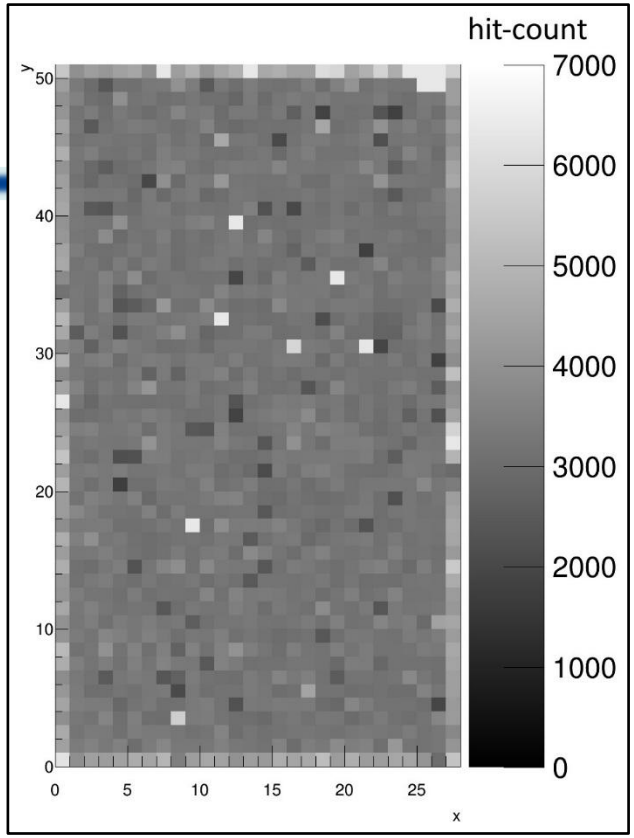
Border effect

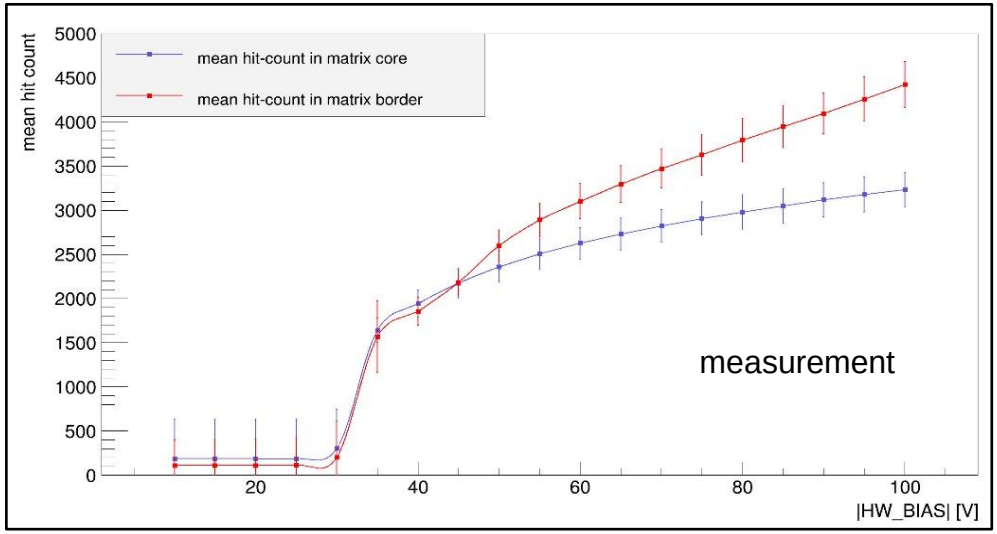
- Pixels along along the edge give more hits compared to pixels inside the matrix

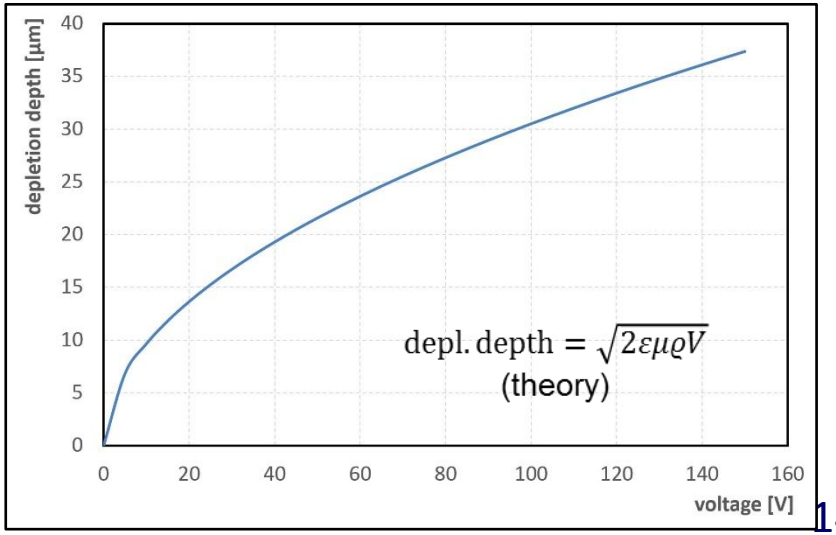
  => border effect

  => sign of large (possibly 100 %) fill factor



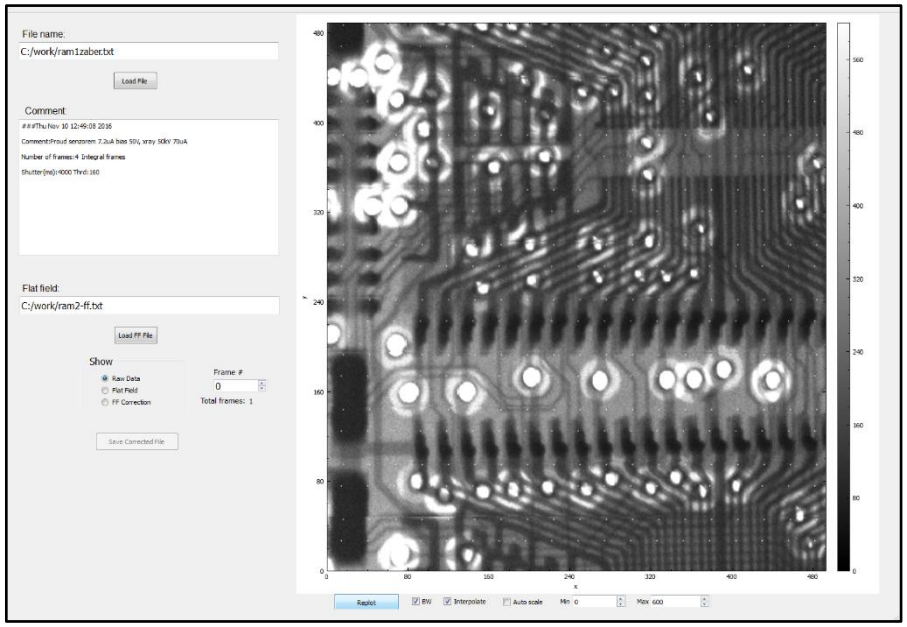


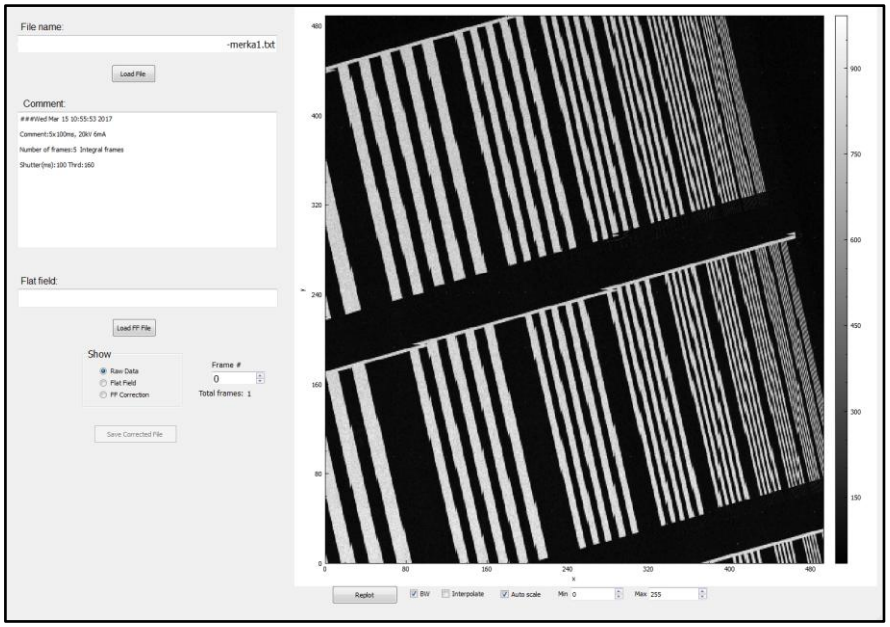


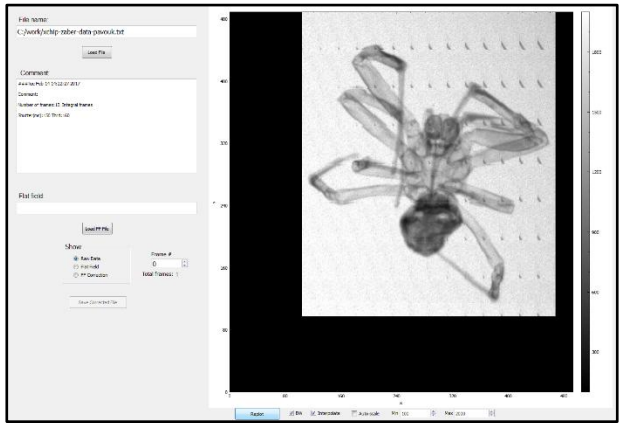


First images

- X-CHIP mounted on moving table => area of about 2×2 cm^2 can be scanned







- Small chip area overcame by moving table
- Small dynamic range overcame by integration of several frames

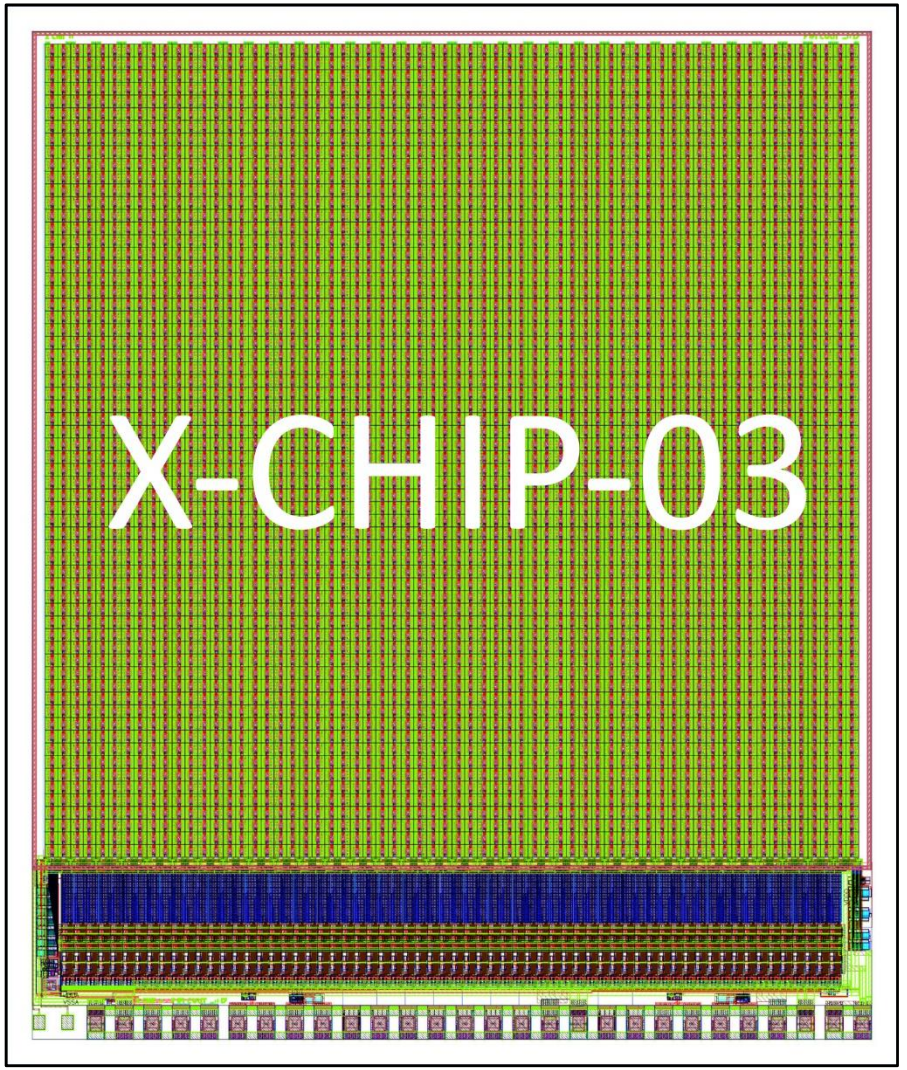
This chip is already applicable for basic radiation imaging tasks

Future development

- **Limitations of X-CHIP-02:**
  - slow read-out (2 FPS)
  - small dynamic range (8-bits)
  - hit counting only

- **New version → X-CHIP-03:**
  - pixel matrix 64×64 pixels (3.84×3.84 mm^2)
  - fast read-out (≈400 FPS)
  - large dynamic range (16-bits)
  - hit counting mode
  - ADC mode
  - complexity 3.6 mil. transistors

Design submitted in May 2017



Acknowledgement

- **Plenty of work done in short time**
  - chip design
  - PCB design
  - USB read-out SURE
  - SURE firmware
  - control software
  .
  .
  .
- **I would like to thank to my colleagues for help to work on this project**

This project has been supported Technology Agency of the Czech Republic under project number: TE01020069

Email: miroslav.havranek@fjfi.cvut.cz

Thank you for your attention

Email: miroslav.havranek@fjfi.cvut.cz