

Katherine: Ethernet Embedded Readout Interface for Timepix3



19th International Workshop on Radiation Imaging Detectors

P. Burian^{a,b}, P. Broulim^a, V. Georgiev^a, M. Jara^a and B. Bergmann^b

^a Faculty of Electrical Engineering, University of West Bohemia, Univeritni 26, Pilsen, Czech Republic

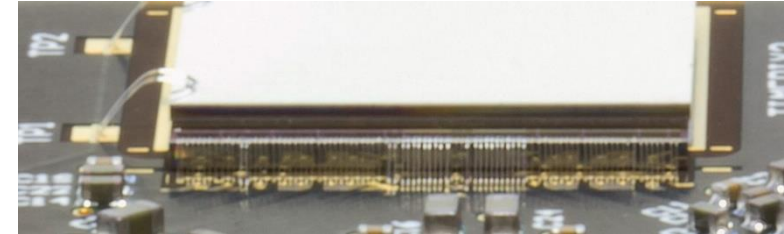
^b Institute of Experimental and Applied Physics, Czech Technical University in Prague, Horská 3a/22, Prague, Czech Republic

Outline

- ▶ Timepix3 – Fundamental Description
- ▶ Motivation
- ▶ Description of readout device
 - ▶ Fundamental Features
 - ▶ Interfaces
 - ▶ Communication
 - ▶ Software support
- ▶ Demonstration of usage
- ▶ Summary

Timepix3 – Fundamental Description

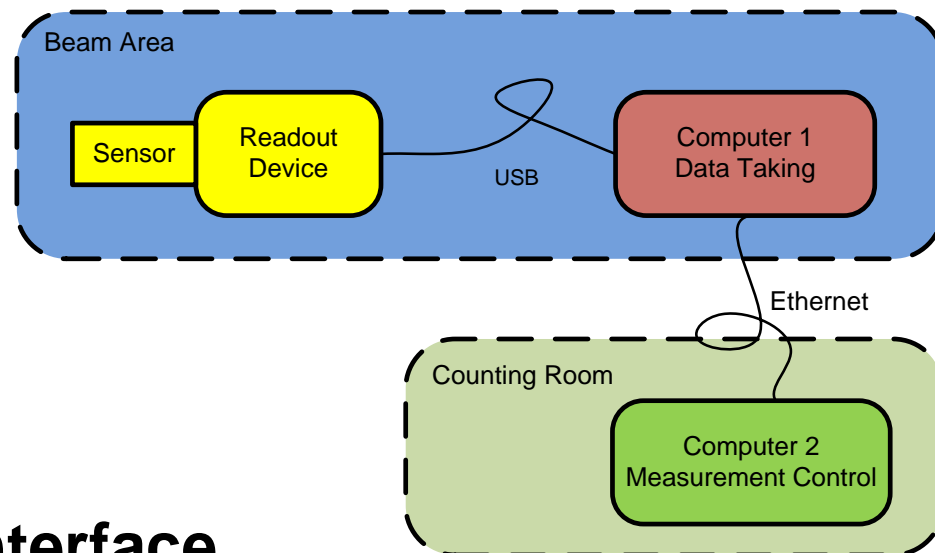
- ▶ Hybrid pixel detector
- ▶ Resolution 256x256 pixels; pixel pitch 55 μ m
- ▶ Developed within Medipix3 Collaboration, CERN
- ▶ Designed in 130nm CMOS technology
- ▶ **Measuring ToT (energy) and ToA (time-stamping) simultaneously**
- ▶ ToA measurement:
 - ▶ Coarse ToA clock = 40MHz => 25 ns
 - ▶ **Fine ToA clock = 640MHz (ring oscillator) => 1.56ns**
 - ▶ Global time stamp range 14 bits => 409.6 μ s
- ▶ **Readout modes:**
 - ▶ **Frame-based mode with zero-suppressed (max ~1300 fps)**
 - ▶ **Data-driven mode (~40Mhits/s); dead time per pixel min. 475ns**
- ▶ Acq. modes: ToA & ToT, Only ToA, Event Count & Integral ToT
- ▶ Output data: up to 8 serial lines @ 640MHz => max. data rate = 5.12 Gbps



Motivation

▶ Why Gigabit Ethernet interface?

- ▶ Standard setup with USB readout
=> computer in beam area



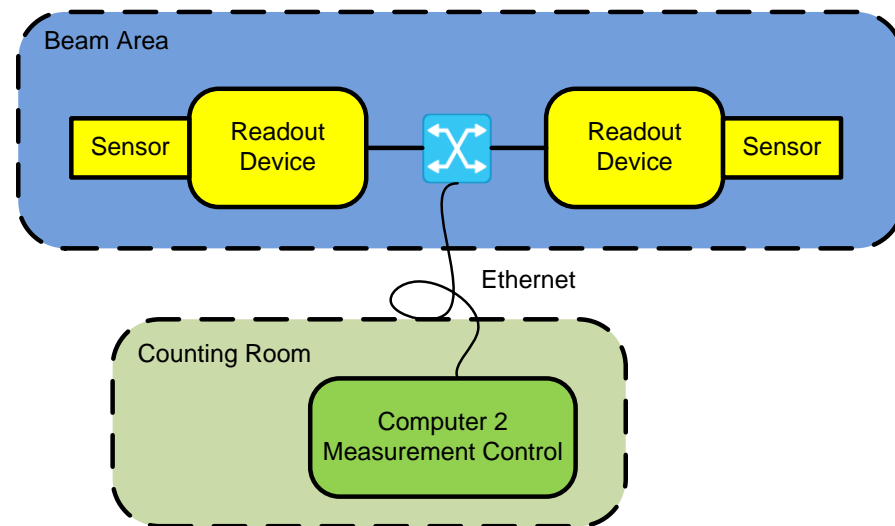
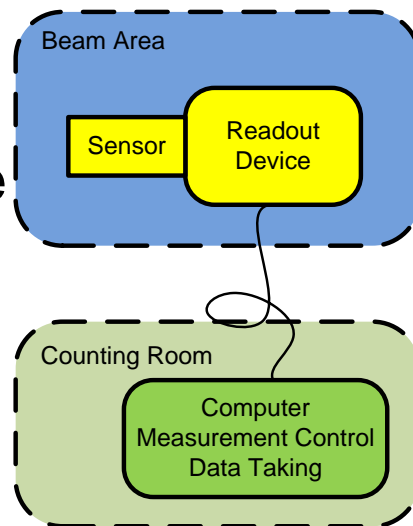
▶ Readout with Gigabit Ethernet interface

▶ Pros:

- ▶ Long distances
- ▶ Independent device

▶ Cons:

- ▶ Limited hit rate
- ▶ Ethernet ports



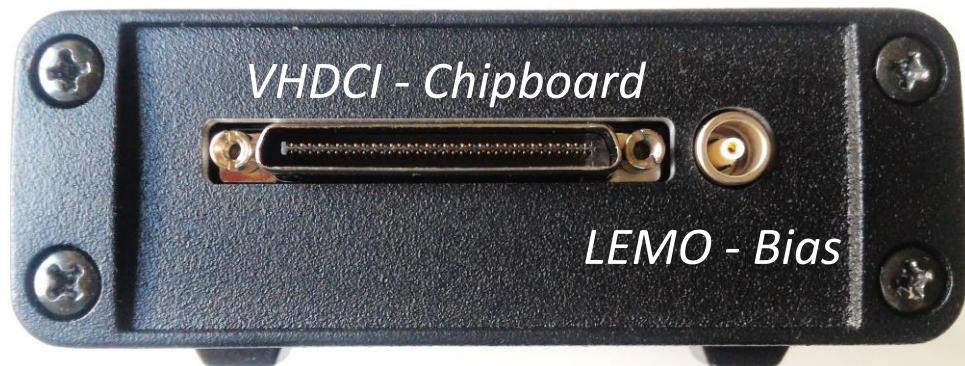
Katherine – Features

- ▶ Embedded computer + interface for one Timepix3 (CERN chipboard)
- ▶ Optimized for long distance between sensor and readout
- ▶ Source of high voltage for bias – both polarities ($\pm 300\text{V}$)
- ▶ Gigabit Ethernet Interface => max. 15Mhits/s
- ▶ Long-distance access (up to 100m)
- ▶ Dimension: roughly 100x80x28



Katherine – Interfaces

- ▶ VHDCI connector
 - ▶ Direct connection of chipboard or VHDCI extending cable
- ▶ Power supply DC 5V
- ▶ Bias voltage – LEMO connector – voltage range $\pm 300V$
- ▶ Status LED diodes (programmable by user)
- ▶ GPIO port – purpose of signals defined by control SW
 - ▶ 1x single-ended input (possible to use as external clock)
 - ▶ 1x single-ended BiDir signal
 - ▶ 1x LVDS input, 1x LVDS output

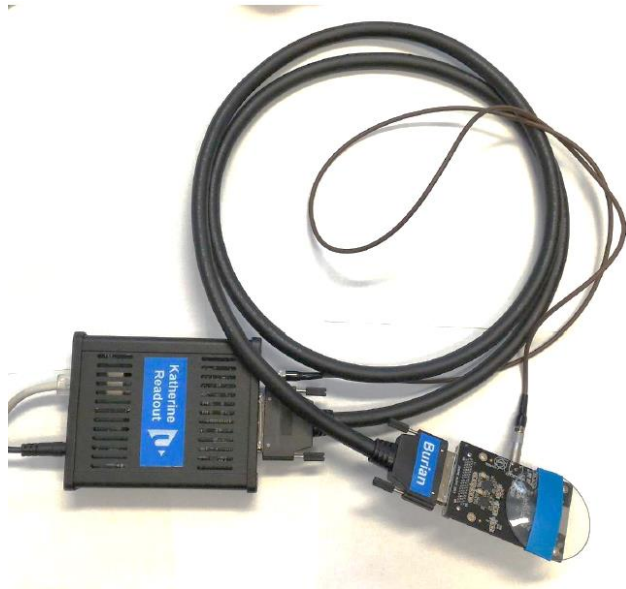


Katherine – Communication

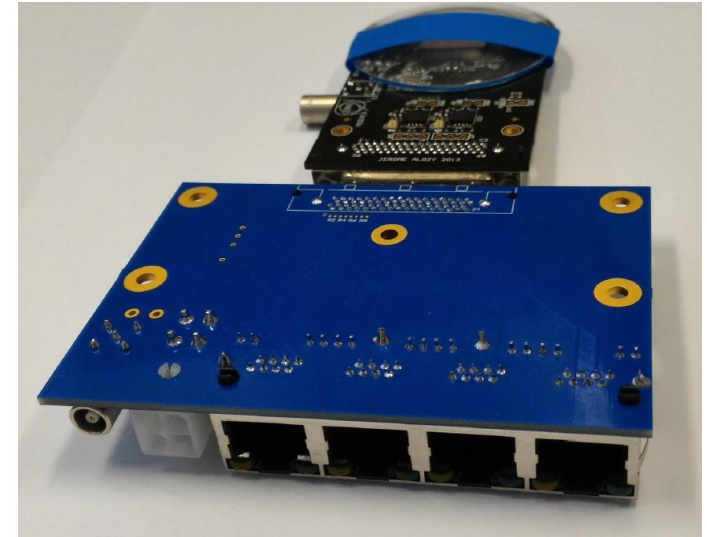
- ▶ Communication with sensor:
 - ▶ Two “fast” lines (2x 640Mbs)
 - ▶ Embedded clock
 - ▶ Direct connection with chipboard
 - ▶ Shorter distance via VHDCI cable (max. approx. 3.5m)
 - ▶ Hit rates: up to 20Mhit/s (but limited by Gigabit Ethernet bottle-neck)
 - ▶ Four “slow” lines (4x 160Mbs, 4x 80Mbs or 4x 40Mbs)
 - ▶ Longer distance between readout and chipboard
 - ▶ Verified: 10m VHDCI cable at 4x160Mbs rate
 - ▶ Hit rates: up to 10Mhit/s
 - ▶ Automatic setting of maximal speed according to used cable during power-up sequence
- ▶ Communication with computer/server:
 - ▶ Peer-to-peer communication with computer (based on UDP datagrams; TCP/IP in development)
 - ▶ 36 control/status commands
 - ▶ Automatic/independent sending data to server (via SSH connection)

Katherine – Communication

- ▶ How to connect sensor...
 - ▶ Directly (CERN chipboard)
 - ▶ Extending VHDCI cable



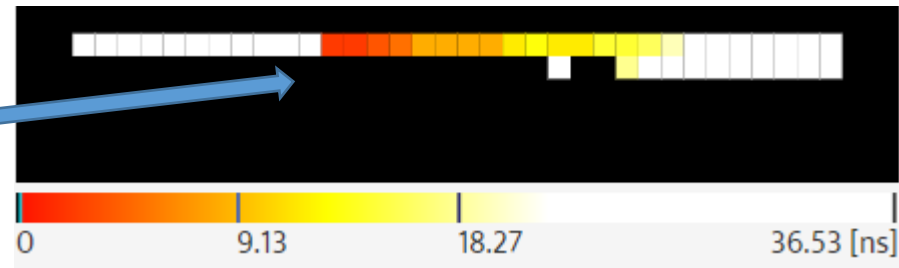
- ▶ Active or passive ethernet cabling extenders
 - ▶ Up to 100m distance between sensor and readout
 - ▶ 20m => no decreasing in speed
 - ▶ Radiation hardness solution
 - ▶ New rad. hard. chipboard



Katherine – Other Features

▶ Automatic correction of corrupted ToA timing

- ▶ Bug in Timepix3 ASIC chip
- ▶ Column 192 and its neighbourhood
- ▶ ToA counter shifted about 25ns
- ▶ Using testpulses during power-up sequence
- ▶ “On-line“ correction directly in readout device
- ▶ Choice of user



▶ ToA overflow in data-driven mode

- ▶ Coarse ToA counter overflow period = 409.6 μ s
- ▶ The device adds 32 extra bits for time-stamping
- ▶ Overall 50-bit (32 extra, 14 ToA, 4 fToa) time-stamping => overflow period is ~20 days

▶ All data from Timepix3 are decoded from LFSR and Gray to binary code in the device

▶ Enough computing power for user purpose:

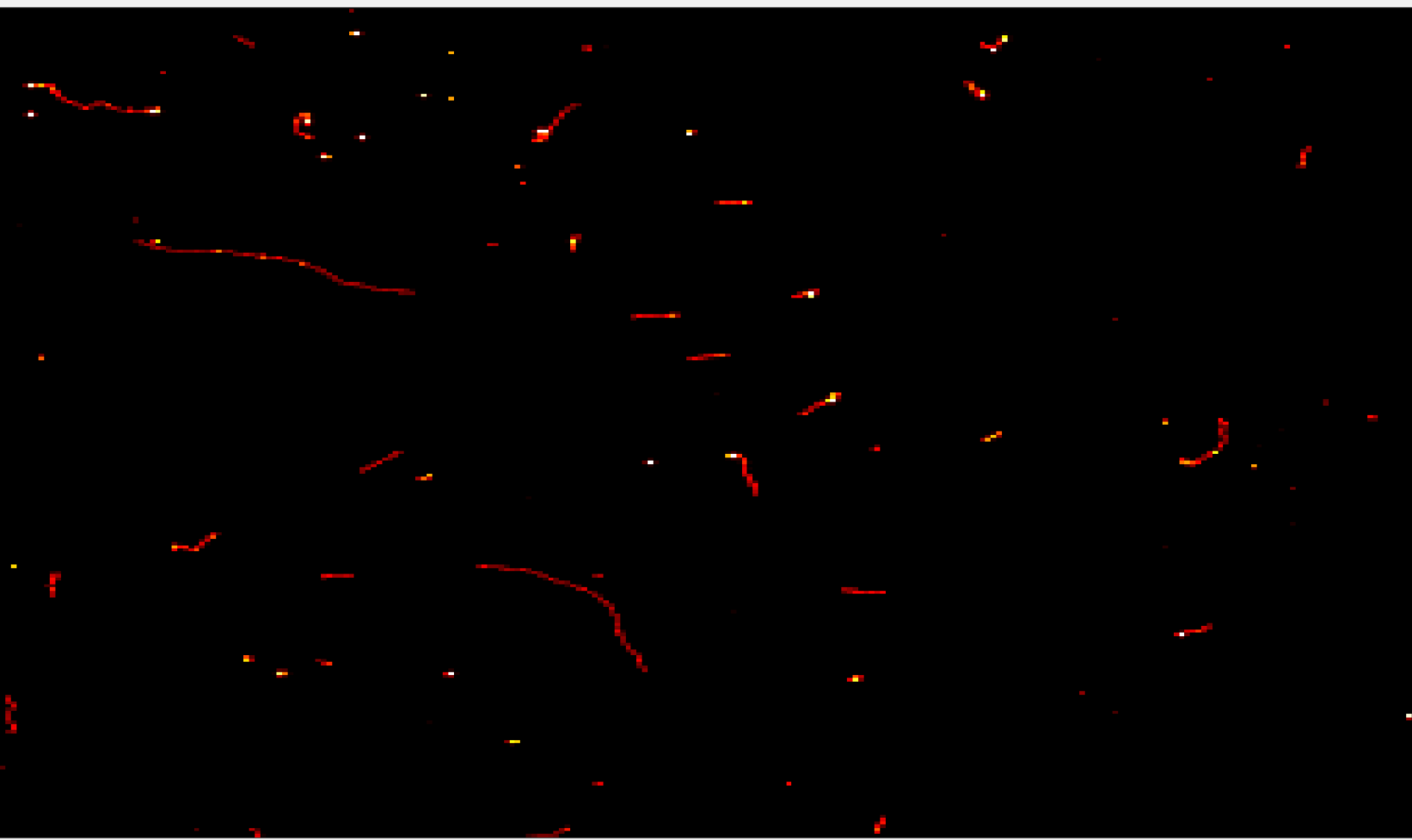
- ▶ Approximately 8000 ALMs in FPGA free to use
- ▶ Dual-core ARM Cortex-A9 processor
- ▶ 1GB DDR3 RAM

Katherine – Software support

- ▶ Completely new software tool was developed
- ▶ No support of Pixelaman or Pixet SW at this moment
- ▶ Basic functionality is ensured (equalization, THL scans, internal DAC scans, data taking, temperature monitoring, internal test pulses, trigger settings etc.)
- ▶ Supporting more devices connected in LAN

Katherine – Software support

---BurdaMan--- Chip ID: H6-W0005 | IP address of readout: 192.168.1.31



Measurement Internal DACs Readout HW

Load Config

Digital Test

Grid

Ratio

Acquisition settings:

Time [s] 300 Frames 1

Frames Start

Repeat

Save Results to File Save to RAM

Detector mode:

ToA & ToT Data-Driven

Threshold:

1574

Bias Voltage [V]:

230

Frames

<= 1/1 => jump to:

Frames Auto Update

Frame statistic

Pixel count:	713
Max ToT:	140
Min ToT:	1
Average ToT:	18.72
Total ToT:	13344
Deadtime [ms]:	0
Timespread:	0
UDP Transfer:	105,5%

Color Map

Hot

Min 0 Max 80

Under Warning Over Warning

Frame progress 274,3

Acq. progress 274,3

Energy Time Count Mask Bits Pixel Th

Katherine – Internal DACs – Settings and Scan

Measurement Internal DACs Readout HW

Preamp ON	128	1.159 V
Preamp OFF	8	1.310 V
VPreamp	128	0.586 V
Ikrum	15	1.094 V
Vfbk	164	0.774 V
Threshold fine	463	0.762 V
Threshold coarse	7	0.762 V
DiscS1 ON	100	1.058 V
DiscS1 OFF	8	1.274 V
DiscS2 ON	128	0.299 V
DiscS2 OFF	8	0.146 V
PixelDAC	128	0.949 V
TPbufferIn	128	1.120 V
TPbufferOut	128	1.030 V
VTP coarse	128	0.601 V
VTP fine	256	0.594 V
CP PLL	128	0.481 V
PLL Vcntrl	128	0.658 V

Temperature: 73.6 °C

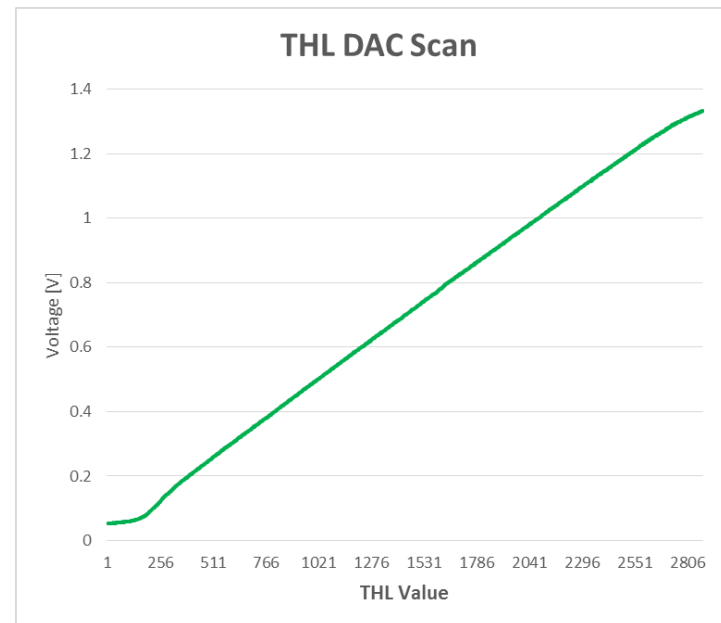
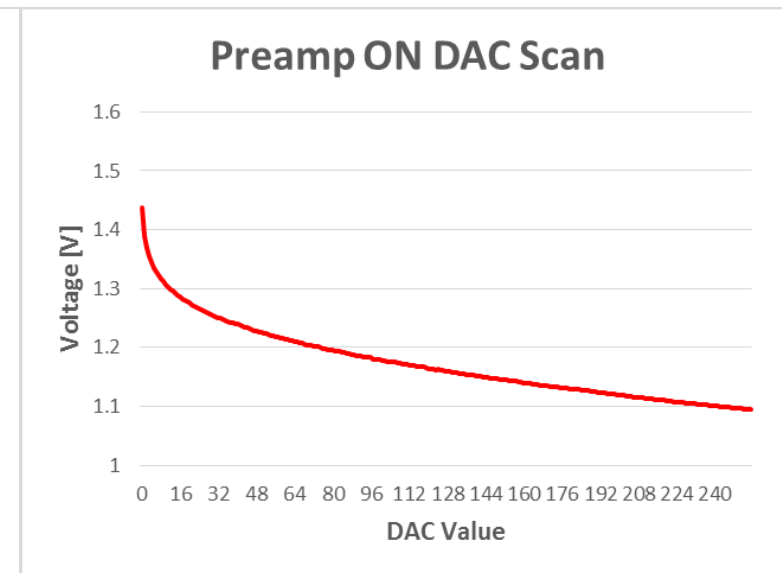
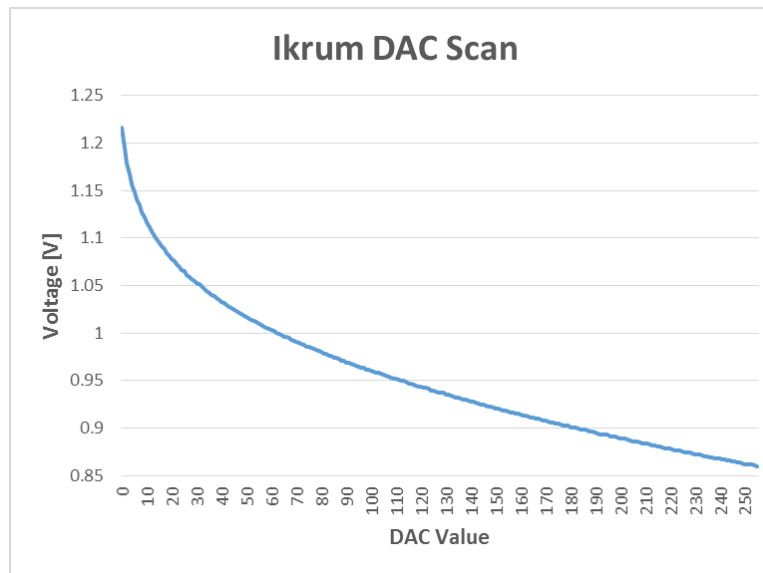
Monitoring voltage: OFF

Replacement by ext. DAC: OFF

DAC Update

DAC Scan: **lbias_Preamp_ON** THL Raw Value Save THL profile

Scan & Save!



Chip Equalization and Threshold Scan (Calibration)

SW Settings Chip Tools Miscellaneous

Chip Equalization

THL Step:

Count Threshold:

Save Equalization Data Optimization

Center Shift:

Pixel Local Threshold Shifting

Pixels with value higher than

Pixel Masking

Pixels with value higher than

Pixel Config Bits

X (Column) from to

Y (Row) from to

Mask Bit

Test Bit

Th Bits

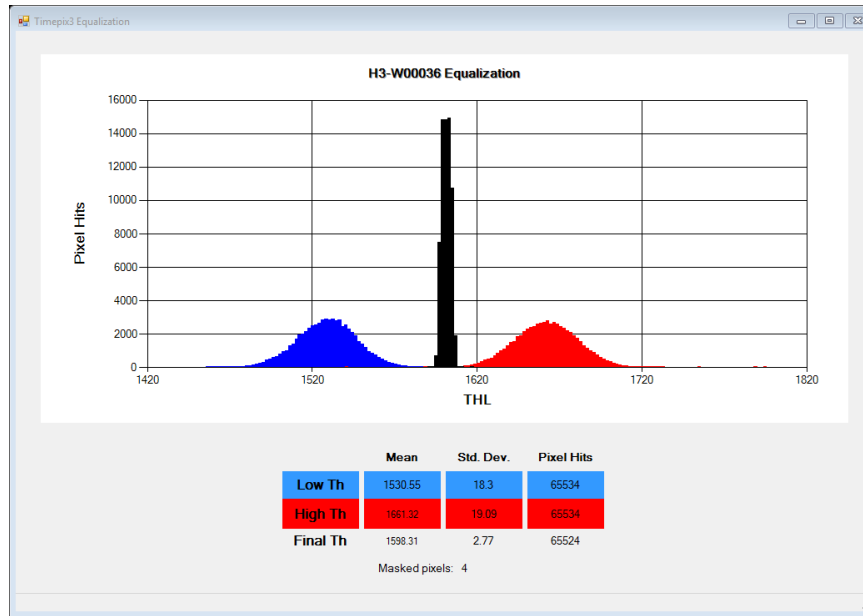
Save All Changes to Config File

THL Scan

Min: Max:

Step: Acq. Time:

Total: Acq. Count:



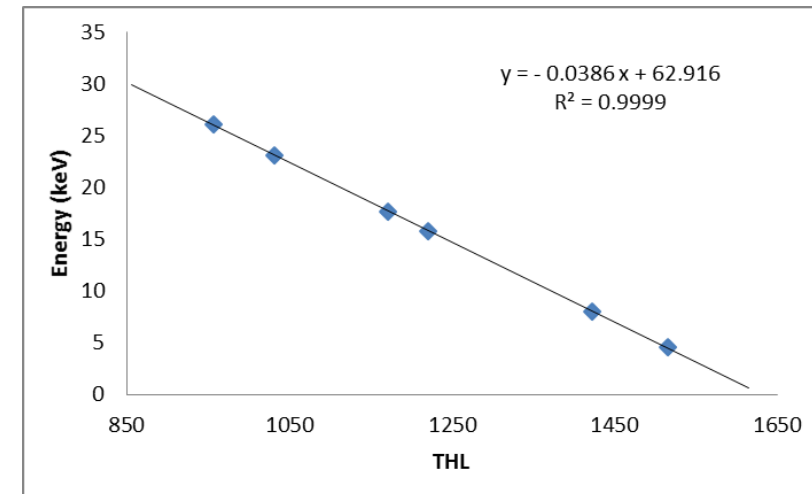
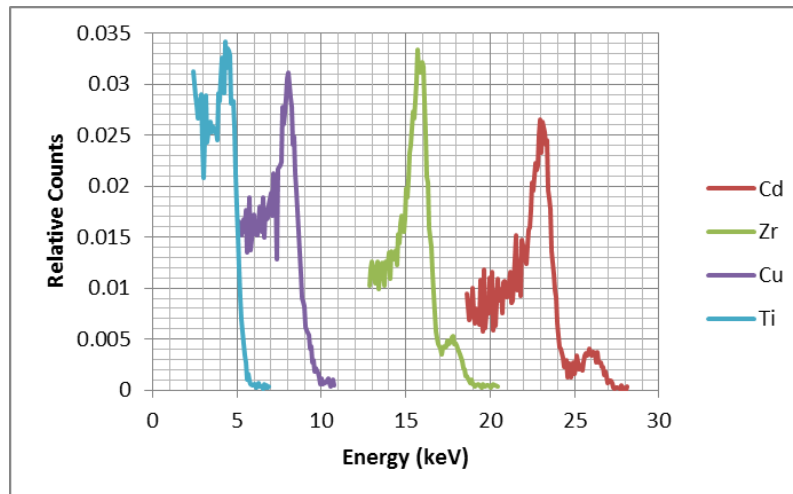
▶ Noise edge equalization

▶ Demonstration of threshold scans

▶ Ti, Cu, Zr and Cd

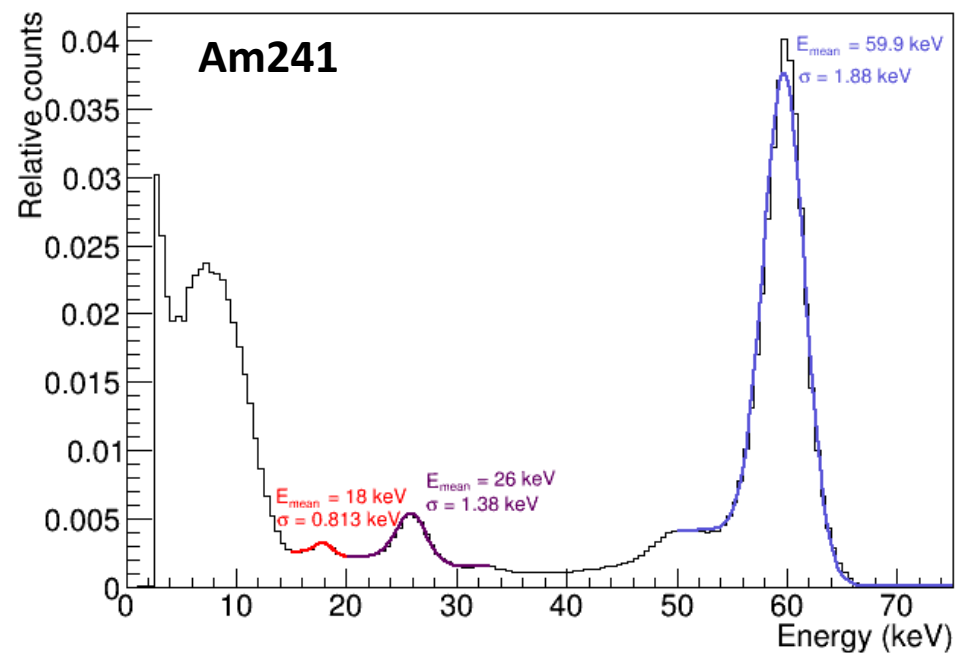
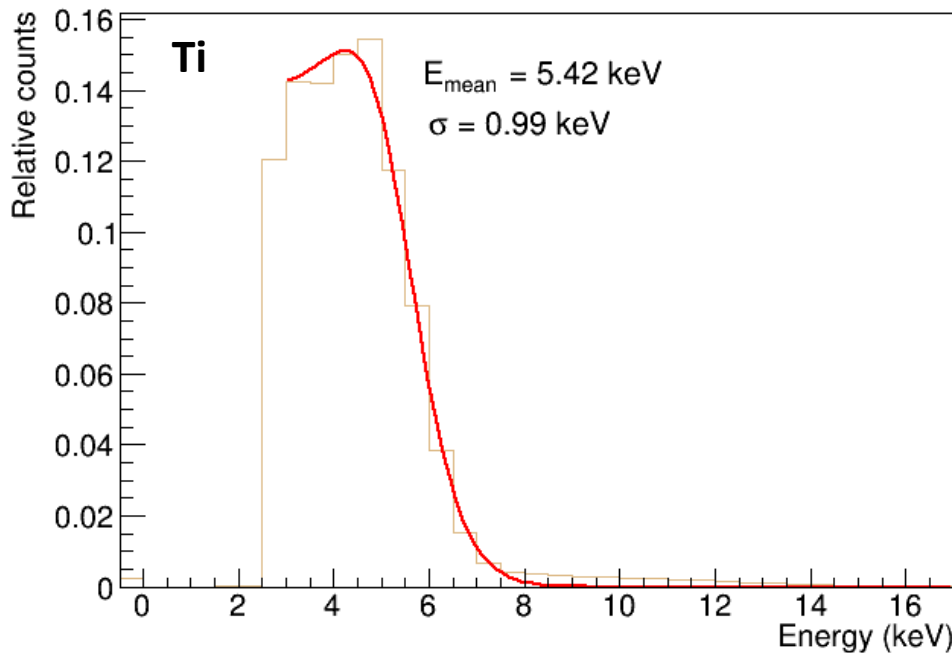
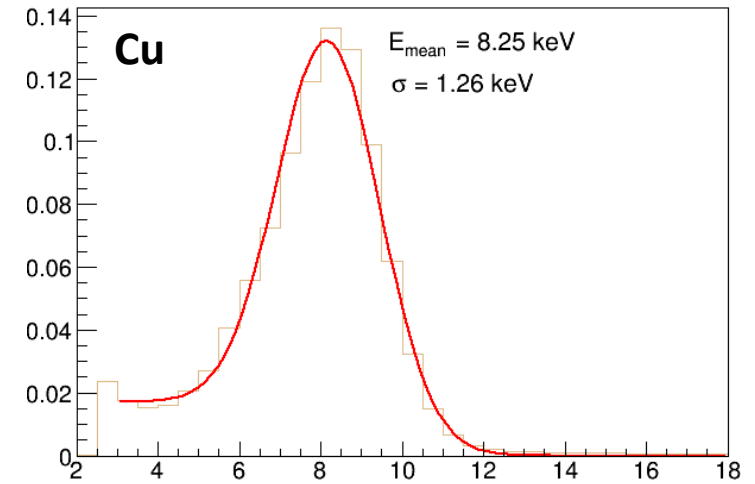
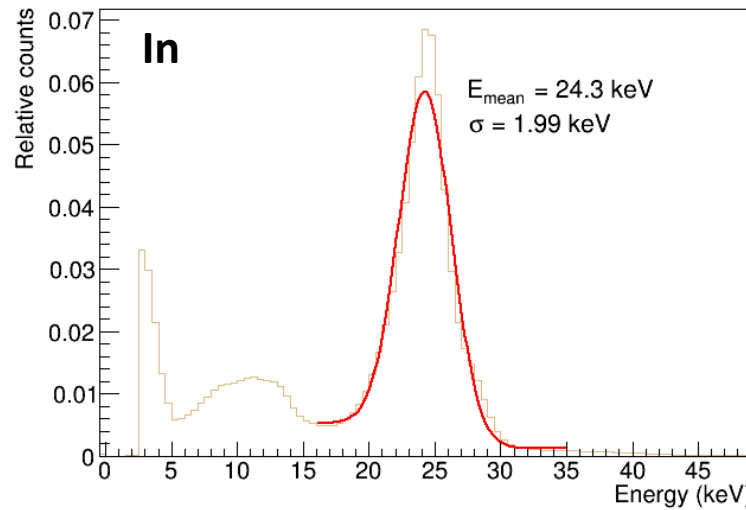
▶ Threshold level ~ 2.6keV (58°C)

▶ Threshold level ~ 2.2keV (35°C)



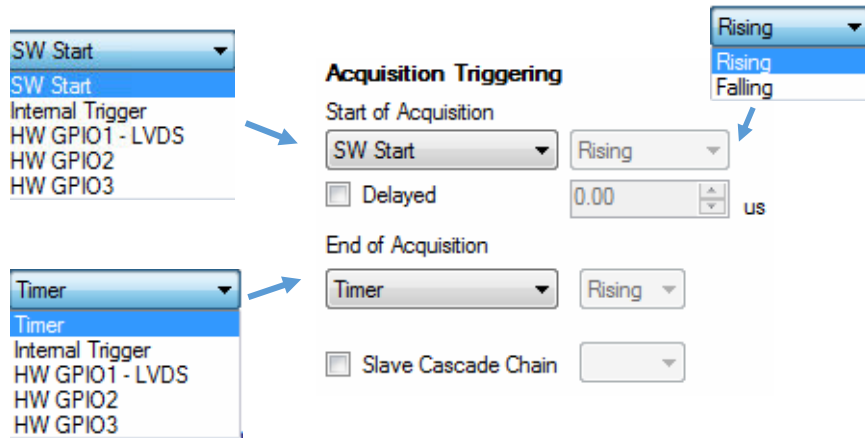
Demonstration of Energy Calibration

- ▶ Threshold ~ 2.6keV
- ▶ Ikrum = 15
- ▶ Temperature ~ 58°C

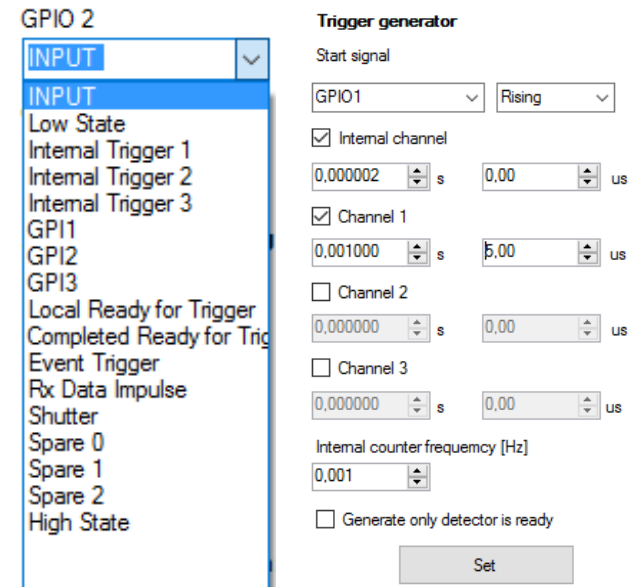


Katherine – GPIO Signals and Triggering

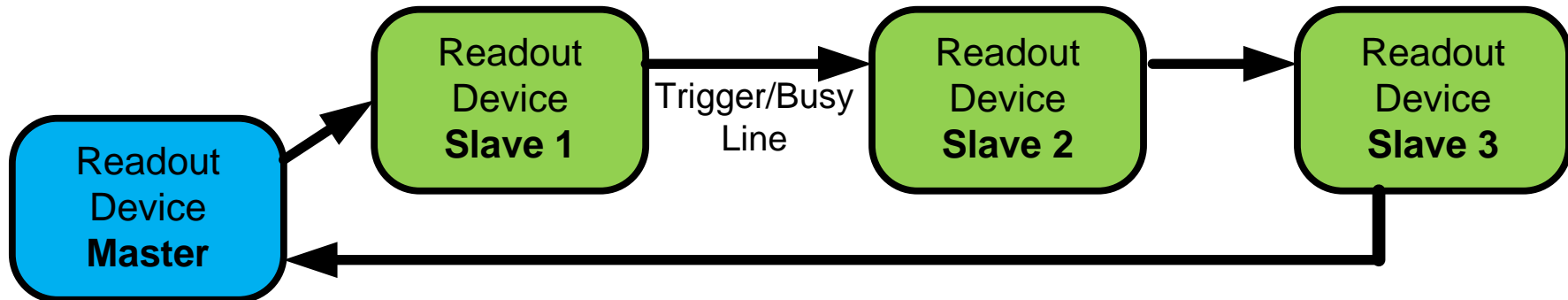
- ▶ Triggering - Start and stop events



- ▶ Implemented internal trigger generator
- ▶ User can define the meaning of GPIO

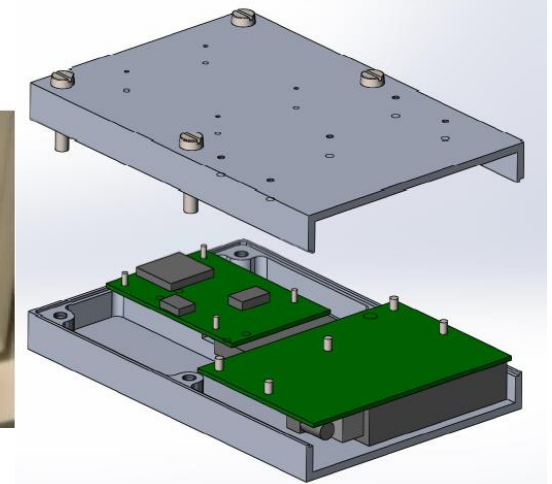
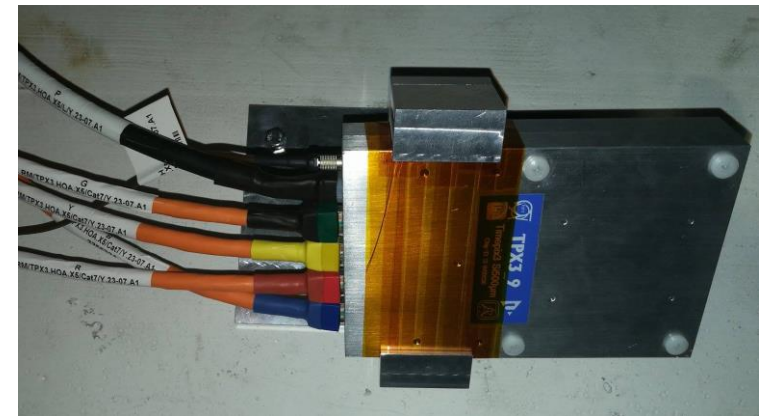
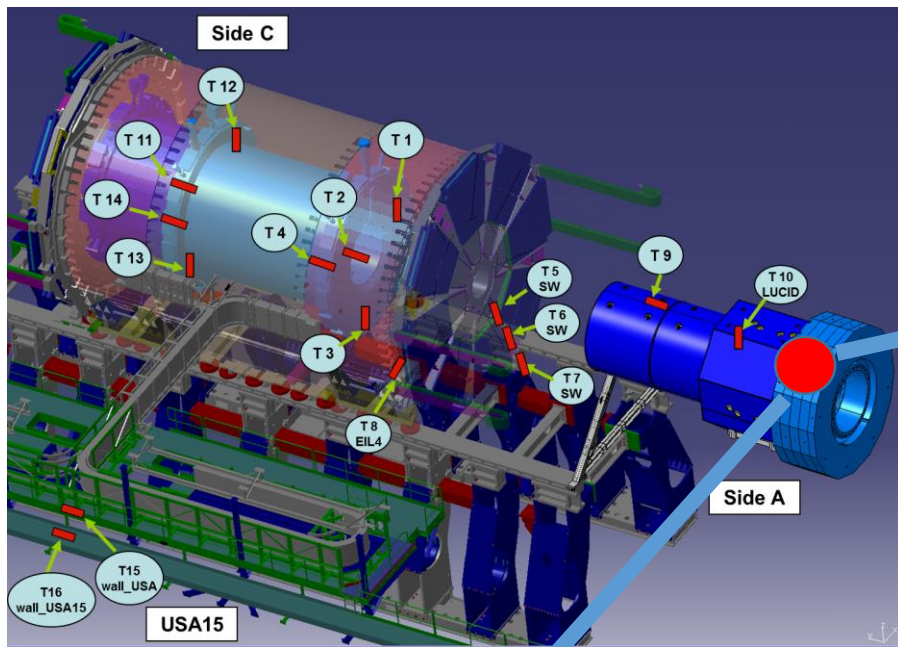


- ▶ Triggering more detectors – cascade chain
- ▶ Common LVDS trigger/busy signal



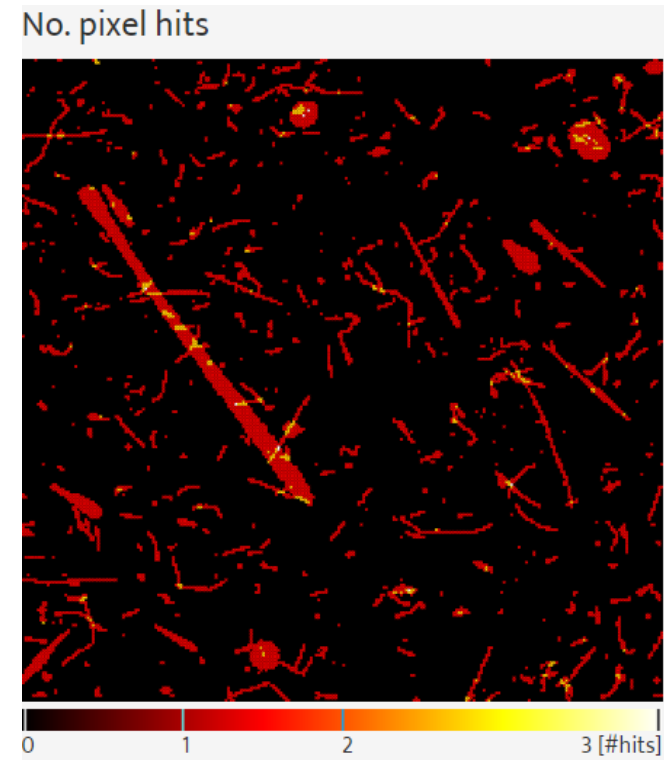
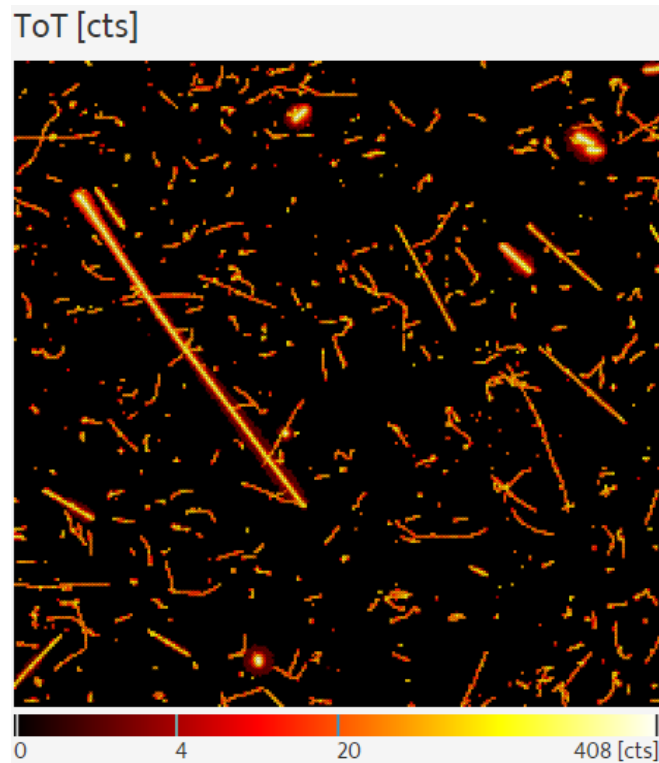
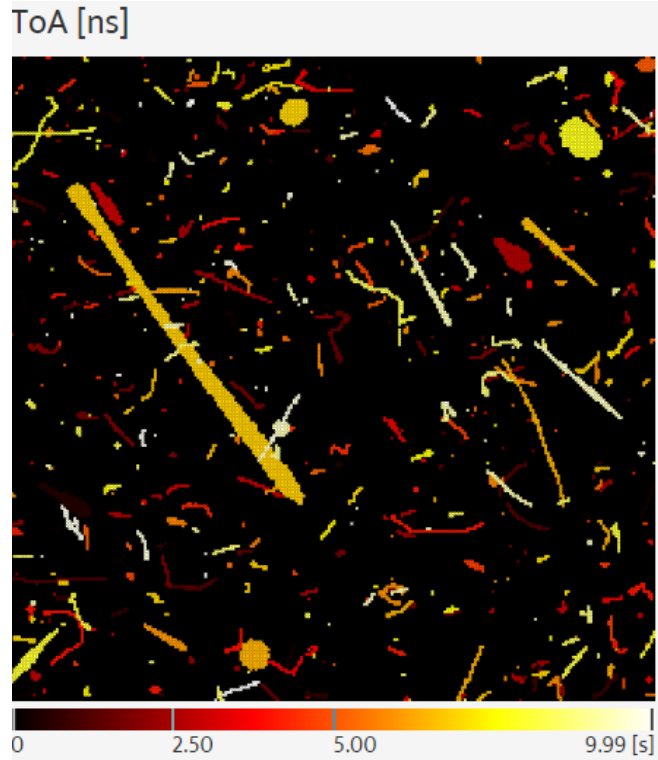
Measurement at ATLAS Cavern - Device

- ▶ Long distance between sensor and readout (~ 80m, verified also for 100m)
- ▶ Using ethernet cabling extenders + rad. hard. chipboard
- ▶ Maximal hitrate ~5 Mhits/s (after minor modification up to 10 Mhits/s)



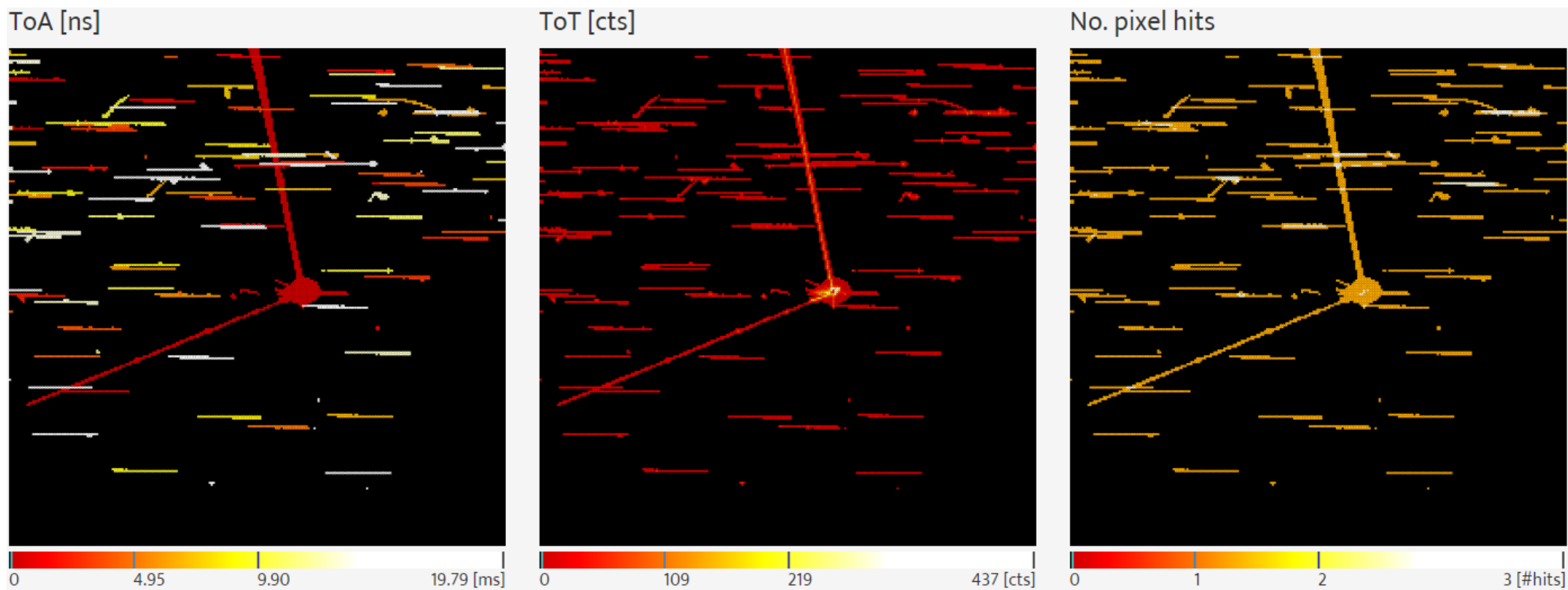
Measurement at ATLAS Cavern – Demonstration

- ▶ 10 s “frame“ in data-driven mode
- ▶ Si500 μm



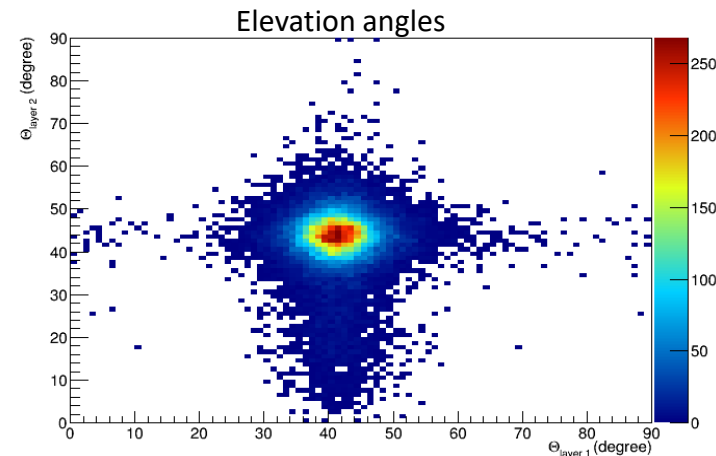
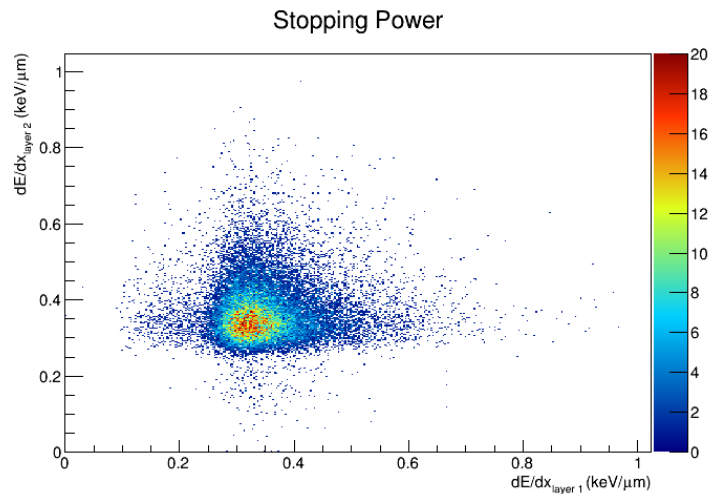
Measurement at SPS, CERN – 120GeV Pions

- ▶ 5 ms “frame“ in data-driven mode
- ▶ Si500 μm

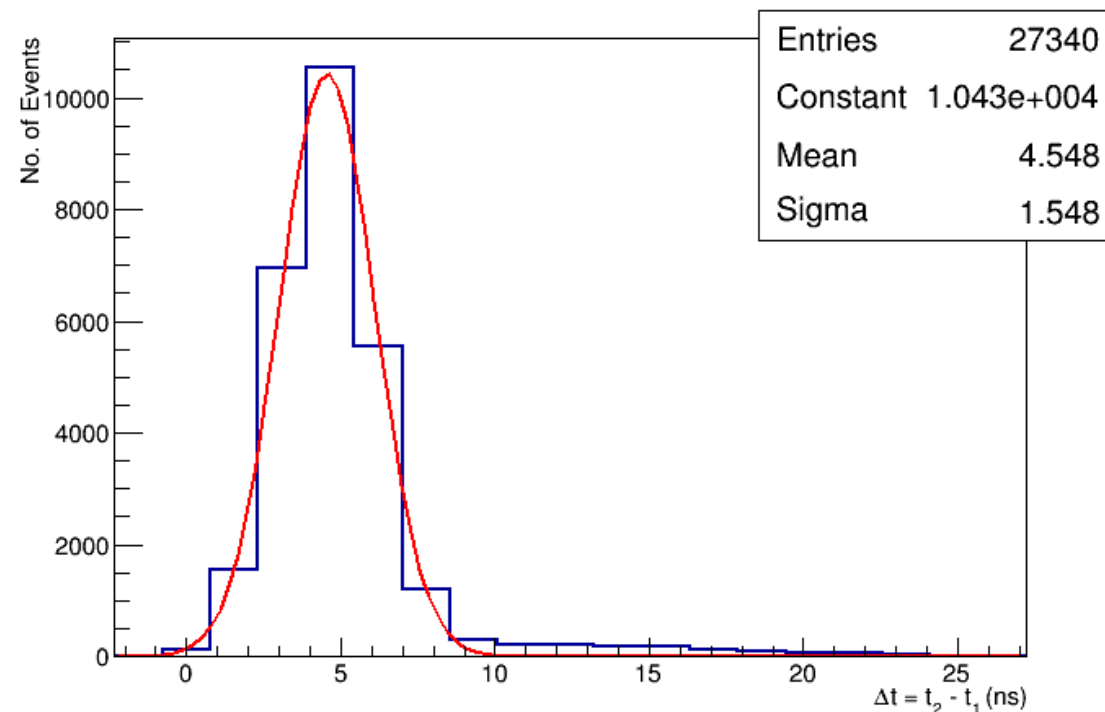


Measurement at SPS, CERN – Particle Telescope

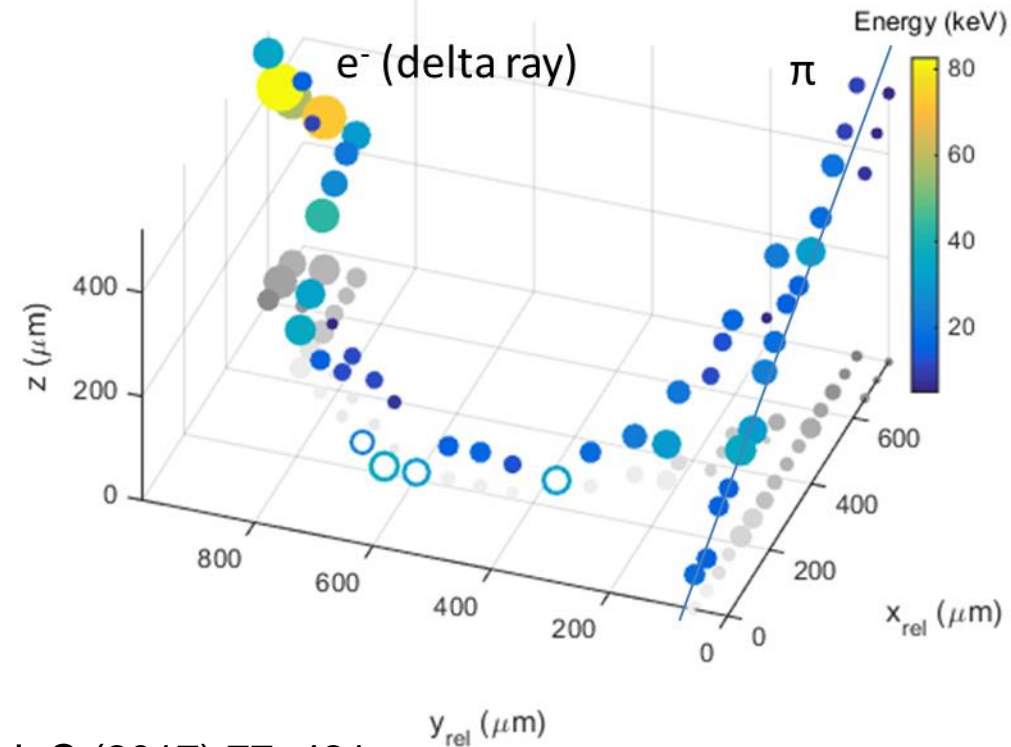
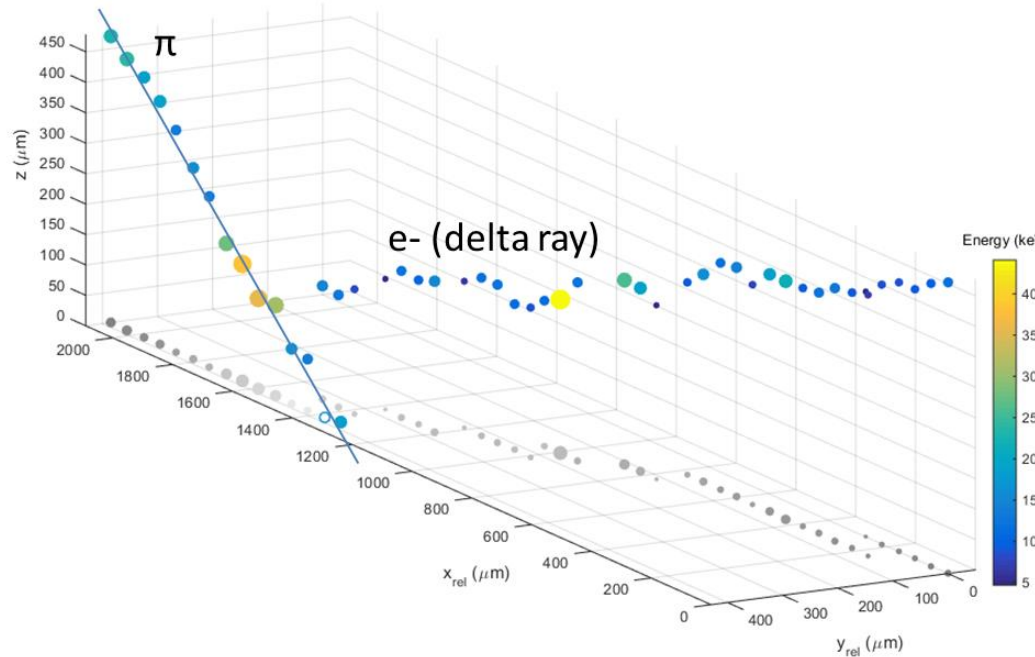
- ▶ Two Timepix3 detectors as particle telescope
- ▶ Analysis of Concurrent Tracks (time-differences between layer1 and layer2)



- Resolution $\sigma = 1.548$
- Offset due to 80 cm particle motion (2.67 ns)
- Offset of measuring chain ~ 1.8 ns



Measurement at SPS, CERN – 3D Trajectory Reconstruction



See our paper for details:

Bergmann, B., Pichotka, M., Pospisil, S. et al. Eur. Phys. J. C (2017) 77: 421.
doi:10.1140/epjc/s10052-017-4993-4

Summary

- ▶ Gigabit Ethernet interface
- ▶ Main drawback: 15Mhits/s
- ▶ Independent sending data to server or NAS (usable with low rate ~kHits/s)

- ▶ Ecosystem:
 - ▶ Software tool for detector control and data taking (Windows platform)
 - ▶ Simple SW tool for data taking (Windows, Linux, Mac)
 - ▶ Synchronization board and TDC device for interconnection of more devices
 - ▶ Radiation hardened chipboard
 - ▶ Extenders for long distances
 - ▶ Web-based visualization tool (J. Vycpalek from IEAP in Prague)

- ▶ Readouts are available (several pieces in stock) for interested people



Thank you for your attention

Petr Burian
petr.burian@cern.ch