Feedback On Nanosecond Timescales

Philip Burrows
Neven Blaskovic, Ryan Bodenstein, Talitha Bromwich, Glenn Christian,
Michael Davis, Davide Gamba, Chetan Gohil, Young Im Kim,
Pierre Korysko, Jan Paszkiewicz, Colin Perry, Rebecca Ramjiawan,
Jack Roberts

John Adams Institute, Oxford University
Oxford k-contract 1/4/14 – 31/3/17

WP1: BDS + MDI design optimisation and integration
   27 + 18 staff months + £5k + £10k

WP2: BDS beam feedback and control
   16.5 + 13.5 staff months + £11k + £60k

WP3: Drive beam phase feed-forward system
   26 + 18 staff months + £15k + £80k

WP4: Drive beam BPM feasibility study
   4.5 + 4.5 staff months + £19k + £12k

Total: 74 + 54 staff months + £50k + £162k

Key: UK + CERN (£612k)
Outline

WP3: Drive beam phase feed-forward system

WP2: BDS beam feedback and control

WP4: Drive beam BPM feasibility study

WP1: BDS + MDI design optimisation and integration
WP3: drive-beam phase feedforward system

- Develop feedback boards and amplifiers for CTF3 phase feed-forward prototype system
- Commission CTF3 prototype feed-forward system with beam
- With beam experience, optimize component design and test modified components
- Apply experience gained from CTF3 prototype to CLIC drive beam design, including performance simulations
Normal PFF Correction Mode

UPSTREAM PHASE
1.2µs, 3GHz beam pulse
4A beam current.

DOWNSTREAM PHASE
1.1µs, 3GHz beam pulse.
3.5A beam current.

COMBINER RING
0.5 turns.
Magnetic injection.
**FONT5a Board**

- Digitises phase monitor signals, calculates and outputs voltage to drive amplifiers.

- Custom built digital board:
  - 9 x 14-bit ADCs clocked at 357 MHz.
  - 4 x 14-bit DACs
  - Xilinx Virtex-5 FPGA.

- Also used by Oxford/JAI FONT group for IP feedback + ground-motion FF tests at ATF2.
• Control module: Takes inputs, distributes signals to drive modules.

• Drive module: Ixys DE150-201N09A Si FETs driving Wolfspeed C2M0160120D SiC FETs.

• 20 kW power. Max output of around 700 V for 2 V input.

• 47 MHz bandwidth for small signal variations (up to 20% max output).

• Returning signals terminated at amplifier, with monitoring.
Correction Range

- Phase shift in chicane:
  \[ \phi_f = \phi_i + R_{52} x' \]

- Applied deflection, \( x' \), defined by:
  - Amplifier output voltage.
  - Kicker design.

- \( R_{52} \) defined by chicane optics.
  - Difficult to achieve both large \( R_{52} \) and low dispersion.
  - Our optics: \( R_{52} = -0.7 \) m, Dispersion = -1.1 m (max).
Phase FF results (December 2016)

CLIC goal met: 0.2 degrees stability

and factor ~6 correction:

Jack Roberts’ PhD thesis (contributions also from Davide Gamba’s PhD)
Piotr Skowronski
CTF3 crew
For CTF3: SiC
- Silicon carbide FETs for CTF3 to get high power from a module
- high voltage devices (1kV, vs 100V LDMOS)
- eased the impedance transformation requirement
- penalty was limited high frequency output power, high power only at lower frequencies
- in practice, the unsuitable packaging available gave various not unexpected problems
- they remain attractive if power requirement are higher at low frequencies
- I did not demonstrate that they could meet full bandwidth requirement as originally stated
- I believe they can (just), but that is unproven
- remain possibly attractive for CLIC, but require bare die to be used not packaged parts

The future: GaN?
- gallium nitride relatively new (commercial for ~5 years) and rapidly improving technology
- unfortunately they are low voltage (presently: 200V max)
- harder to get high power from one module (needing more step-up of impedance)
- also unfortunate is their small die size, giving poor pulse power handling
- albeit preferable for all normal use...
- they are high frequency devices which is good for making fast amplifiers
- and not good, aggravating the usual stability problem use in linear amplifiers
- being commercially developed entirely (?) for power conversion (switching) use
- I feel they would prove the best choice on a 5 to 10 year timescale, but can't prove this
Future directions for amplifier?

**Better characterization of requirements**
- planned for wideband correction of phase noise from klystrons
- but in CTF3 dominant corrections are at much lower frequency as well as larger in magnitude

**Safely combining modules needs to be demonstrated**
- theoretically, a large number of modules can be combined
- but this has to be done without any risk of propagation
- and the system has to be able to work with failed modules
- it may not be convincing that this can be achieved

**Evaluation of amplifier technologies**
- a considerable choice in amplifier technologies
- unless power requirements come down considerably (!)
- to do this all realistic alternatives have to be pursued

**Possible Work – more relevant for CLIC ‘eng’**
- reached the stage that 'real engineering' is essential
- significant group working on it - perhaps 5 or 6
- this would have the resources to effectively test designs

**Feasible demonstrations on shorter timescale**
- a demonstration GaN amplifier power module
- but *not* a full amplifier, complete with its control and signal processing
- the associated output transformer as a practical and producible configuration
- would need to lead to a solution sufficiently developed by 2018 to be costable
Reminder of CLIC requirements

- 4 kickers at each bend
- 16 amplifiers & kickers / drive beam
- 250kW peak power / amplifier
- 256 modules in each amplifier
- 768 amplifiers total, 200MW total peak power
- amplifier cost: £75K per 250kW amplifier
- SYSTEM COST: £60M (+/-£30M) !!!
Future directions for amplifier?

**Better characterization of requirements**
- planned for wideband correction of phase noise from klystrons
- but in CTF3 dominant corrections are at much lower frequency as well as larger in magnitude

**Safely combining modules needs to be demonstrated**
- theoretically, a large number of modules can be combined to get the high peak powers needed
- but this has to be done without any risk of propagating failures
- and the system has to be able to work with failed modules
- it may not be convincing that this can be achieved without a practical demonstration

**Evaluation of amplifier technologies**
- a considerable choice in amplifier technologies, in broad terms and at more detailed level
- unless power requirements come down considerably (!) cost effective performance is vital
- to do this all realistic alternatives have to be pursued to the point that comparisons are possible

**Possible Work – more relevant for CLIC ‘engineering phase’?**
- reached the stage that 'real engineering' is essential for real progress
- significant group working on it - perhaps 5 or 6 people?
- this would have the resources to effectively test, prototype, and iterate designs

**Feasible demonstrations on shorter timescale**
- a demonstration GaN amplifier power module
- but *not* a full amplifier, complete with its control and signal processing
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WP2: BDS beam feedback and control

- Optimisation of the performance of ATF2 feedback systems as part of the ATF2 collaboration goals of 37nm beam size and nm-level beam stabilisation
- Where relevant, bench testing of prototypes: drive amplifiers, signal processors, feedback boards
- Beam tests of prototype systems at ATF2 and CTF3 – subject to beam availability
- With WP1: simulation of the integrated performance of feedback (and feed-forward) systems in the global CLIC design
- Optimised design of CLIC IP (and interface with related BDS) beam steering feedback systems for luminosity stabilisation and optimisation
- Integration of component designs within Machine Detector Interface (MDI) design
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ATF2/KEK

- Extraction line
- Damping Ring
- Nano-meter beam R&D (ATF-FF)
- Photocathode RF Gun
- S-band electron LINAC
- 1.3 GeV
FONT5 ‘intra-train’ feedbacks

ATF2 extraction line

最終収束ビームライン
— ナノメートルビームの開発 —
Nano-meter beam R&D (ATF-FF)

光陰極型高周波電子銃
— 電子ビームを生成する —
Photocathode RF Gun

電子線形加速器 (1.3GeV)
— 電子ビームを加速する —
S-band electron LINAC

ビーム取り出しライン
— 世界最先端ビームモニタの開発 —
Extraction line

ダンピングリング
— 世界最高品質の電子ビームに変換する —
Damping Ring
FONT5 ‘intra-train’ feedbacks

Quadrupole  Sextupole  Dipole  Skew Quadrupole  Corrector
Single-loop feedback

P3 used to drive K2 in single-loop mode
Used to demonstrate ILC IP feedback

ATF2:
• 3-bunch train
• Bunch interval up to 154ns
• Measure bunch-1 vertical position
• Correct bunch-2 and bunch-3 positions
Upstream FONT5 System

Analogue Front-end BPM processor

FPGA-based digital processor

Kicker drive amplifier

Beam

Strip-line kicker

Stripline BPM with mover system
Stripline BPMs

Excellent temporal resolution

V_Σ (ADC counts)

Sample index

154ns 154ns
BPM system resolution

Resolution = 291 $\pm$ 10 nm (Q $\sim$ 0.9 nC)
Two technical improvements to BPM signal processor:

- 6 dB attenuator before sum mixer used for high-charge operation
- No-PLL firmware used to remove FONT5A board sample timing jitter relative to the beam

Resolution = 157 ± 8 nm (Q ~ 1.3nC)
FB system latency

Kick to bunch 2

Latency: <154 ns
⇒ meets ILC requirements
FB system dynamic range

Kick to bunch 2

Max. kick $= 75 \text{ um}$ (1.3 GeV)
$= 400 \text{ nm}$ (ILC 250 GeV beam)
$= 66 \sigma_y$ (ILC 250)
$
\rightarrow$ meets ILC requirement of 50 $\sigma_y$
Incoming beam trajectory scan

vertical beam position
Operational jitter correction

Normal operations:

2μm jitter $\rightarrow$ 500nm
Random jitter source

Random jitter introduced pulse-to-pulse using ZVFB1X & ZVFB2X

Vertical steering magnets

FONT stipline BPMs and kickers

from Y. Kano
Enhanced-jitter correction

Normal operations:
2μm jitter → 500nm

Deliberately enhanced jitter:
14μm jitter → 500nm
Enhanced-jitter correction

Results agree with expected performance (in green)
Coupled-loop feedback

P2 & P3 used to drive K1 & K2
Beam position and angle stabilisation
Witness BPM
FONT5 system performance

Bunch 1:
- input to FB
  - FB off
  - FB on

Bunch 2:
- corrected
  - FB off
  - FB on
Time sequence

Bunch 2: corrected

FB off
FB on
### Jitter Reduction

<table>
<thead>
<tr>
<th>BPM</th>
<th>Feedback off</th>
<th>Feedback on</th>
<th>Feedback off</th>
<th>Feedback on</th>
</tr>
</thead>
<tbody>
<tr>
<td>P2</td>
<td>1.80 ± 0.06</td>
<td>1.70 ± 0.05</td>
<td>1.74 ± 0.06</td>
<td>0.44 ± 0.01</td>
</tr>
<tr>
<td>P3</td>
<td>1.56 ± 0.05</td>
<td>1.66 ± 0.05</td>
<td>1.55 ± 0.05</td>
<td>0.61 ± 0.02</td>
</tr>
<tr>
<td>MFB1FF</td>
<td>29.9 ± 1.0</td>
<td>29.4 ± 0.9</td>
<td>27.5 ± 0.9</td>
<td>8.3 ± 0.3</td>
</tr>
</tbody>
</table>

**Factor ~ 3.5 improvement**
Feedback loop witness
Feedback loop predict
Witness BPM: measure predict
Model-predicted jitter reduction at IP

\[ y \]

\[ y' \]

\[ FB \text{ off} \]

\[ FB \text{ on} \]
Predicted jitter reduction at IP

<table>
<thead>
<tr>
<th>Bunch</th>
<th>Position y jitter (nm)</th>
<th>Angle y' jitter (urad)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Feedback off</td>
<td>Feedback on</td>
</tr>
<tr>
<td>1</td>
<td>9.5 ± 0.3</td>
<td>10.1 ± 0.3</td>
</tr>
<tr>
<td>2</td>
<td><strong>9.4 ± 0.3</strong></td>
<td><strong>3.6 ± 0.1</strong></td>
</tr>
</tbody>
</table>

Predict position stabilised at few nanometre level…

How to measure it?!
Measured beam-size reduction at IP

- Position jitter is suppressed using FONT system at the IP as well.
  - ~ 60 nm
  - ~ 100 nm
Measured beam-size reduction at IP

![Graph showing beam-size reduction with and without modulation](image)

- **Font ON**
  - Modulation vs Jitter source amplitude
  - Peak modulation: 0.39
  - Standard deviation: 58 nm

- **Font OFF**
  - Modulation vs Jitter source amplitude
  - Peak modulation: 0.07
  - Standard deviation: 99 nm
Cavity BPM system near IP
IP cavity BPM system
Cavity BPM signal processing

I → I’
Q → Q’
bunch charge
Resolution has been studied by 3 Oxford PhD students for several years …

Best resolution measured honestly (geometric method) is 57nm (single sample) and 46nm (9-sample integration)

Smallest jitter ever measured at one BPM is 49nm (integration)

Using a multi-parameter fit (up to 13 parameters!) best resolution is 31 nm (single sample) and 27nm (integration)

3.5 times worse than obtained by Honda in 2008!
Low-Q cavity BPMs

Design parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Dipole cavities</th>
<th>Reference cavities</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$x$ port</td>
<td>$y$ port</td>
</tr>
<tr>
<td>Resonant frequency $f_{mn}$</td>
<td>5.712</td>
<td>6.426</td>
</tr>
<tr>
<td>Internal quality factor $(Q_0)_{mn}$</td>
<td>4959</td>
<td>4670</td>
</tr>
<tr>
<td>Decay time $\tau_{mn}$</td>
<td>18.72</td>
<td>17.23</td>
</tr>
</tbody>
</table>

Measured was 10 ns (A, B), 6ns (C) (BPMs remade twice, and C since been In-sealed twice)
Cavity BPM IP feedback

IPB used to drive IPK in single-loop mode
Working towards nanometre level stability
Best IP feedback results

Stabilising from 440 nm to ~70 nm
2-BPM IP feedback

Use input from IPA and IPC to stabilise beam at IPB

First look in October 2016: nice initial results, more work needed:

<table>
<thead>
<tr>
<th>Feedback</th>
<th>Bunch 1 jitter (nm)</th>
<th>Bunch 2 jitter (nm)</th>
</tr>
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<tbody>
<tr>
<td>Off</td>
<td>261 ± 19</td>
<td>264 ± 19</td>
</tr>
<tr>
<td>On</td>
<td>267 ± 20</td>
<td>133 ± 10</td>
</tr>
</tbody>
</table>
Proposal for ongoing work

• CLIC review highlighted small, stable beams as issue for achieving CLIC luminosity
• The beam-size dependence on bunch charge is not yet fully understood – Pierre Korysko PhD → ATF2 goal 1
• ATF2 goal 2 is to stabilise beam at ‘nanometer level’ – far from demonstrating this: much harder than at CLIC
• Functionally both the upstream and IP FB systems are capable of doing this, the problem is getting nm resolution in the cavity BPMs
• Needs a redesign and/or refabrication of the IP cavity BPMs (and possibly also the electronics)
• PhD students: Talitha Bromwich, Rebecca Ramjiawan
• 2-years of postdoc effort, supported by Colin Perry
CLIC IP FB system (CDR)
Engineer comments (Colin Perry)

- radiation: this is the biggest problem
- magnetic field: restrictive, in that ferrite cored inductors and transformers have to be avoided
- size: very limited space is available, but this is not a real difficulty
- reliability: critical
- inaccessibility: only exchange of a single IP electronics unit is practical, & without manual connections
- configurability: operation needs to be reconfigurable as far as possible without access to the IP unit
A demo system could be built today – ambitious for 2019!
- would meet size, magnetic field, and radiation requirements
- assumes we do not need normalization for bunch charge
- includes controllable non-linearity
- little or no digital internally except for simple switches

Limited demonstrations?
- BPM 1.5GHz front end avoiding use of ferrite components
- GaN amplifier output stage of appropriate capabilities (driving a dummy kicker)
- could be demonstrated at CLEAR, given suitable BPM + kicker
Ryan Bodenstein will report the scientific progress in a short talk to follow.
WP1: BDS + MDI design optimisation and integration

- Set up CLIC integrated beam tracking simulation on Oxford Grid cluster
- Extend and augment tracking code by implementing FB and stabilisation systems based on measured performance of prototypes at ATF2 and elsewhere
- Develop and implement CLIC tuning tools for ATF2 and compare techniques
- Strong emphasis on static two-beam tuning
- Evaluate CLIC luminosity performance under realistic machine condition scenarios
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  - ✔️
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  - ❌
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  - ❌
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Proposal for ongoing work

• Ryan is now fully up to speed and integrated in the CLIC beam tuning team
• At ATF2 (with Fabian) in December + January
• Continue to develop single- and two-beam tuning techniques for CLIC
• Apply + develop tuning techniques at ATF2
• Contribute to luminosity tuning/optimisation studies for the energy-staged CLIC Project Plan
• New doctoral students:
  Chetan Gohil – stray magnetic field effects
  Pierre Korysko – wakefield effects on beam size
• 2-years postdoc effort, also to support PhD students
WP4: description of work

• Study of low cost BPM pickup alternatives
• Study of the PETS RF power EMI at the pickup location
• Theoretical (EM simulations) and practical (CLEX beam)
• Compare different BPM types, including costs and performance
• Stripline, button, coaxial and other “exotic” designs
• Evaluate read-out electronics for a cost/performance optimized DB BPM pickup
Proposed programme summary

- ATF2: small-beam + nm-stabilization
  Burrows, Christian, Perry, vice Blaskovic, Bromwich, Ramjiawan, Korysko

- CLIC beam tuning + luminosity optimisation
  Bodenstein, Korysko, Gohil

- CLIC phase feed-forward amplifier module?
  CLEAR: demo of CLIC IPFB components?
  Stripline BPM applications for CLIC?
  Perry, Christian, Burrows

- (Xbox-3 + RF studies: Paszkiewicz)
## Proposed resources (1/4/17-31/3/19)

- **Staff effort (months):**
  - Burrows, Christian: Oxford 44, CERN 0
  - Blaskovic, Roberts: Oxford 3, CERN 1
  - Bodenstein, vice Blaskovic: Oxford 0, CERN 48
  - Perry: Oxford 15, CERN 9
  - **Total:** Oxford 62, CERN 57

- **PhD students (months):**
  - Bromwich, Ramjiawan: Oxford 36, CERN 0
  - Gohil, Korysko, Paszkiewicz: Oxford 72

- **Equipment, consumables, travel (k£):** Oxford 50, CERN 100
Backup slides
CLIC prototype: FONT3 at KEK/ATF

Kicker → BPM 1 → BPM 2 → BPM 3

Electronics latency ~ 13ns
Drive power > 50nm @ CLIC
## ATF2 design parameters

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<th>Design value</th>
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<tr>
<td>Energy (GeV)</td>
<td>1.3</td>
</tr>
<tr>
<td>Intensity (electrons/bunch)</td>
<td>$1 \times 10^{10}$</td>
</tr>
<tr>
<td>Repetition rate (Hz)</td>
<td>3.12</td>
</tr>
<tr>
<td>Horizontal emittance $\epsilon_x$ (m rad)</td>
<td>$2 \times 10^{-9}$</td>
</tr>
<tr>
<td>Vertical emittance $\epsilon_y$ (m rad)</td>
<td>$1.2 \times 10^{-11}$</td>
</tr>
<tr>
<td>Horizontal IP beam size $\hat{x}^*$ (m)</td>
<td>$2.8 \times 10^{-6}$</td>
</tr>
<tr>
<td>Vertical IP beam size $\hat{y}^*$ (m)</td>
<td>$3.7 \times 10^{-8}$</td>
</tr>
<tr>
<td>Horizontal IP beta function $\beta_x^*$ (m)</td>
<td>$4 \times 10^{-3}$</td>
</tr>
<tr>
<td>Vertical IP beta function $\beta_y^*$ (m)</td>
<td>$1 \times 10^{-4}$</td>
</tr>
<tr>
<td>RMS energy spread (%)</td>
<td>0.08</td>
</tr>
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Xilinx Virtex5 FPGA

9 ADC input channels (TI ADS5474)

4 DAC output channels (AD9744)

Clocked at up to 400 MHz (phase-locked to beam)
FONT4 drive amplifier

- FONT4 amplifier, outline design done in JAI/Oxford
- Production design + fabrication by TMD Technologies
- Specifications:
  
  +- 15A (kicker terminated with 50 Ohm)
  +- 30A (kicker shorted at far end)
  35ns risetime (to 90%)
  pulse length 10 us
  repetition rate 10 Hz
BPM readout

LO source

LO phase shifters

LO signals

P3

P2

P1

stripline BPMs

stripline phase shifters

stripline signals

analogue processor modules

processor output signals

digitizer
BPM signal processing
BPM signal processor
ILC IR: SiD for illustration
ILC IR: SiD for illustration
Final Doublet Region (SiD)
Final Doublet Region (SiD)
IP kicker detail (SiD)
Final Doublet Region (SiD)
IP FB BPM detail (SiD)

- Beam in
- Beam out

Tom Markiewicz, Marco Oriunno, Steve Smith
ILC IP FB performance (TDR)