



Bumping and Flip-Chip of ASICs



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HighRR Seminar

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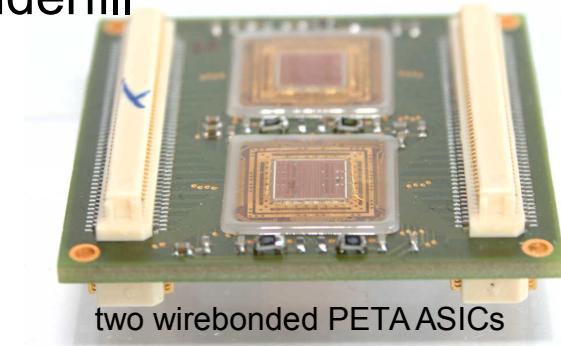
Flip-Chip vs. Wirebonding

- Advantages of Flip-Chip

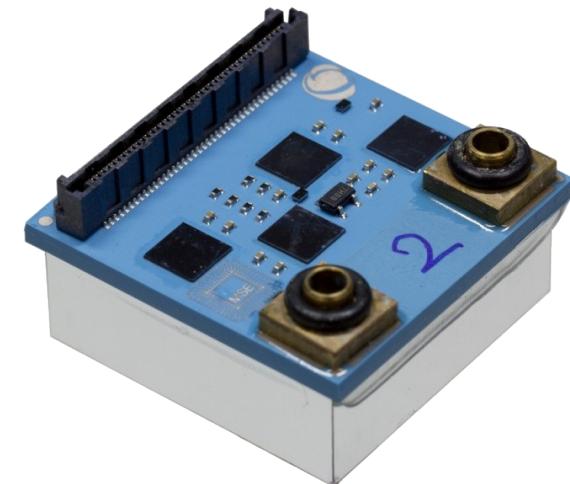
- reduced chip footprint on substrate
- compact modules
- robust modules: interconnect hidden below silicon, underfill
- lower inductance due to shorter interconnect path
- parallel bonding of all signals

- Disadvantages

- complex process: ubm, bumping, flipping, underfill
- wirebonding is fast for prototypes
- industry focuses on wafer processing
- MPW & single chip bumping difficult
- prototyping bumped chips: wirebond interposer
- probestation testing of high bump count



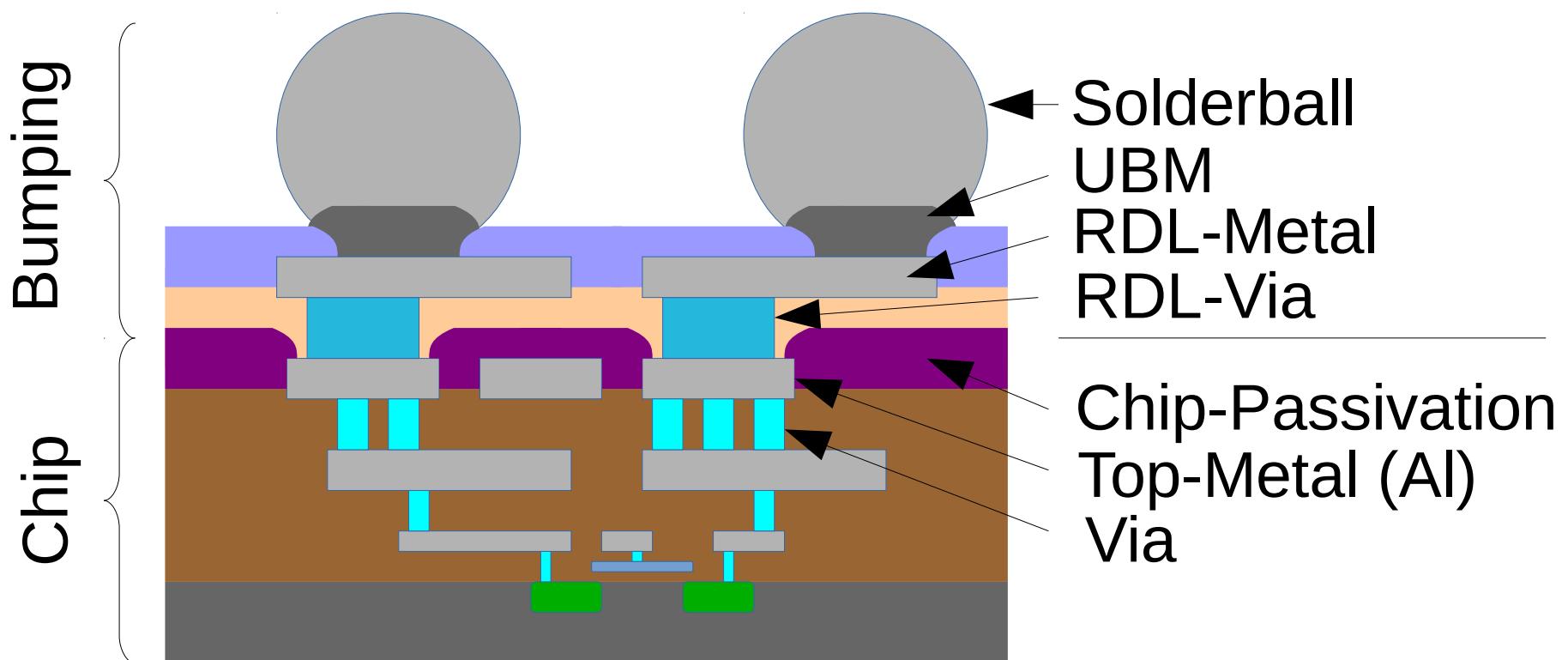
two wirebonded PETA ASICs



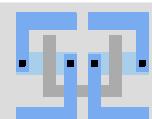
four flip-chip PETA ASICs

- Indium
 - small: 20µm pitch, 10µm diameter; electroplated
 - soft, low soldering temperature (<180°C)
- Goldstud
 - 50µm diameter, 70µm pitch
 - modified gold ball/wedge wirebonding process
 - slow sequential bumping process; high force flip-chip; >300°C
- Solder
 - minimum: 20µm pitch, 15µm diameter; standard: 200µm pitch / 100µm dia
 - Chip-on-Board: 300-500µm diameter
 - evaporation, electroplating, screen printing, ball drop, jetting
 - Eutectic, High-Lead, Lead-free solder alloys; >200°C soldering
- more...
 - Cu-Pillar
 - Solid-Liquid Interdiffusion (SLID): High Temperatur (600°C) applications

Solder Bumping Metal Stack

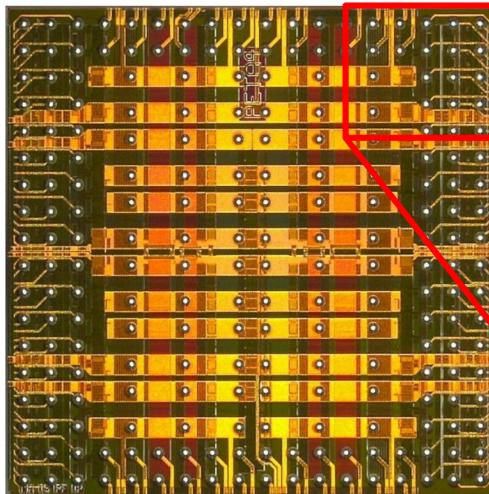


example of solder bumping metal stack (not to scale)

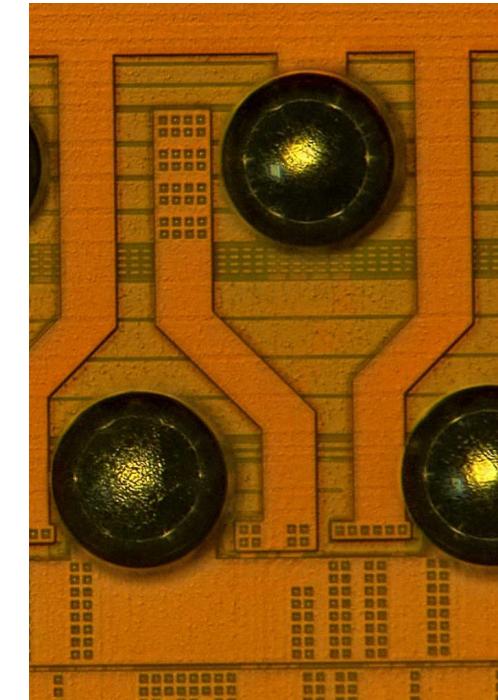
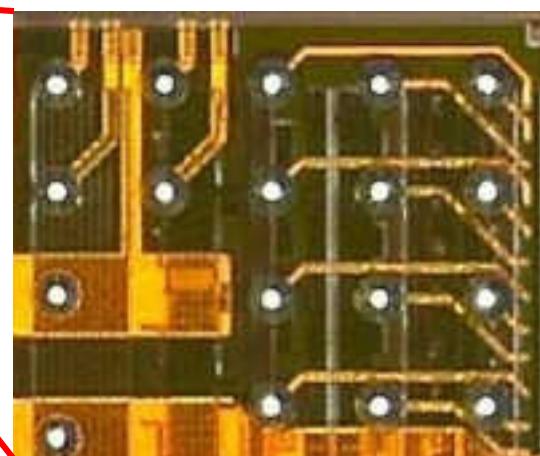


Redistribution Layer (RDL)

- Rerouting from wirebond padframe to bump pad array
 - additional metal/passivation layer ontop of final wafer
 - processed by foundry or bumping provider
- Metal properties vary
 - Al or Cu
 - coarse structures
- Design rules / RDL-layer not part of design kit
 - DRC and LVS rule files need to be extended manually



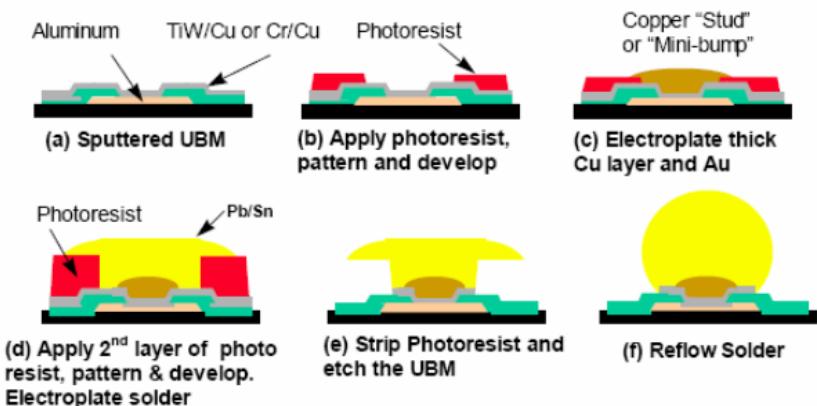
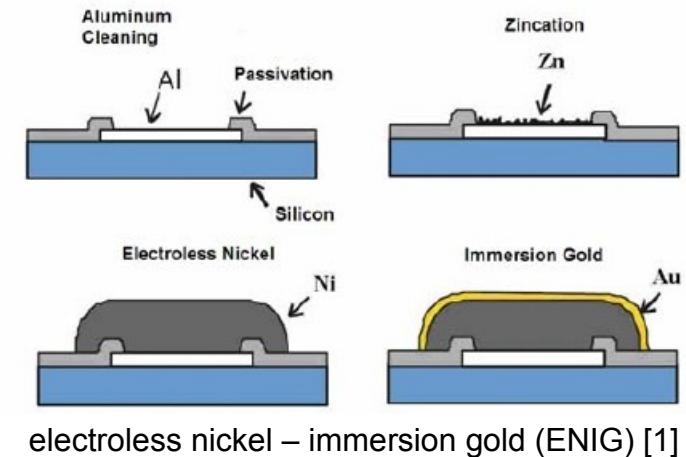
PETA ASIC wirebond rerouting



RDL of bump-only
DCD ASIC

Under Bump Metallization (UBM)

- Solderable surface required
 - Al-pads are not solder wettable
 - MPW submissions have Al-pads
- Under Bump Metallization (UBM)
 - provides solder wettable surface
- Industry standard
 - multi layers of metal: adhesion, diffusion barrier, wettable, oxidation barrier
 - electroless (ENIG), electroplating, sputtering, evaporation
 - complicated process, masks required
 - waferlevel processing
- Solderable substrate required, too!



Further reading:

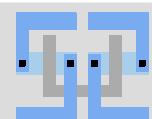
Under bump metallurgy (UBM) - A technology review for flip chip packaging

[1] <https://www.researchgate.net/publication/242476081>

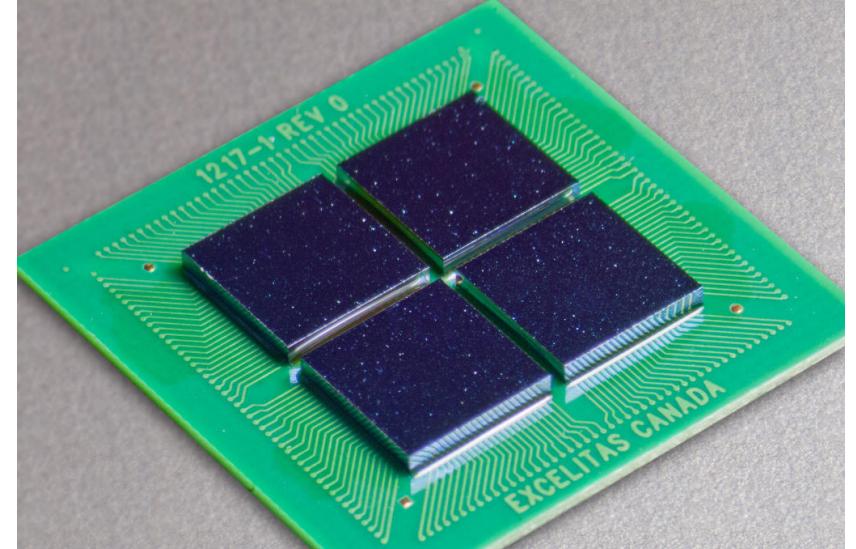
- Bumping of MPW and single chips difficult
 - MPW: no access to wafers, only single chips delivered
 - most bumping technologies process on wafer level!
 - best if MPW offers bumping option
 - bumped single die delivered
 - bumping subcontractors switch often -> designrule, solder changes
 - diff. solder types -> melting temperatures differ
 - single chip handling, manual UBM processing and bumping
 - passivate chip edges and apply ENIG UBM -> time consuming, bad yield
 - solder jetting works well
 - assemble support wafer with single chips and process on waferlevel
 - new, no results yet
- Goldstuds as UBM
 - simple process for single chips
 - gold-solder-intermetallics are brittle

UMC bumping costs

- MPW bumping
 - Masks: 12k EUR
 - Bump process (1 Wafer): 620 EUR
 - Admin+Logistic: 110 EUR
- Engineering Run
 - Masks: 10k EUR
 - Bumping 500 EUR / wafer
 - Thinning 25 EUR / wafer



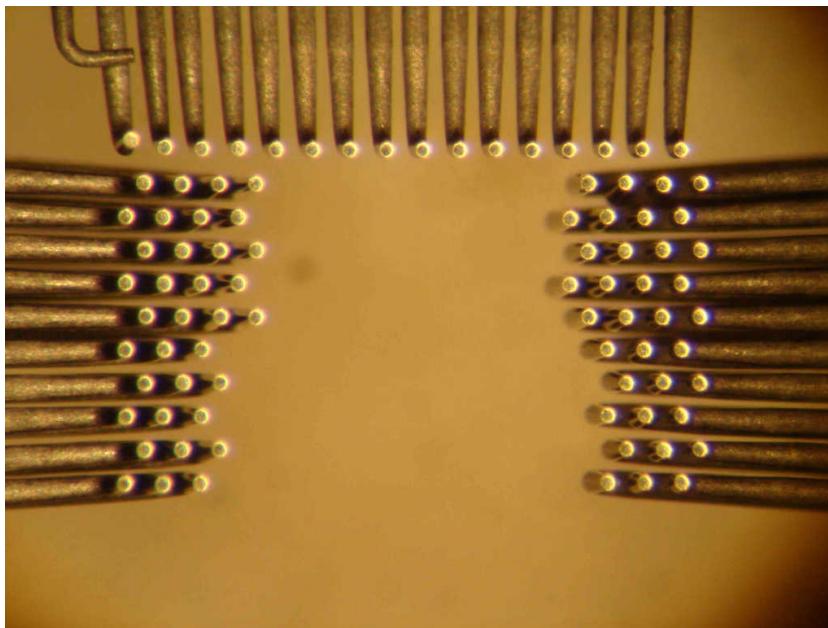
- CTE mismatch of silicon and substrate (ceramic, PCB, ...)
 - mechanical stress on solder joints
 - cracks develop
- Add glue to fill gap between chip and substrate (underfill)
 - glue reduces stress on solder
 - epoxy based, thermal curing
 - medium viscosity
 - apply after flipchip
 - capillary flow



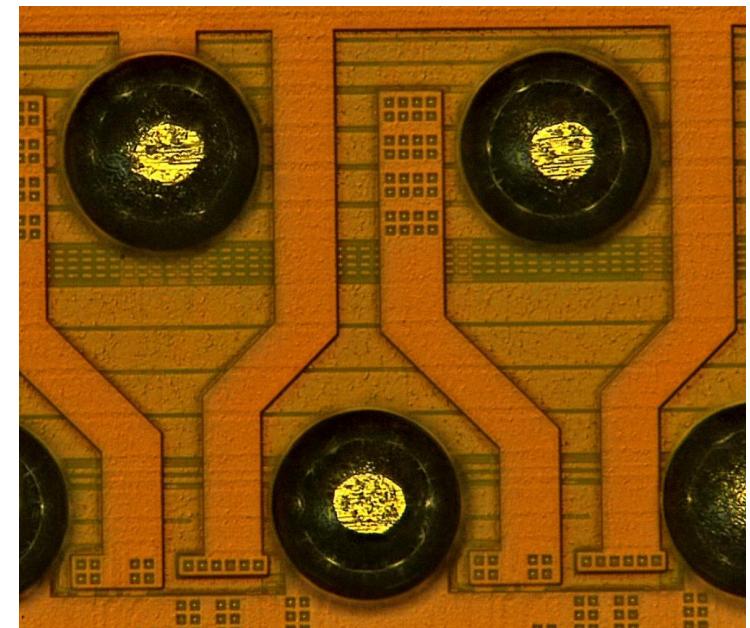
15x15mm² PCB with four underfilled chips

Probecard Testing

- Multiple layers of L-shape probe needles
- Flat needle tips
- Overtravel to break oxide on solder ball -> ball deformation
- Needle cleaning required to remove residues
- Connection problems



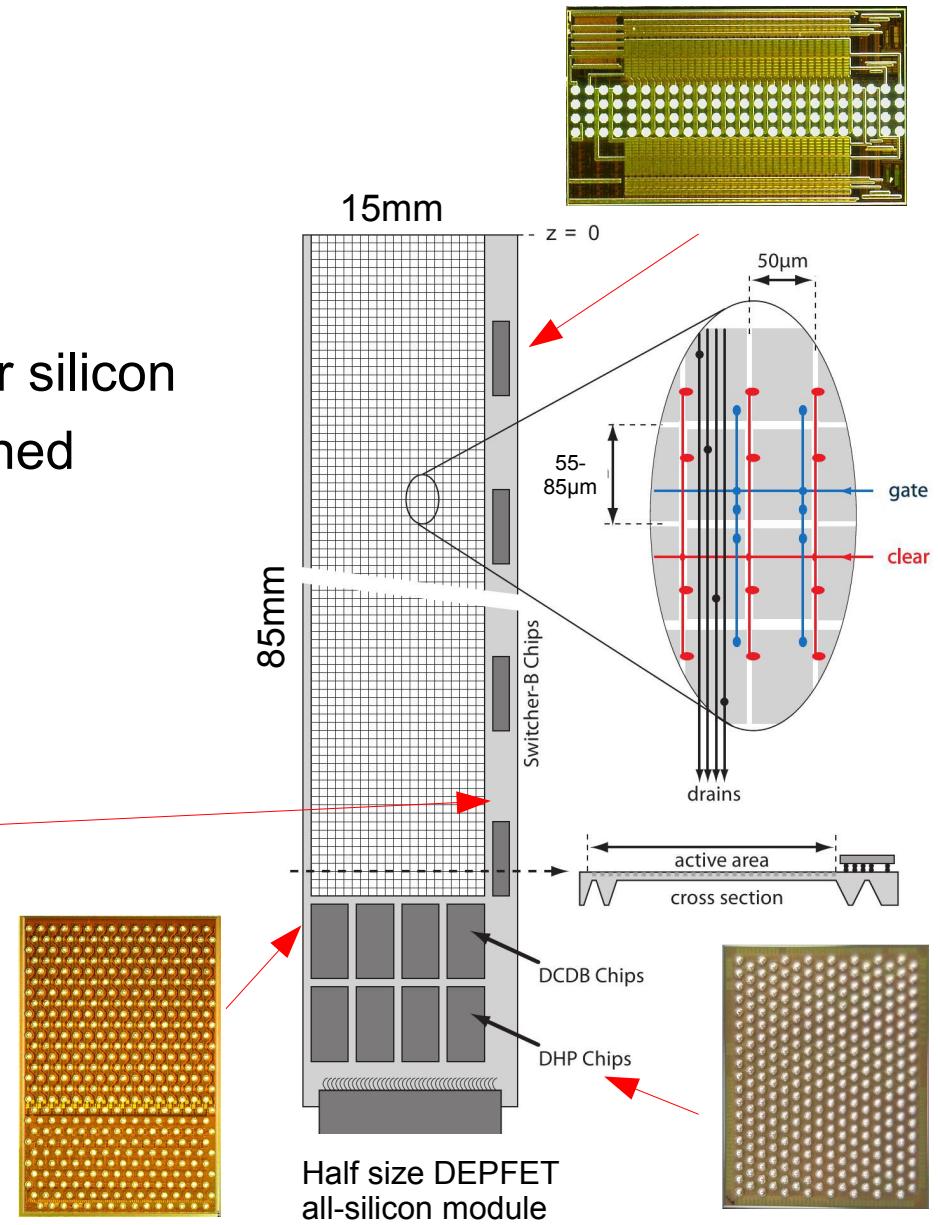
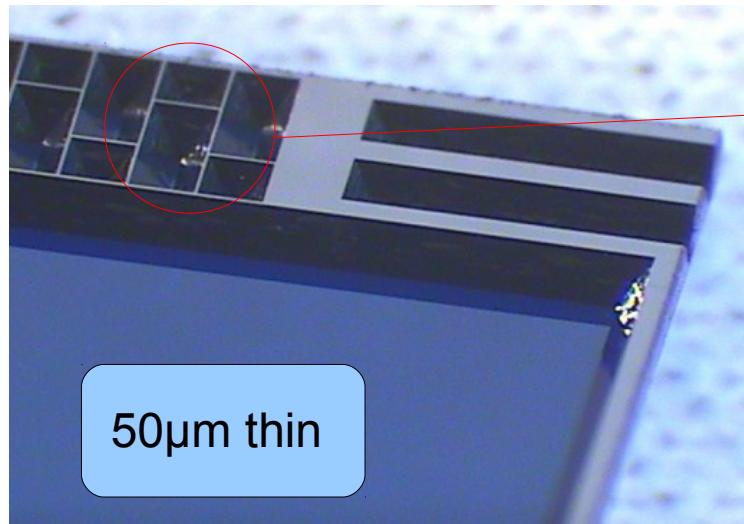
bottomview of probecard needles for solder bump testing.



100 μ m solder bumps with scratch marks after needle probing

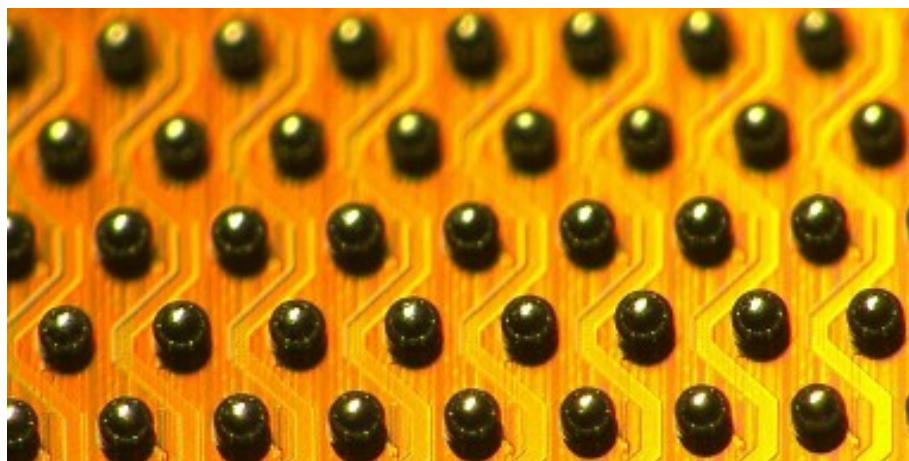
DEPFET all-silicon module

- DEPFET pixel detector
 - Belle tracker upgrade
 - ILC vertex detector
- Self-supporting all-silicon module
 - no interposers: flip-chip onto detector silicon
 - thinning down to $50\mu\text{m}$, partially thinned support frame
 - low material budget: 0.18% X0

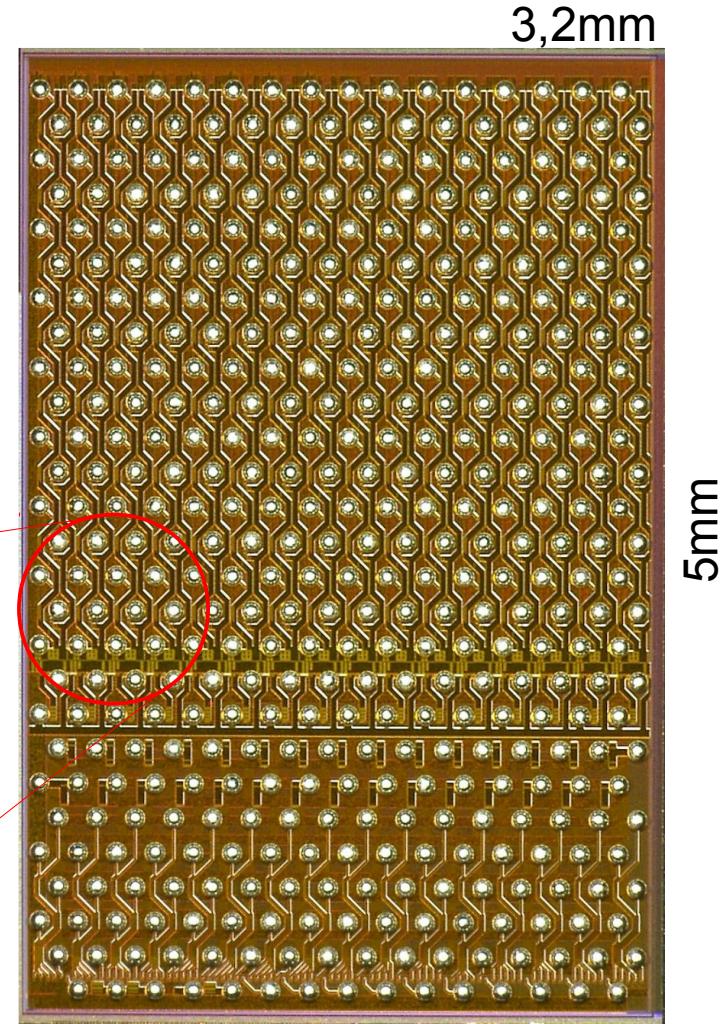


DEPFET ASIC bumping

- Multi-Project Wafer (MPW) Chip Submissions
 - many designs on a single wafer layout -> production cost sharing
 - no access to wafers
 - single chips are delivered
 - limited set of technology options
- DEPFET ASIC bumping
 - DCDB, DHP: MPW bumping
 - SwitcherB: no MPW bumping



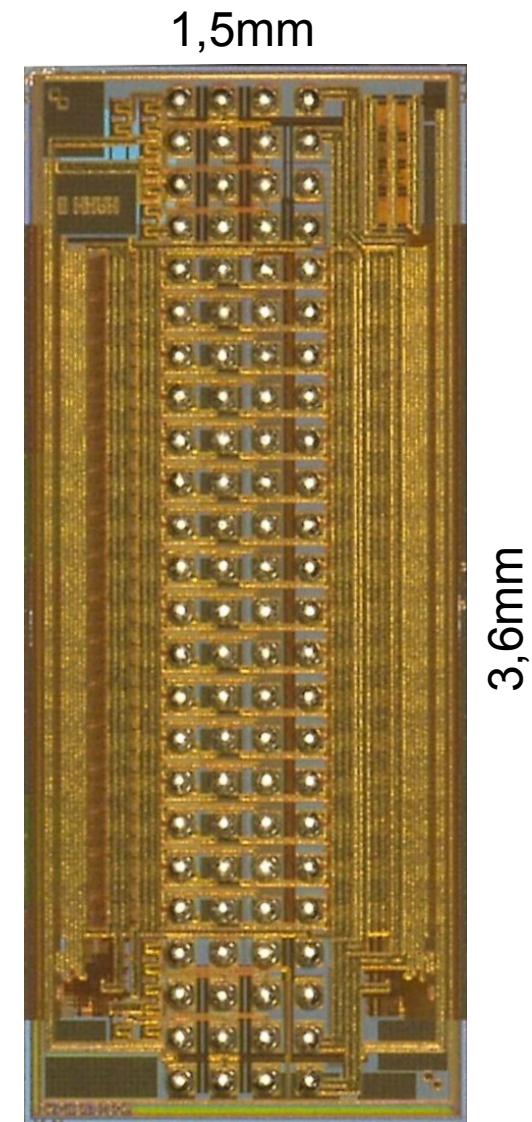
100 μ m bumps, 200 μ m pitch



DCDB read-out chip (430 bumps)

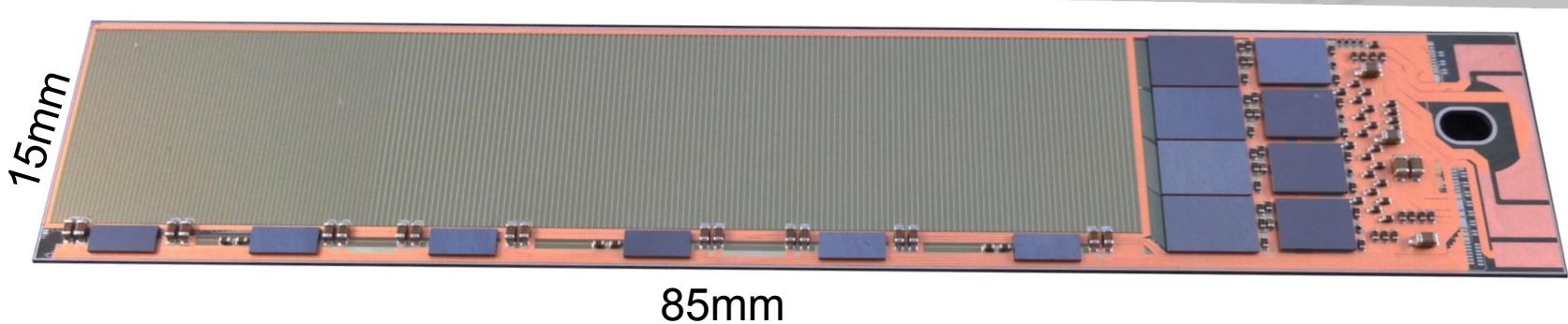
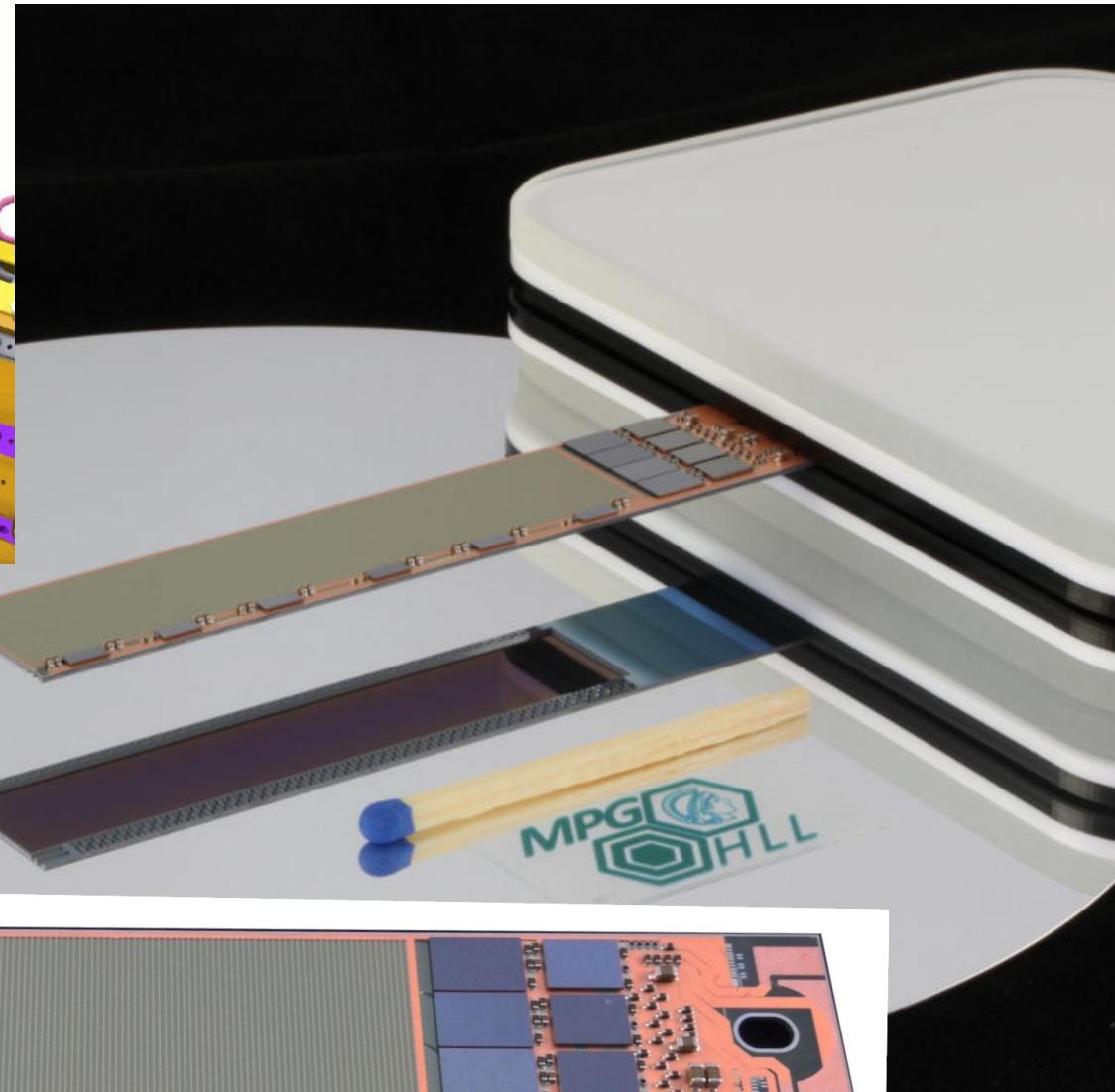
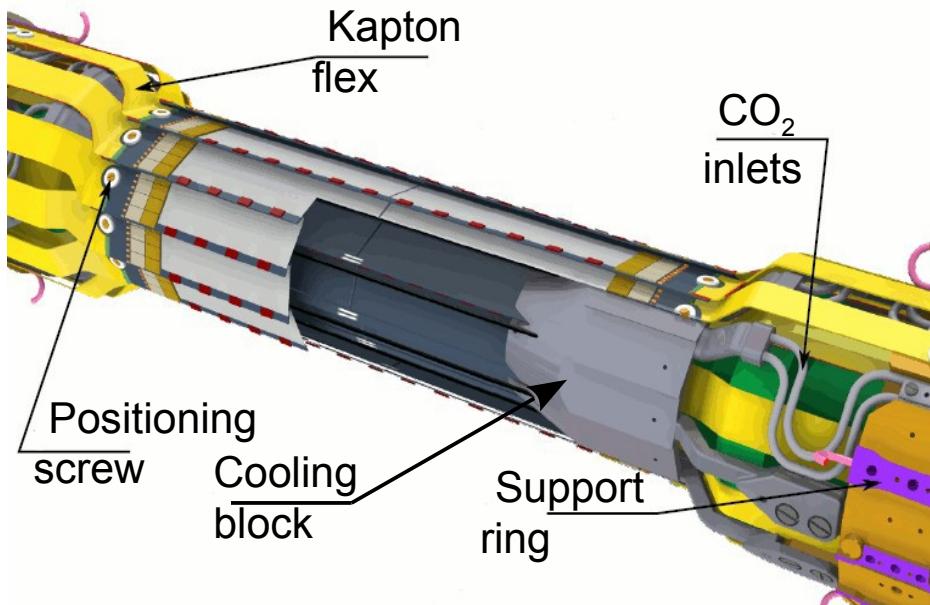
DEPFET ASIC bumping

- Bumping technology for SwitcherB required
 - easy-to-use, low infrastructure requirements
 - gold stud thermocompression already available
 - but: high forces on thinned balcony problematic
 - solder bumps: low force
 - solder allows to rework and repair DEPFET modules
- Solder bumping technology
 - most processes optimized for wafer level bumping:
screen printing, electroplating
 - solder jetting technology is preferred
 - how to add UBM?
 - gold-stud bumps available



SwitcherB (96bumps);
80µm pad 150µm pitch

Assembled DEPFET Module for Belle-II

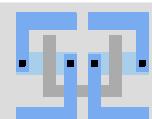


Wire Bonder with Goldstud Bumping

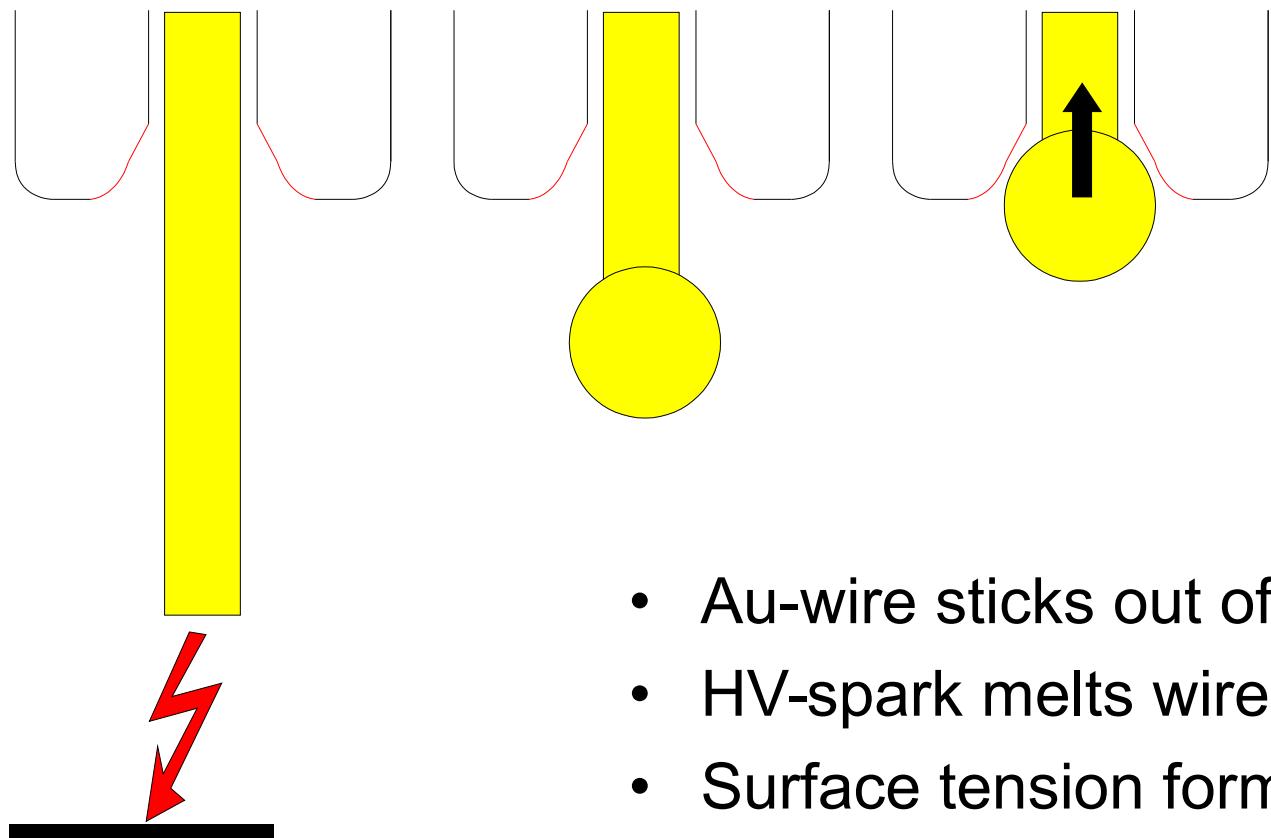
- Half-automatic machine
 - manual placing and aligning of chip (3min)
 - automatic bondprocess (9min/160bumps)
- Modular system
 - Ball-wedge-head for gold bonding and bumping
 - Ball shear tester
 - options: wedge-wedge bondhead, wire pulltester, ribbon bondhead, ...
- Bondprogram conversion tool by SuS
 - draw in wirebonding in Cadence
 - find bumppads in layout



Delvotec 5610

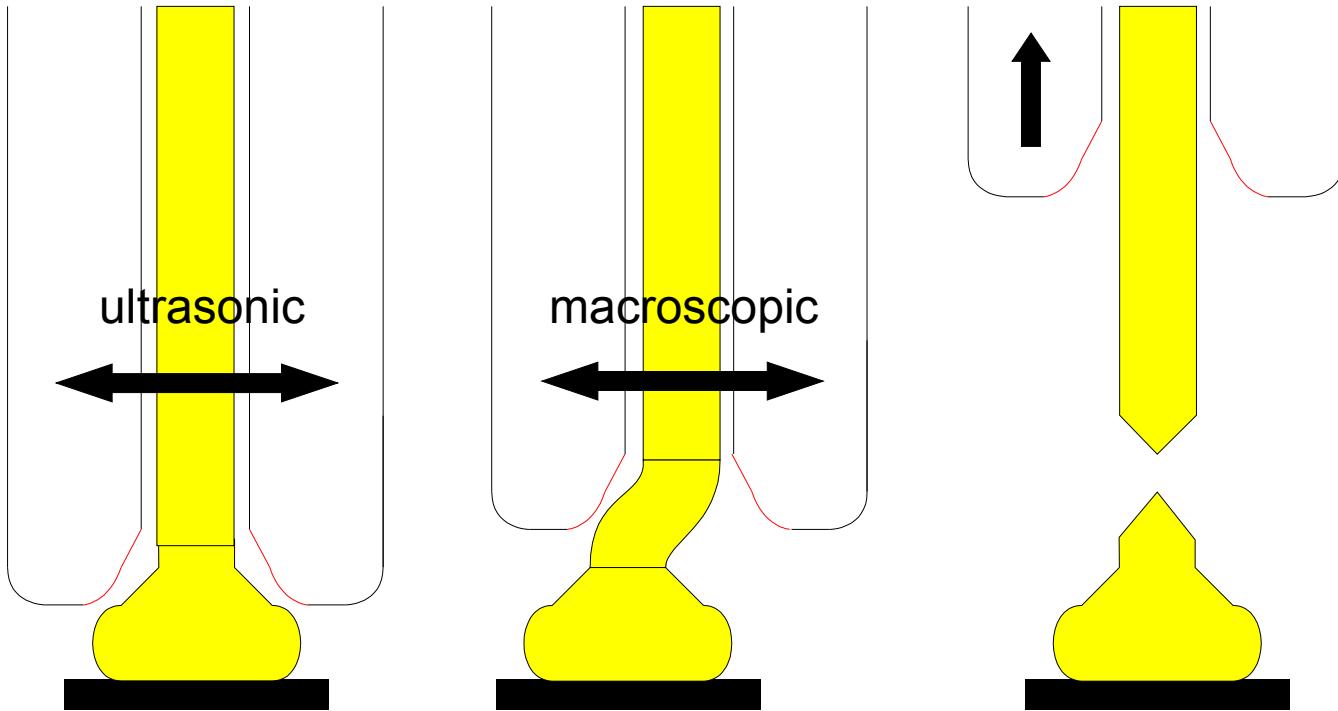


Gold Ball Forming

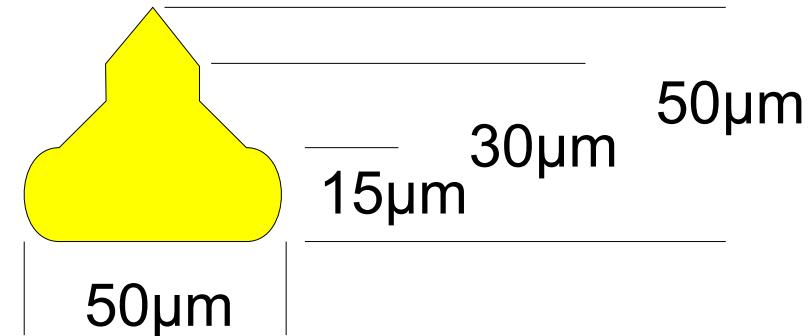


- Au-wire sticks out of capillary
- HV-spark melts wire (“flame-off”)
- Surface tension forms free-air-ball
- Vacuum pulls ball to capillary

Ball Bonding

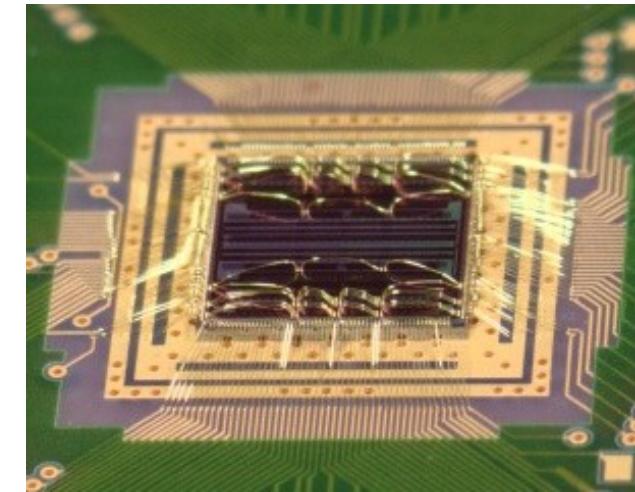
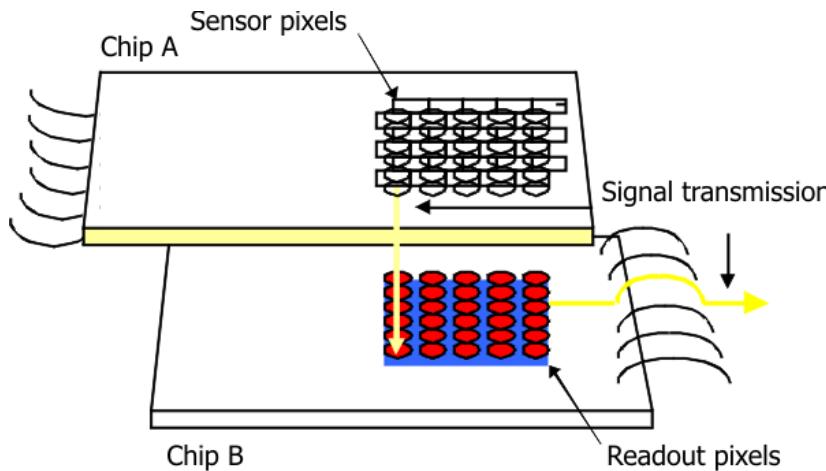


- Capillary presses ball onto Al-bondpad and forms bump
- Ultrasonic to form Au-AI interconnection
- Shear-off wire near the bump
- Pull up capillary and rip off

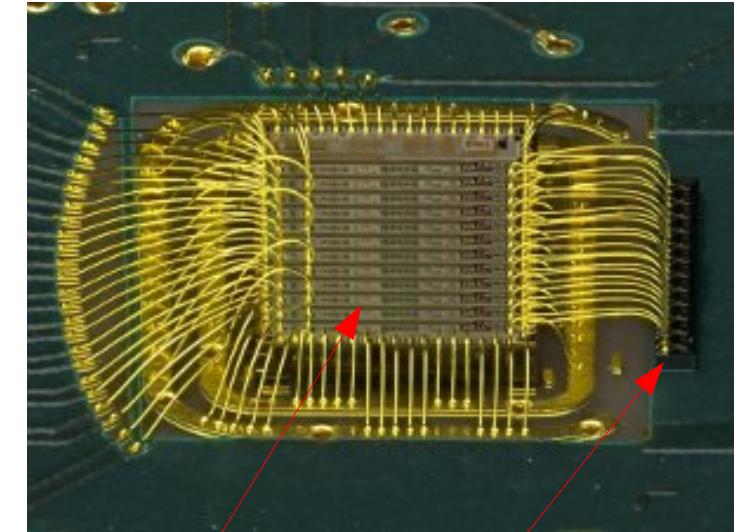
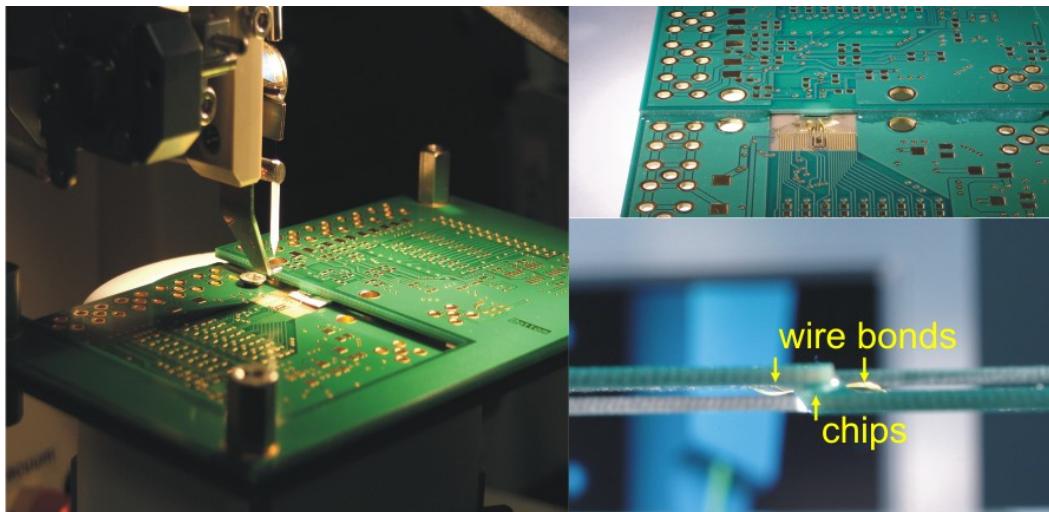


Ball-Wedge Wirebonding

Capacitive Coupled Pixel Detector

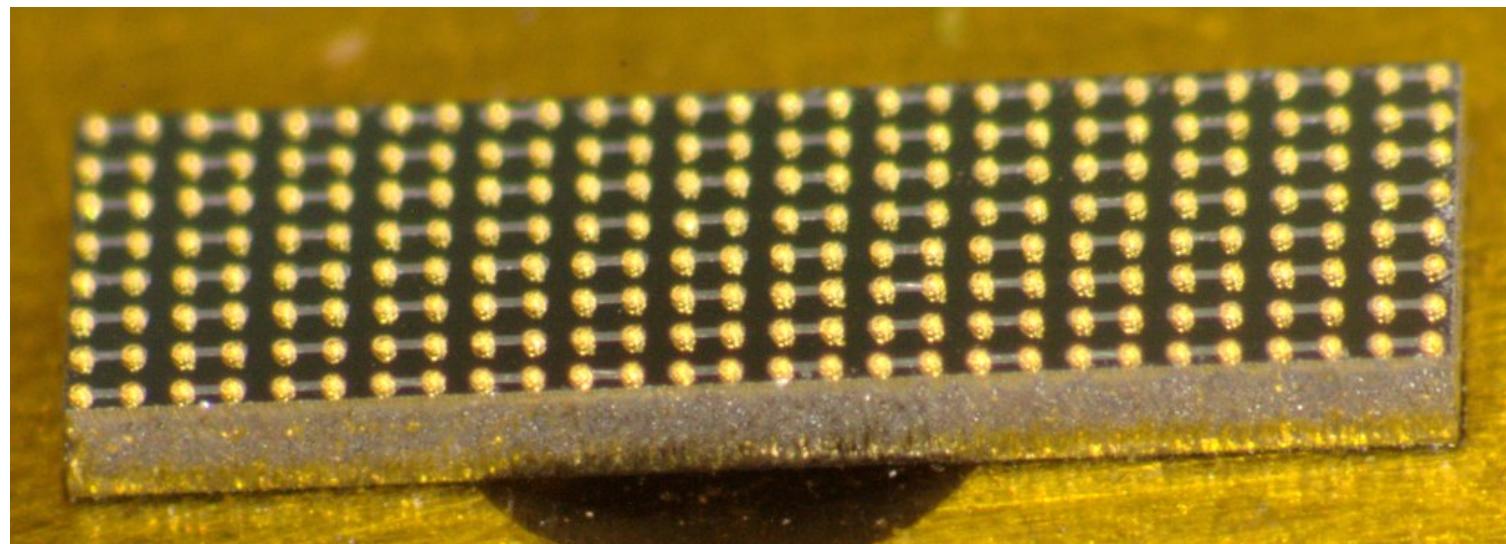


PET Chip with stitch bonds

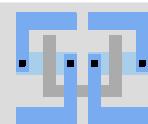
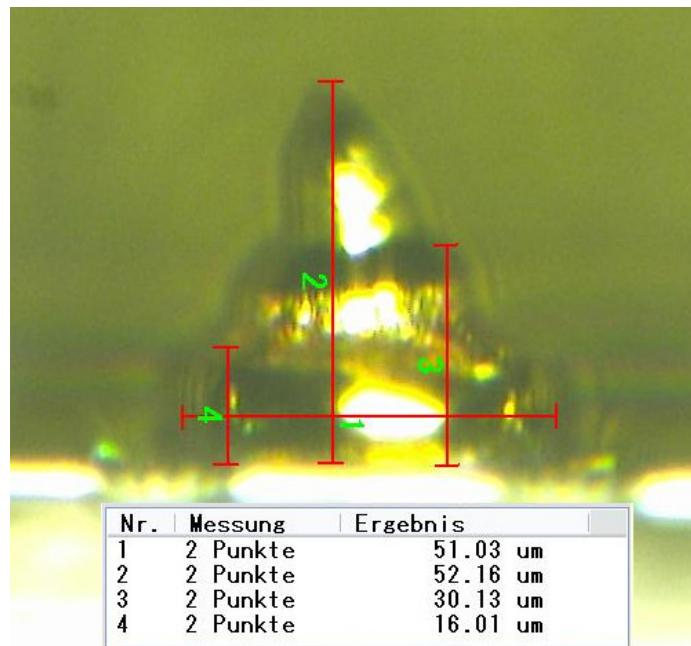
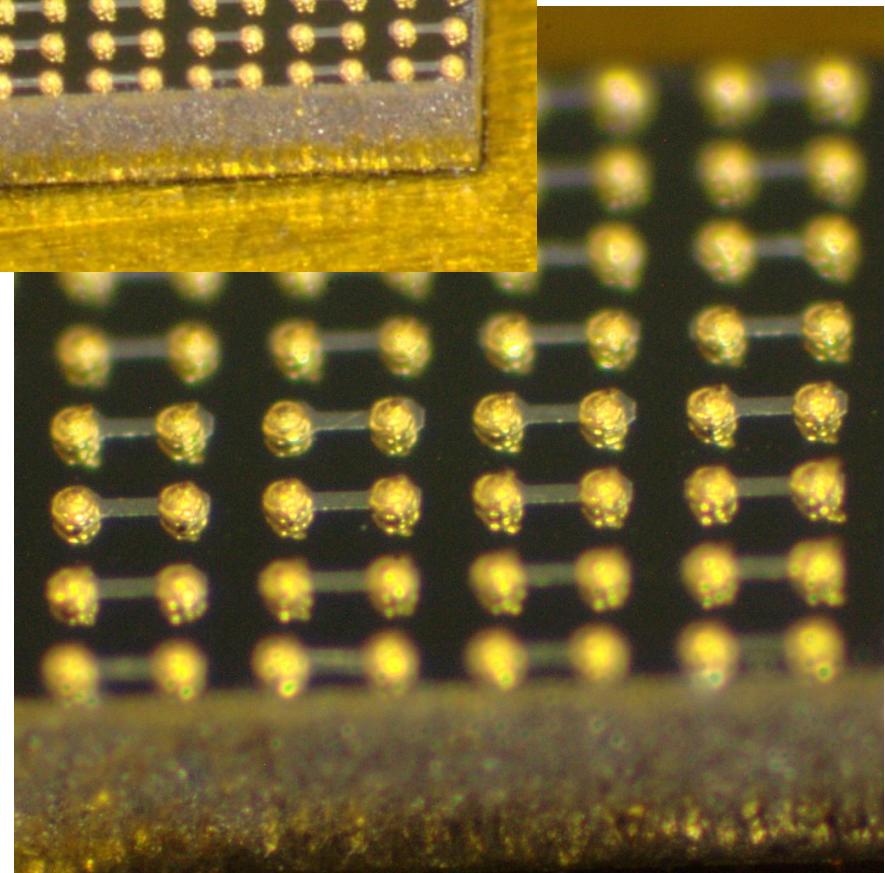


VcSEL driver with diode array

Goldstud Bumps

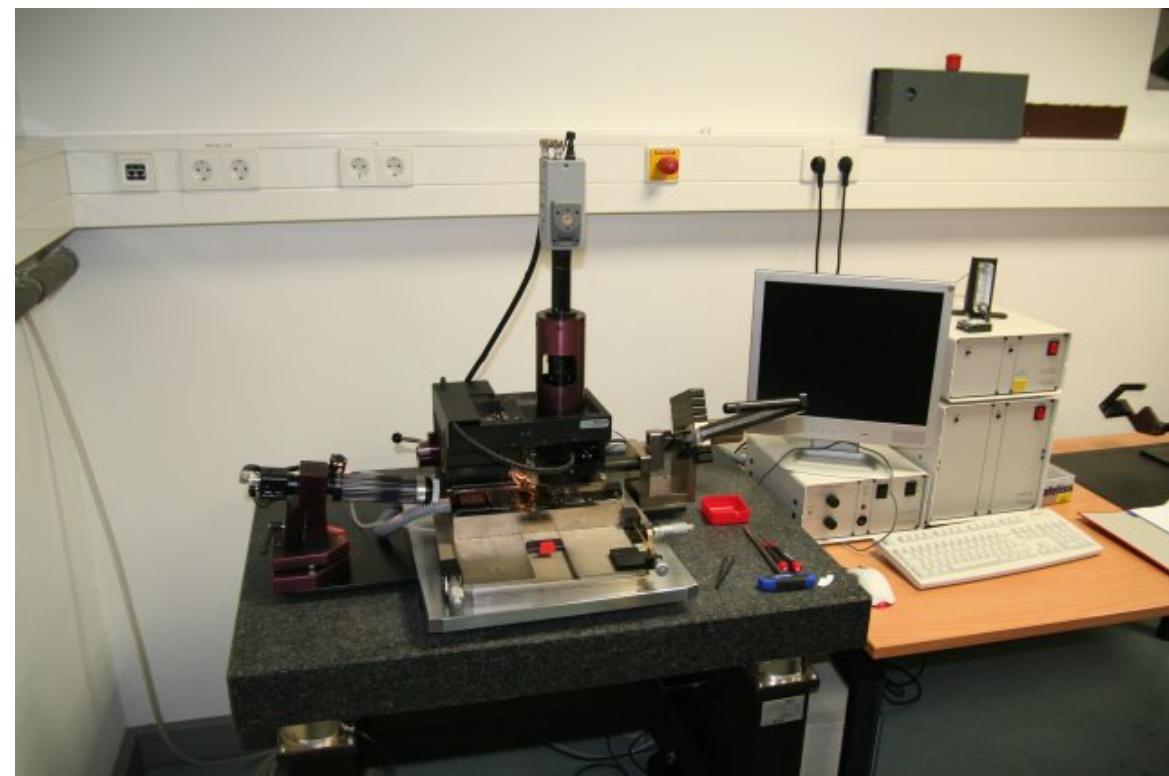
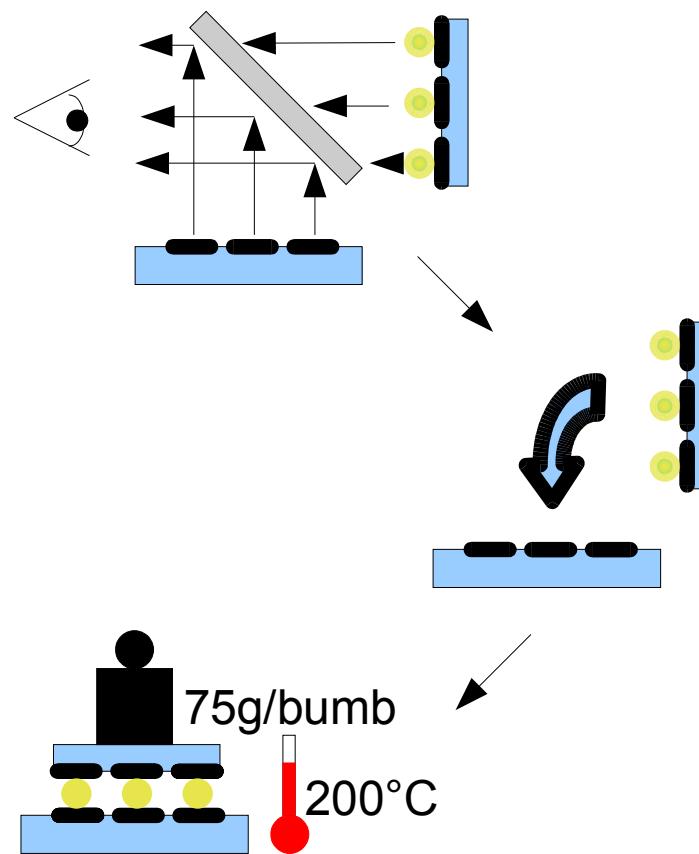


224 bumps
1,35 x 4,95mm²



Flip-Chip

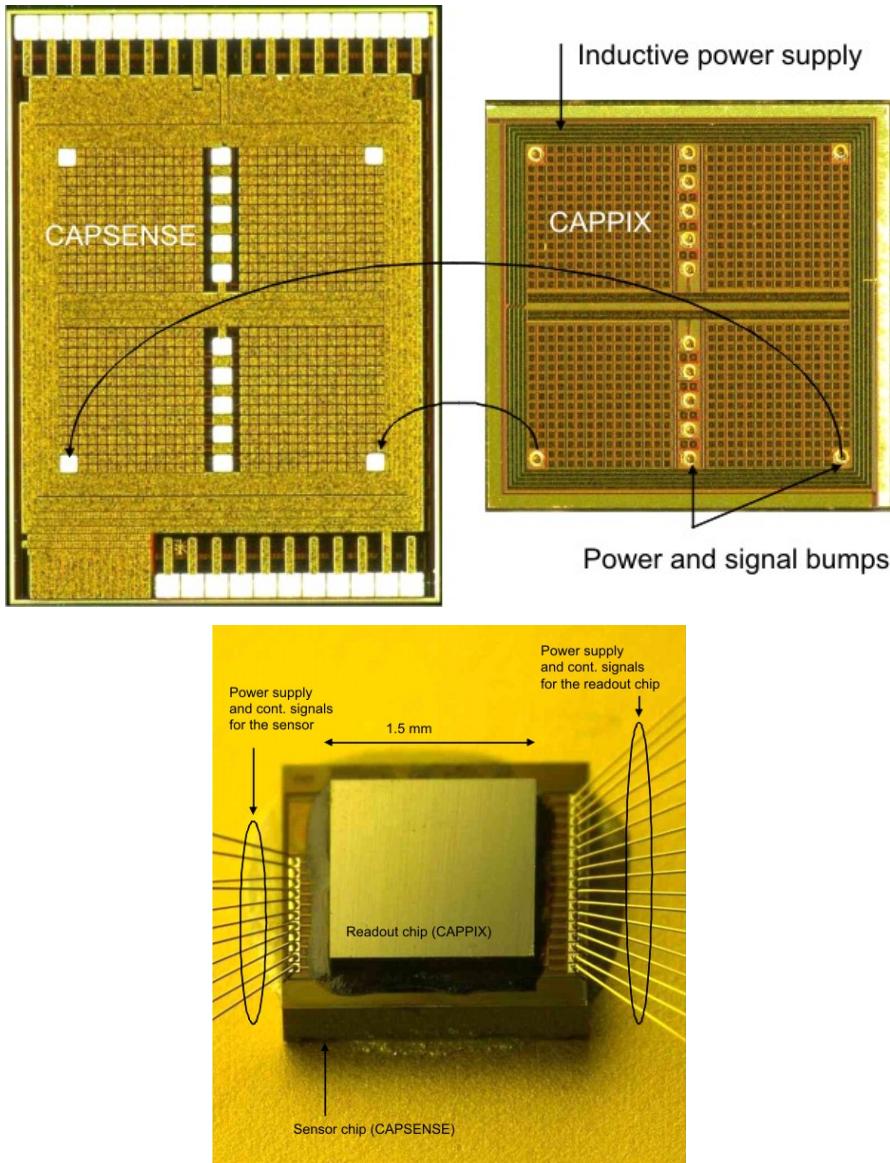
- Pads of substrate and bumps on chip are optically aligned
- Chip is pushed onto substrate
- Temperature profile and static force applied
- Nitrogen atmosphere option for soldering



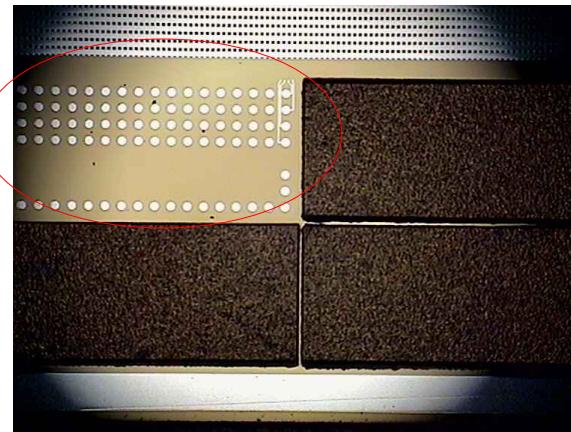
Finetech Lambda, 1µm precision,
400°C, 20K/s, 200N

Goldstud Flip-Chip Bonding

Capacitive Coupled Pixel Detector v2

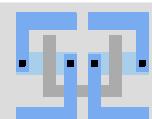
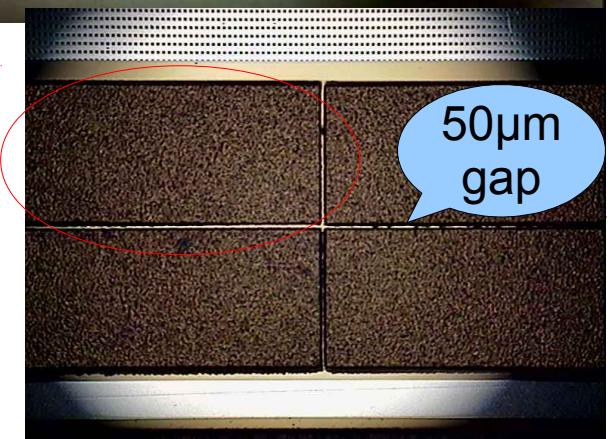


Empty landing area

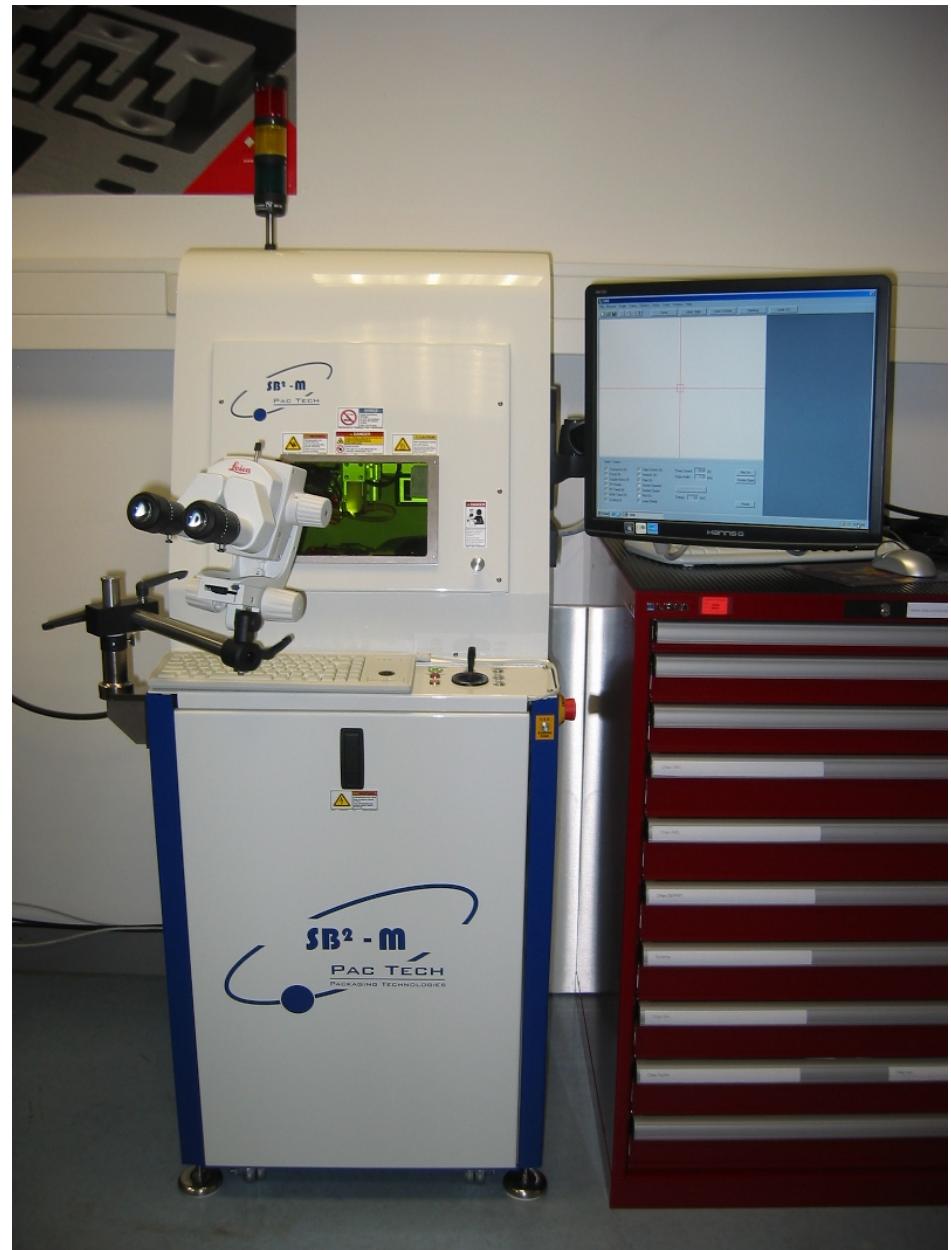


Sideview of flip-chip placement

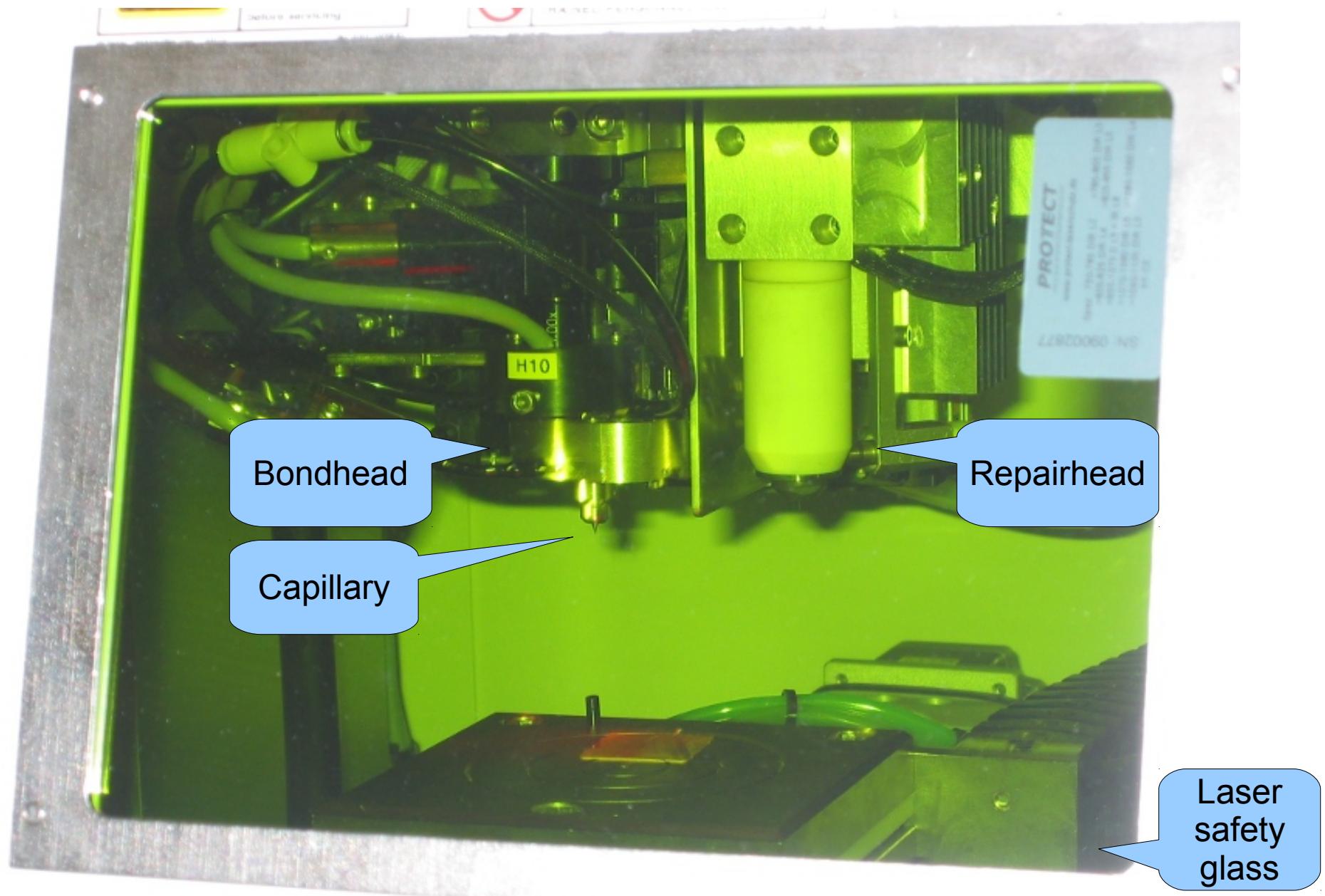
Chip bonded



- Deposit single solder balls
- 60µm solder balls SnAgCu
 - 40µm...760µm possible
 - Max. 5 balls/sec
- Melts ball with 20W IR laser
 - Laser enclosed in housing
 - no laser safety area required
- Low infrastructure requirements
 - pressured air
 - nitrogen

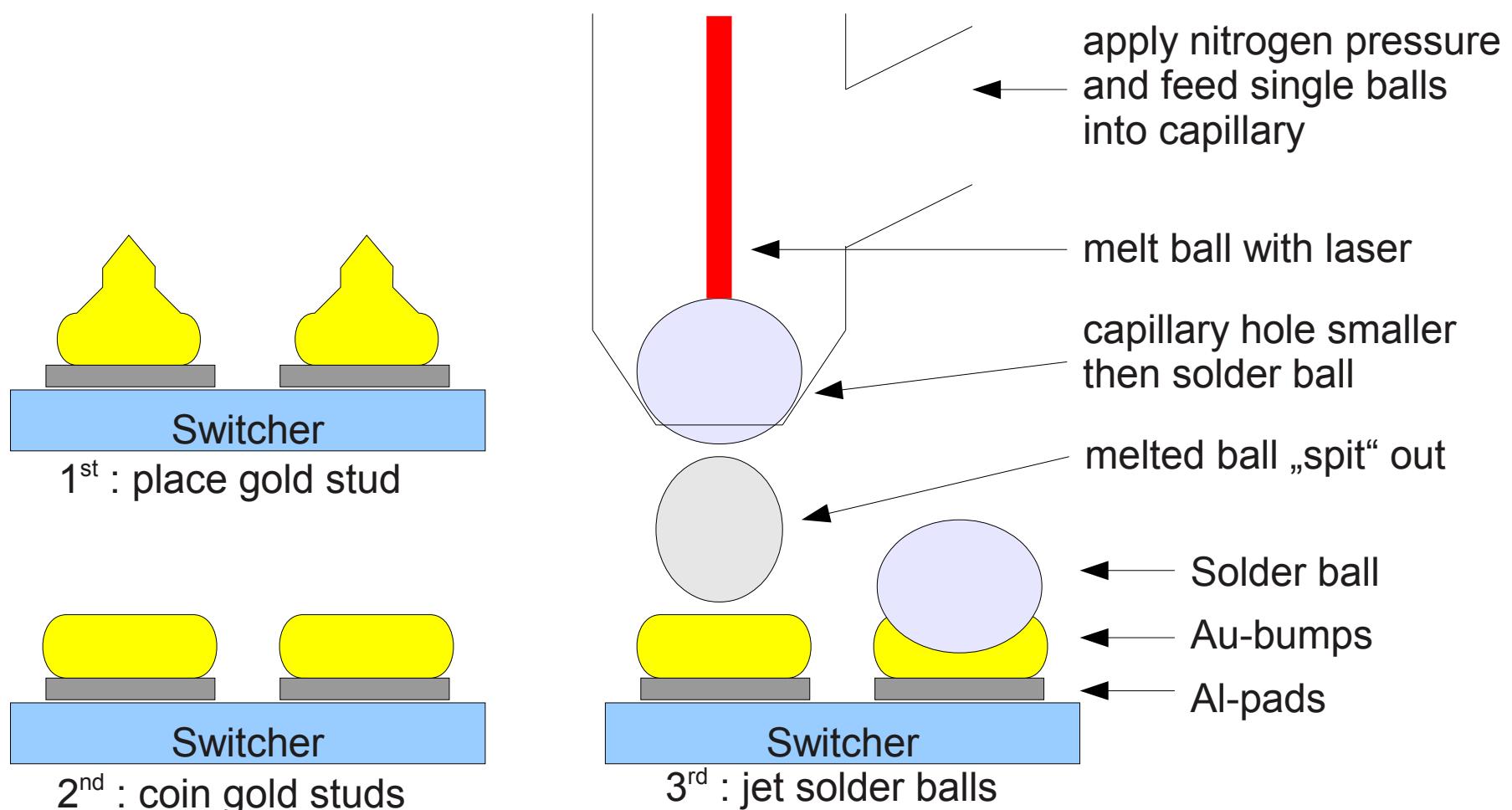


Bond- and Repairhead



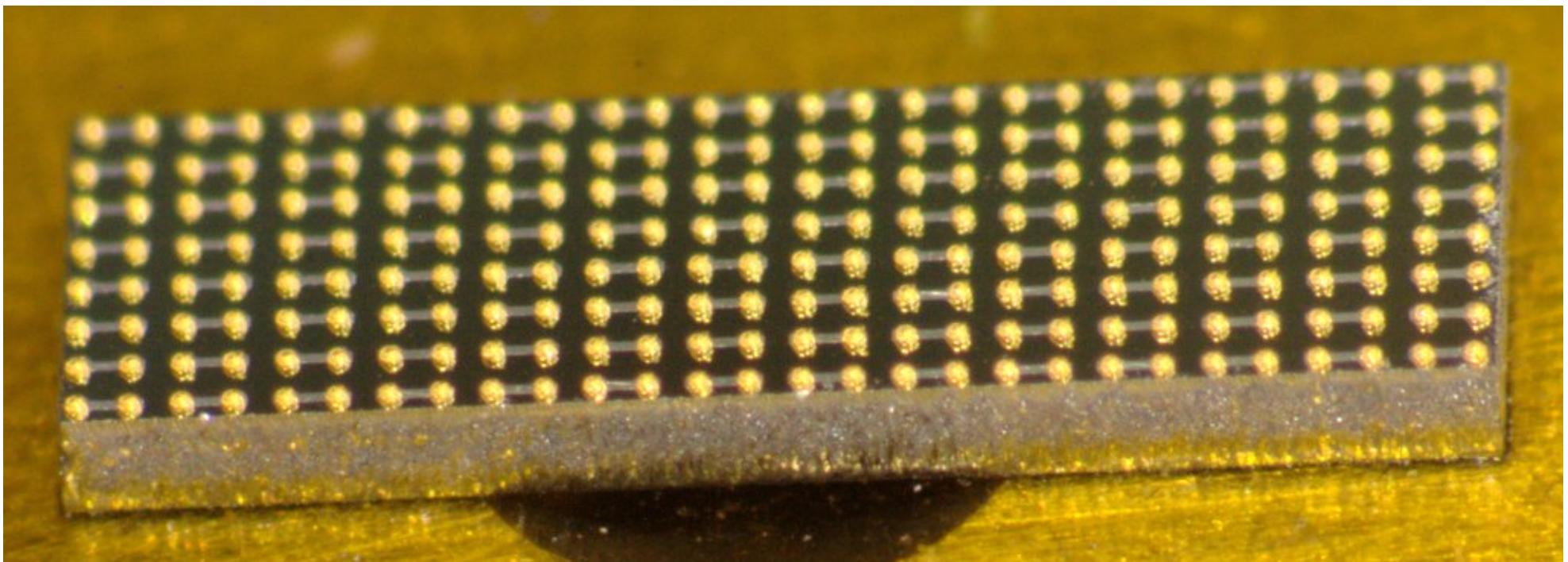
Single Chip Solder Bumping

- Use coined gold studs as an under bump metallization
- Place solder bumps on top using PacTech solder jetting technology



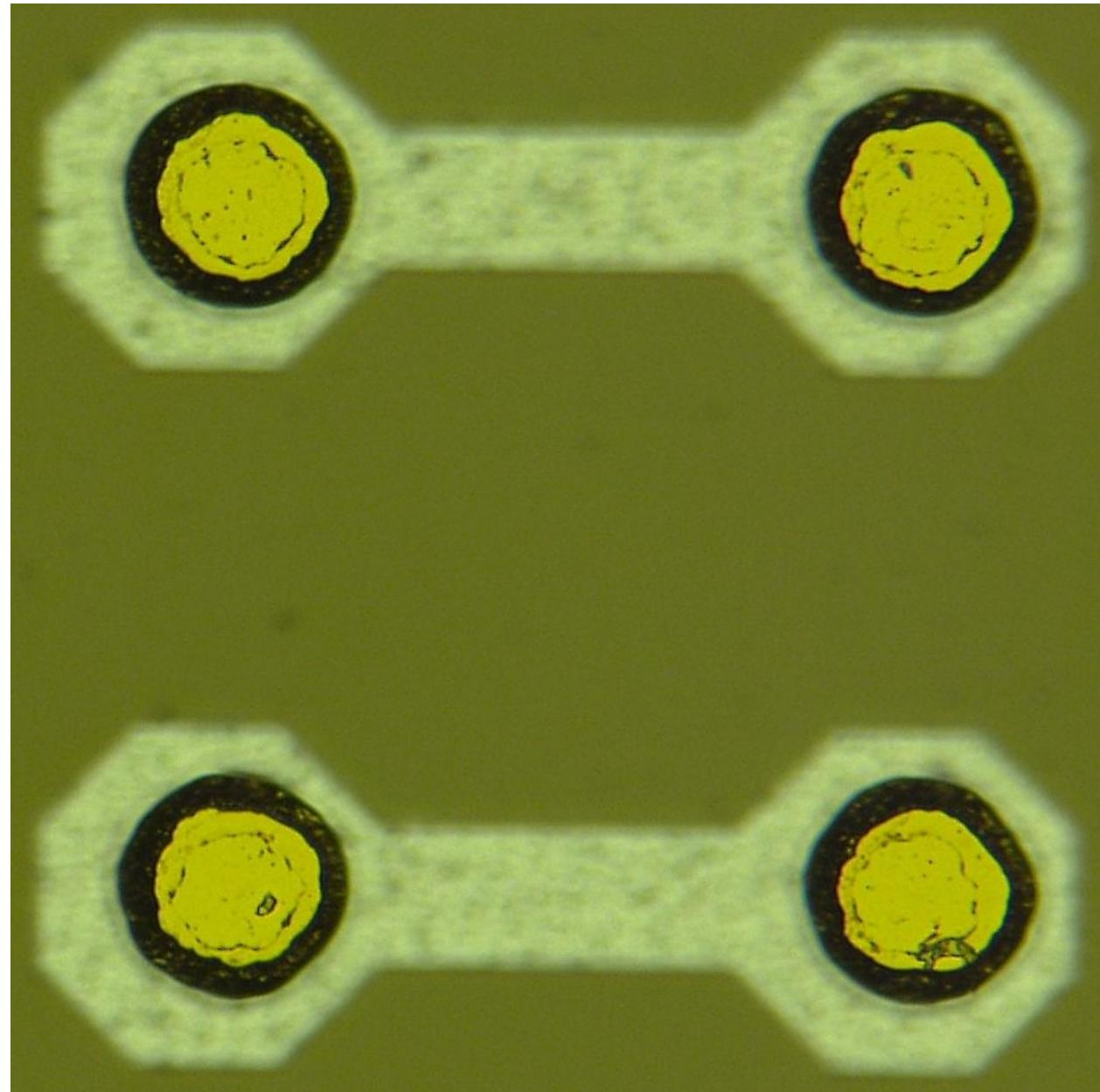
Gold Stud Bumping

- Place gold studs on chip and substrate
- Coin studs on chip to remove tail on top and create a flat surface
 - using flip-chip machine and big piece of silicon



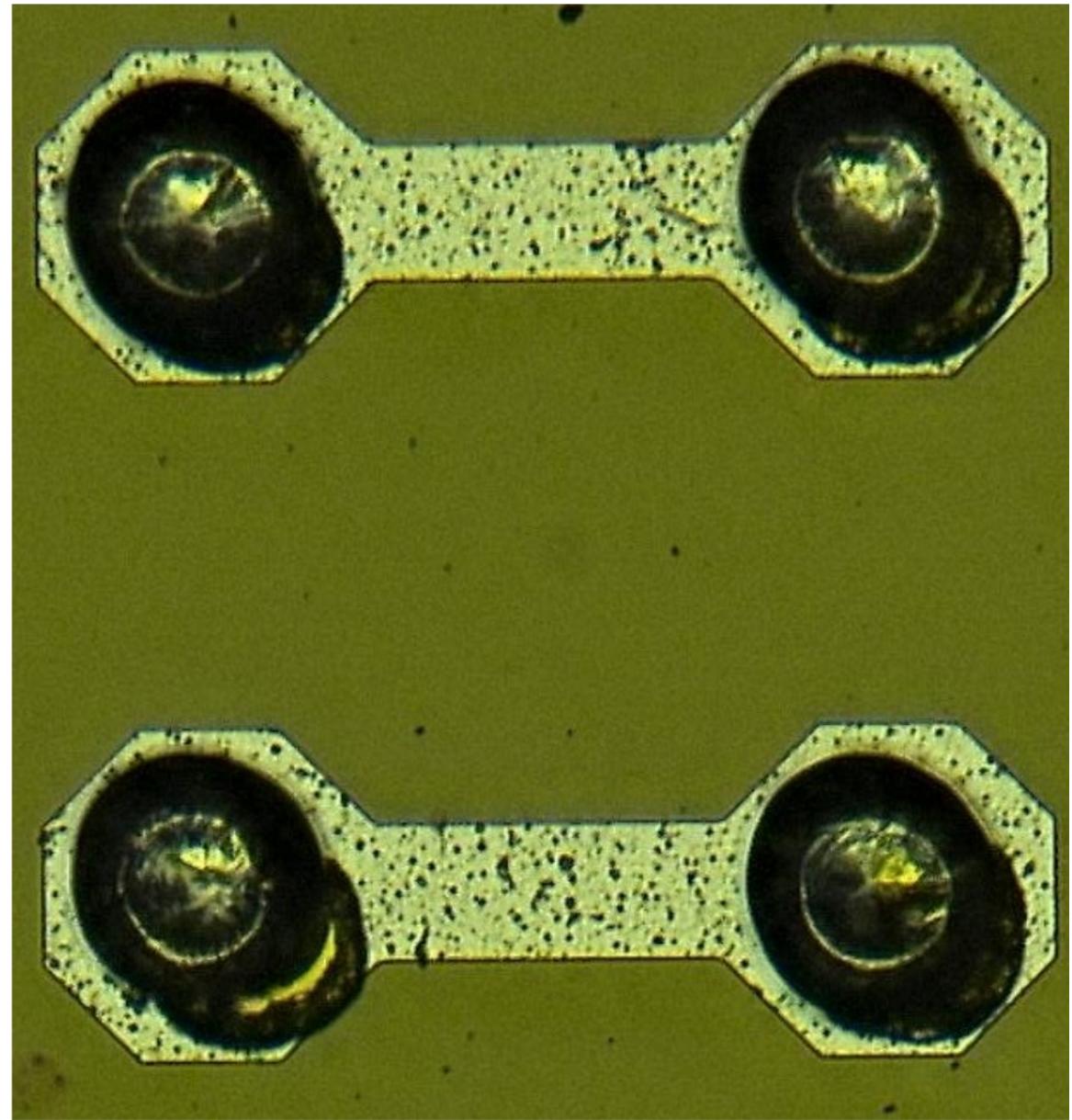
Gold Stud Dimensions

- 58 μ m bump diameter
- 42 μ m flat diameter

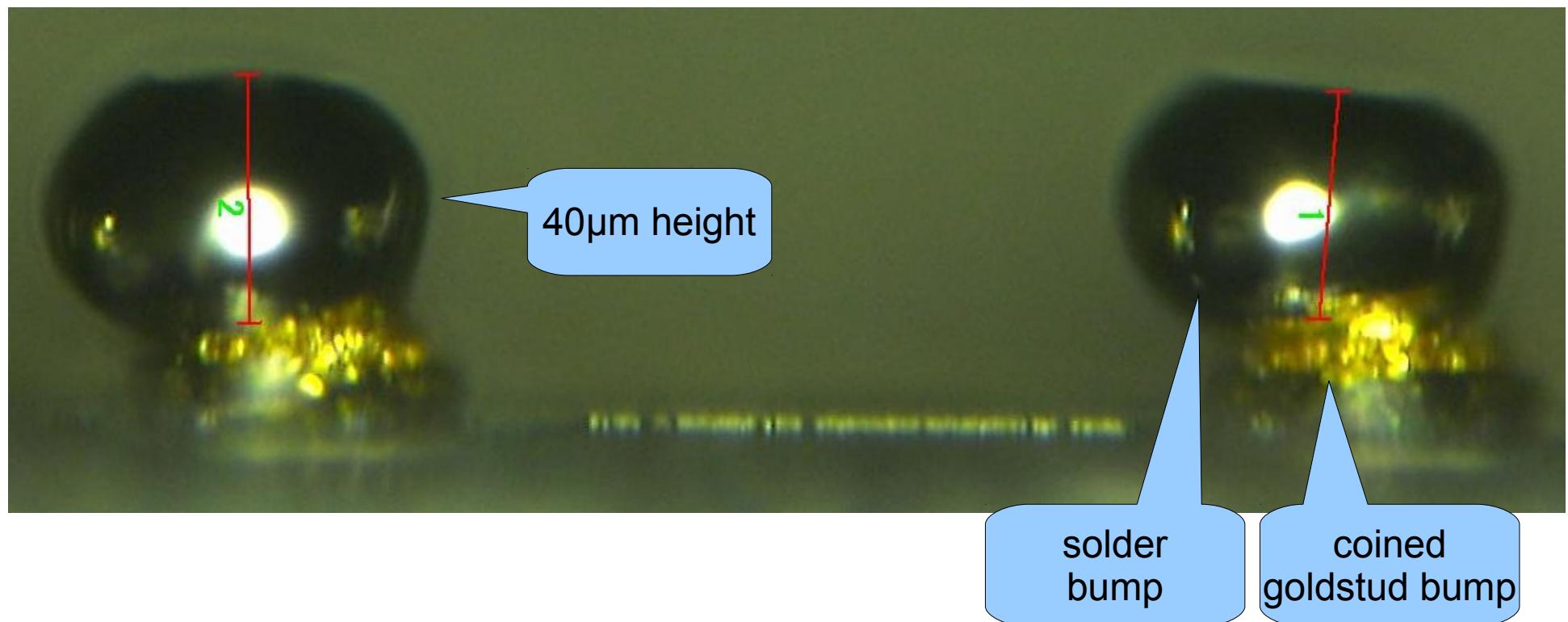


Solder Bumping

- Ball diameter: 67 μ m

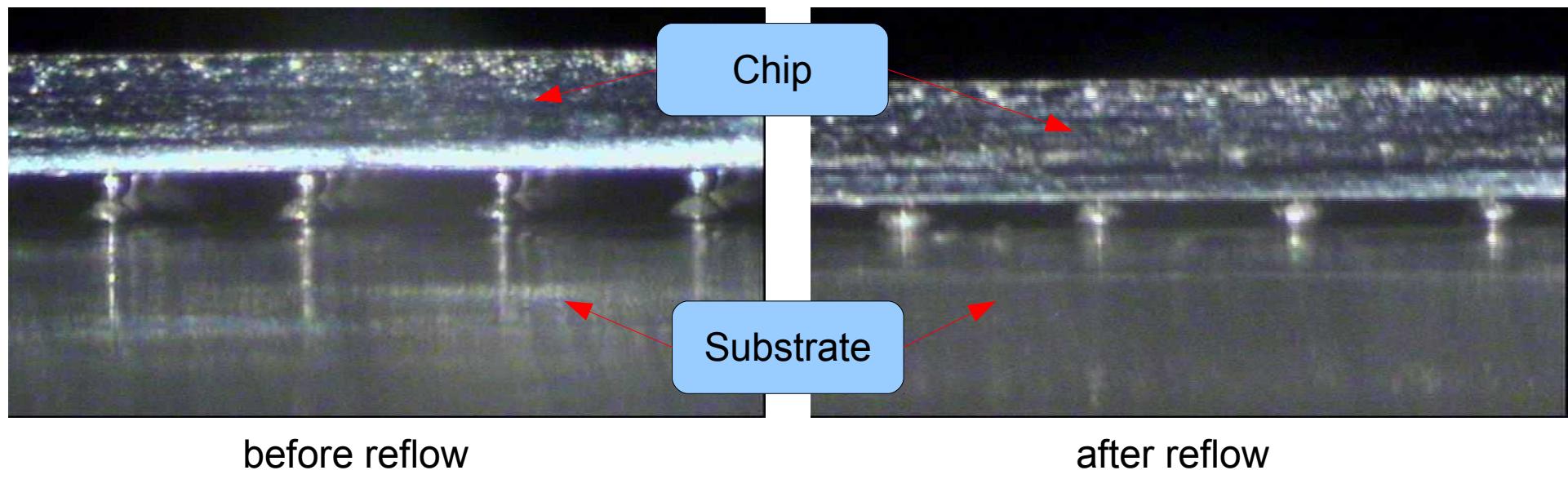


Solder Ball Side View



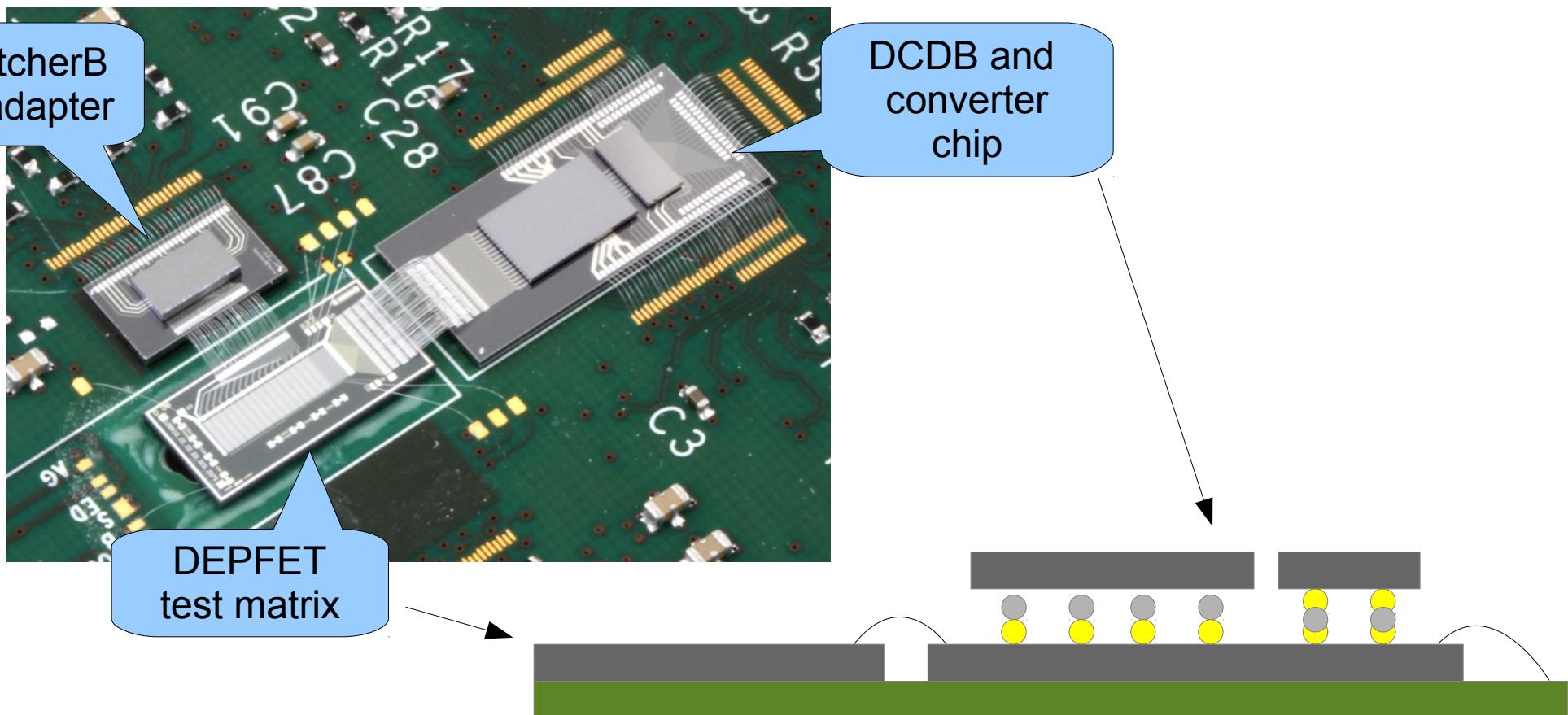
Soldering

- Soldering in Finetech flip-chip machine
- Flux applied to substrate
- Nitrogen atmosphere with ramped temperature profile
- Flux cleaning in ultrasonic bath



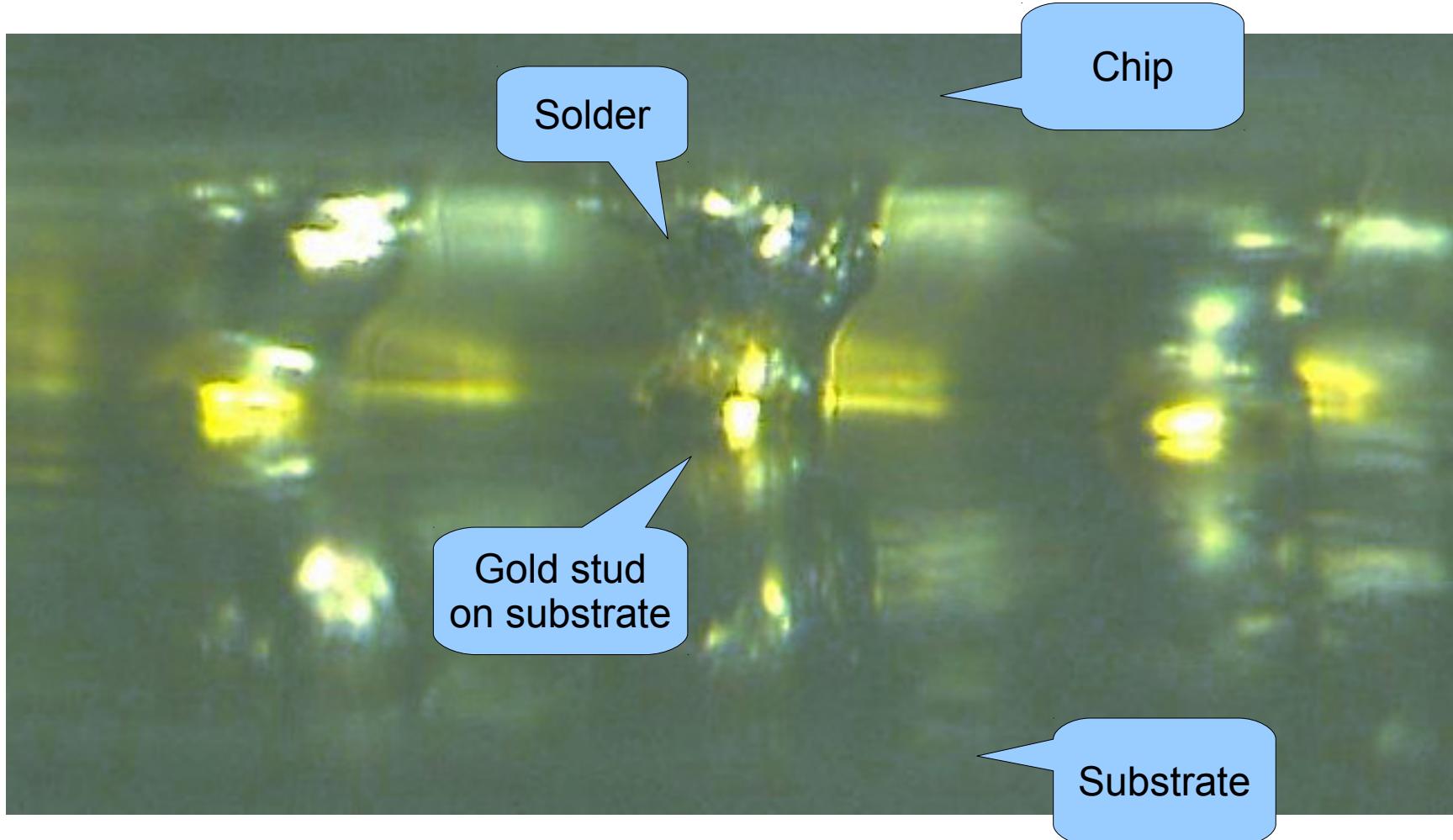
Wire Bond Adapters for DEPFET Test Systems

- Flip-chip only read-out and steering chip
- Wire bond only DEPFET test matrix
- Need wire bond adapters for test systems
 - gold studs as under bump metallization



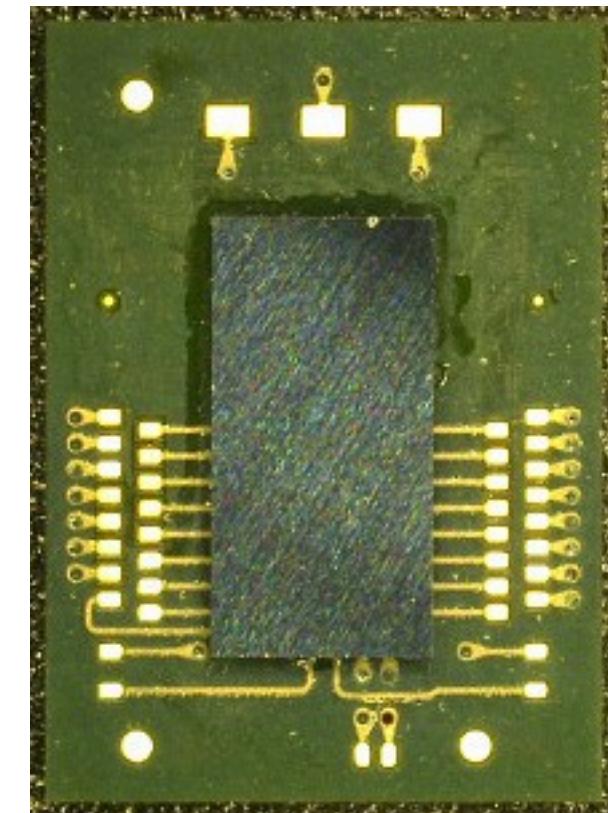
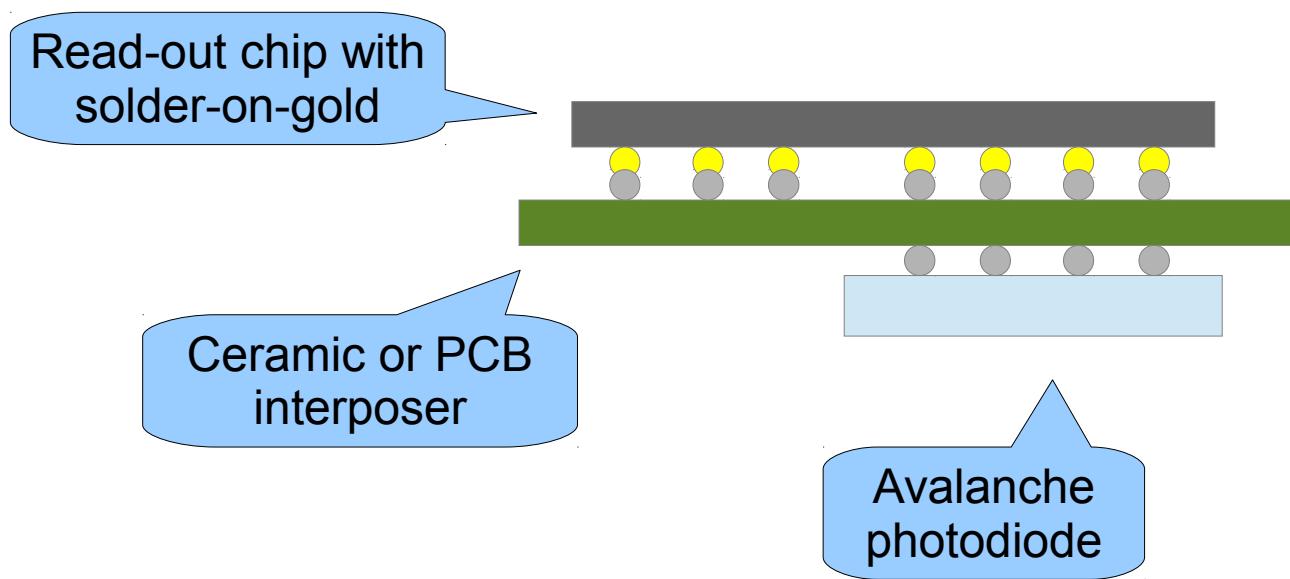
Flipped Side View

- Solder balls compensate ball placement error



Solder Bumping at XNAP

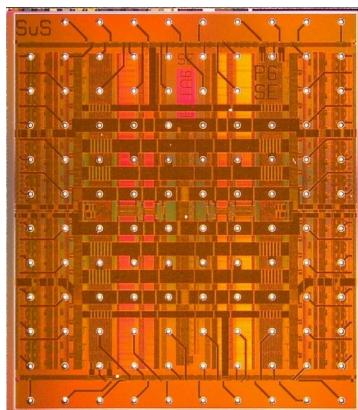
- X-ray diffraction and imaging with avalanche photodiodes
- Detector is sensitive to pressure
 - solder bumping used for test assemblies



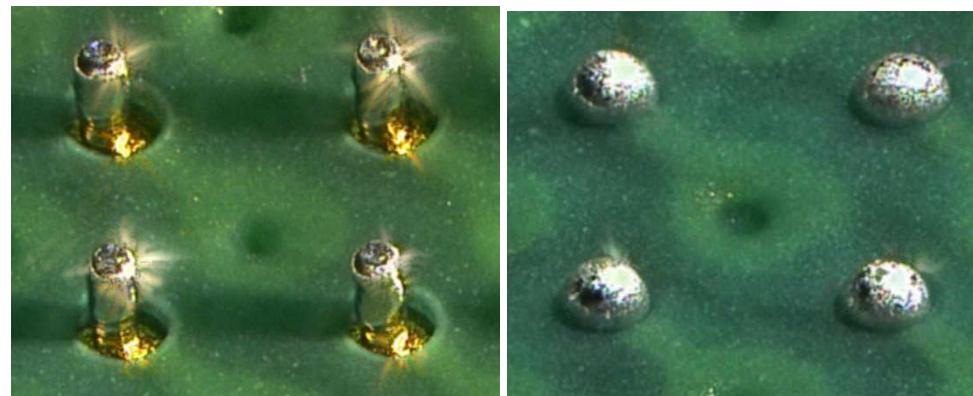
Top view: read-out
chip on interposer

Bump Stacking

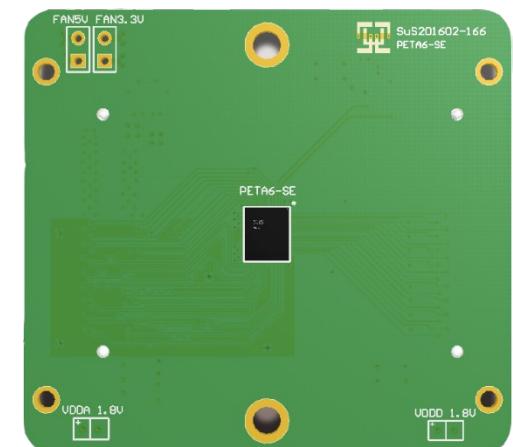
- Stack multiple solder balls to increase solder volume
 - chip-on-board with 100µm balls
 - large pads on PCBs need more solder than 100µm ball provides
 - place balls on PCB and reflow
 - add underfill



5x6mm² PETA6SE
ASIC with 100µm balls
and 500µm pitch



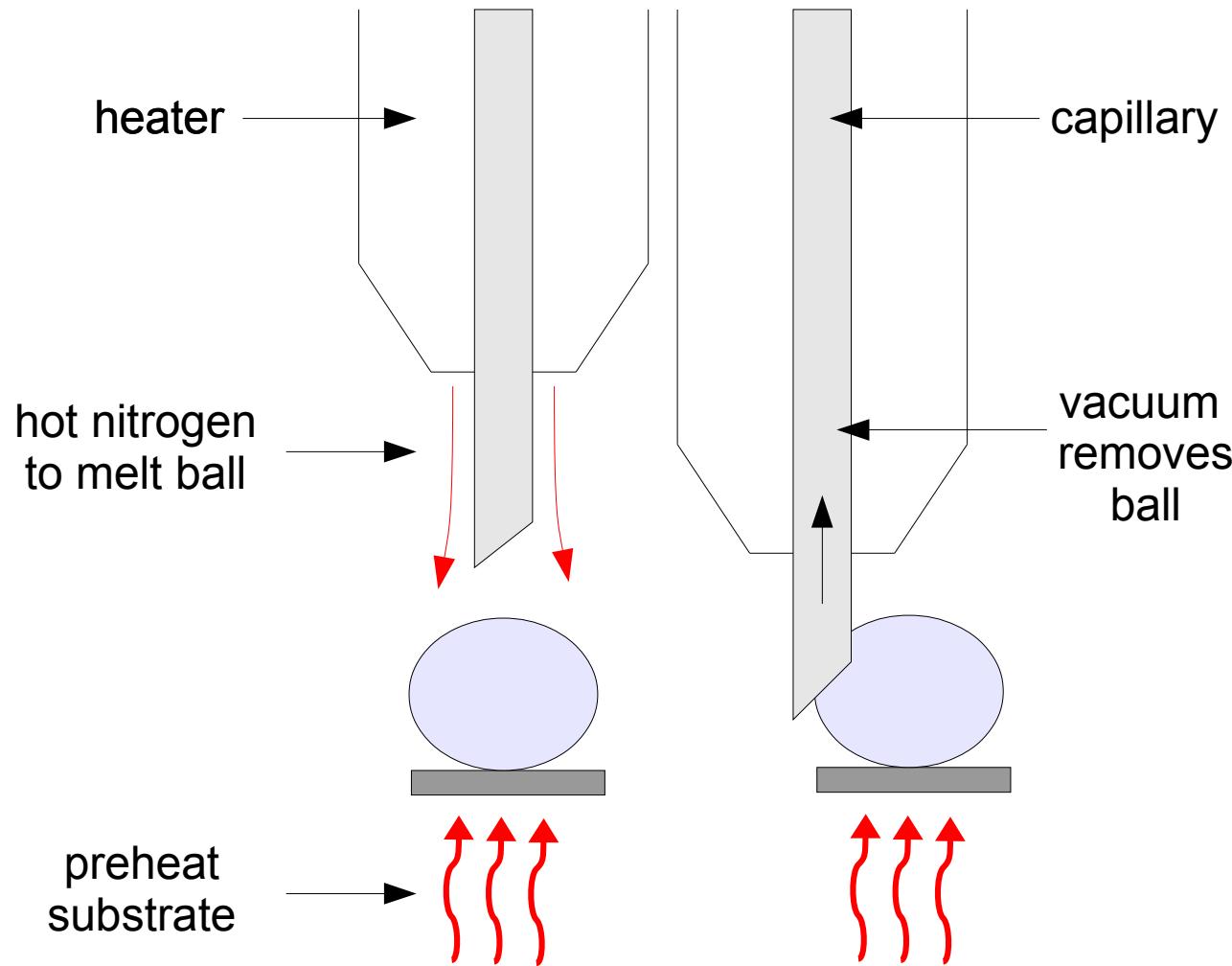
stack of 14 solderballs of 60µm diameter before and after reflow



Chip-on-Board

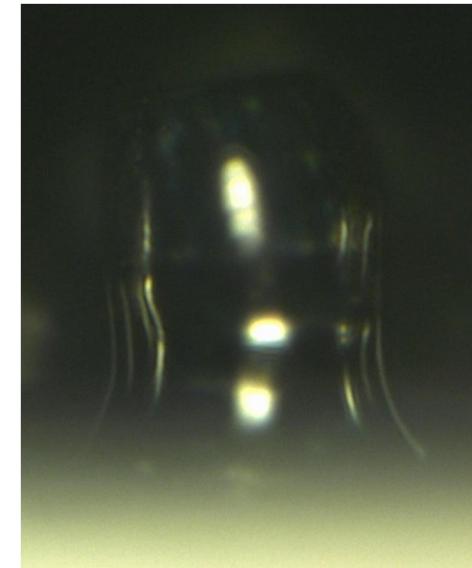
Solder Removal

- Repair head allows selective removal of solder
 - Option for PacTech machine

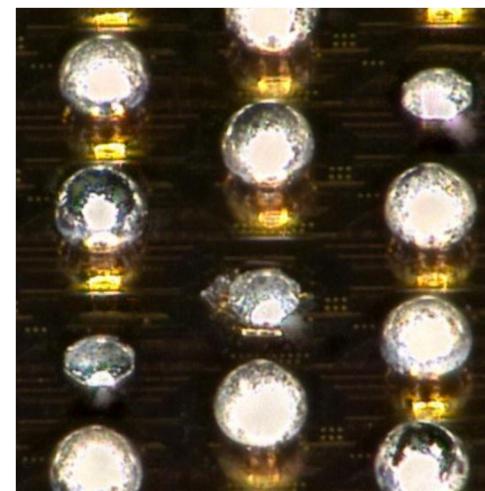


Ball Removal / Reballing

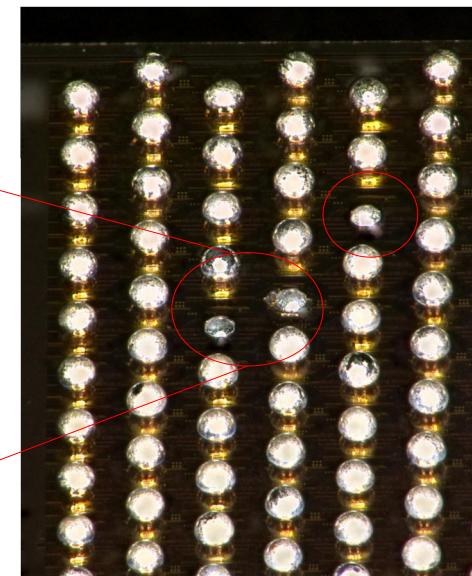
- Reballing of rare chips
 - chips have been desoldered from substrate
 - remaining solder has been removed
 - solder jet multiple 60 μm balls to increase final ball size
 - reflow to reshape ball stack
- Removal of single balls
 - disconnect inputs of readout chip from high current pixels
 - selectively remove single balls using repair head
 - reflow to reshape adjacent balls and solder remains



stack of 6 balls before reflow,
128 μm diameter after reflow



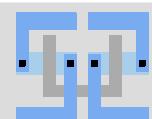
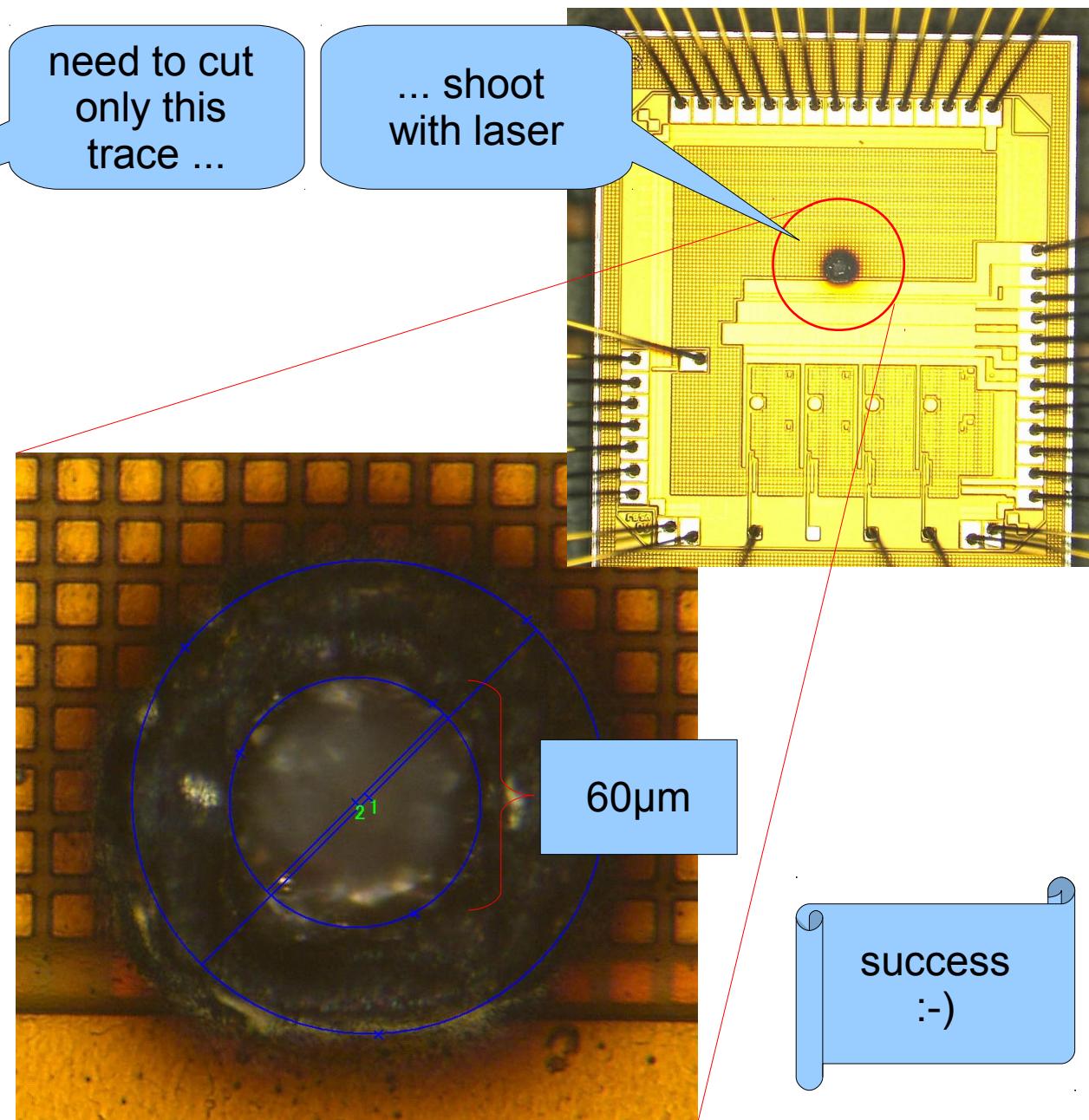
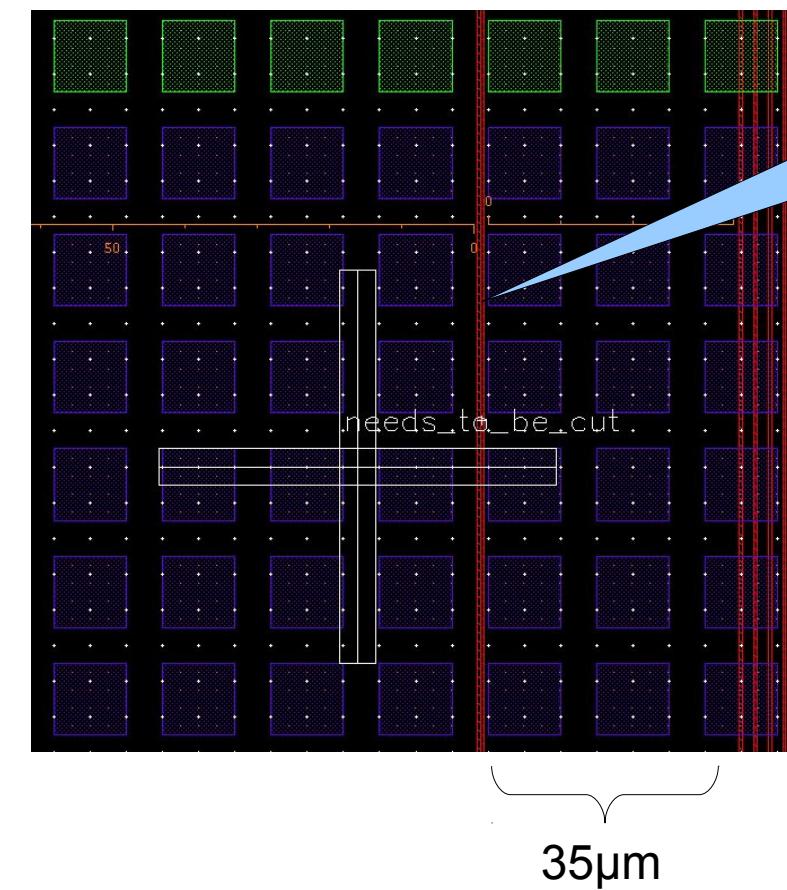
100 μm diameter, 200 μm pitch



removed single solder bumps

- Flip-Chip allows highly integrated, mechanically robust multi-chip-modules with good signal integrity
- MPW production with bumping can be troublesome
- Solder baller offers a flexible solution for single chip bumping
- Suitable UBM is required on both sides! Can use gold studs
- Successfully used in Belle-II prototyping (Switcher chips) and for XNAP (APD array prototype)
-

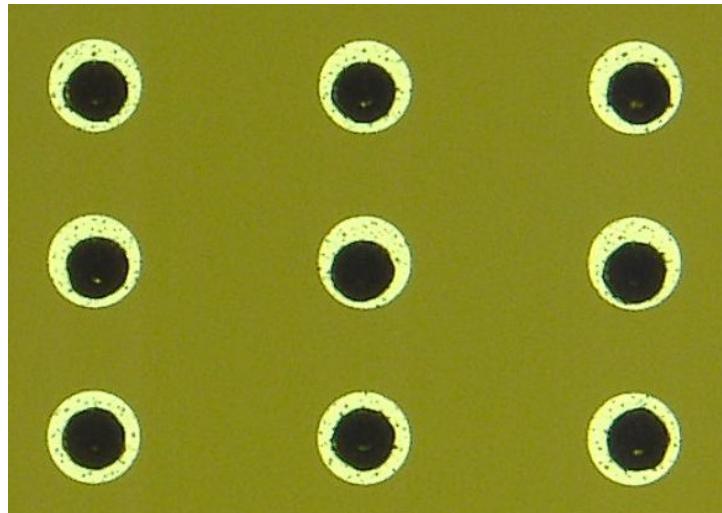
Fun with Lasers



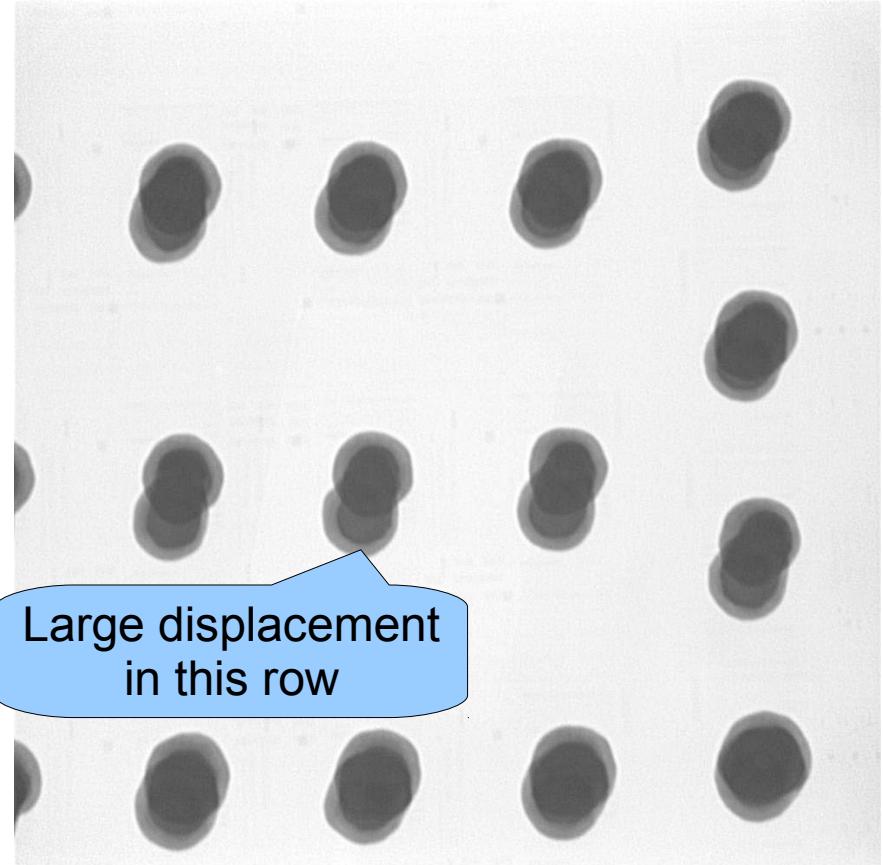
Thank you!

Gold Stud Misalignment

- Gold stud placement error of bonder
 - unconnected bumps



Photograph of gold studs
on substrate



X-ray image of flipped assembly