



NETZWERK
TEILCHENWELT



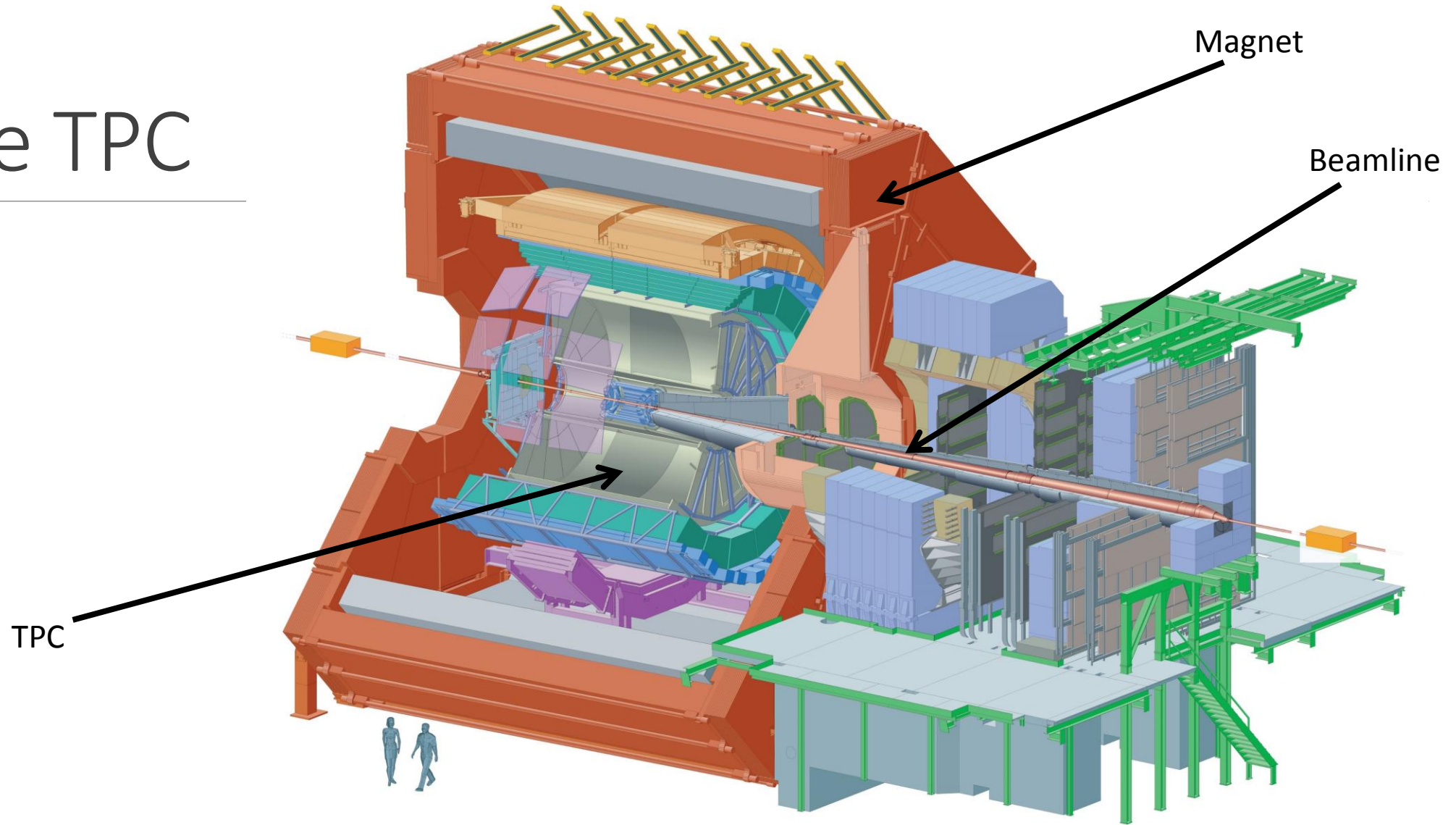
Verhalten der neuen Ausleseelektronik an der TPC

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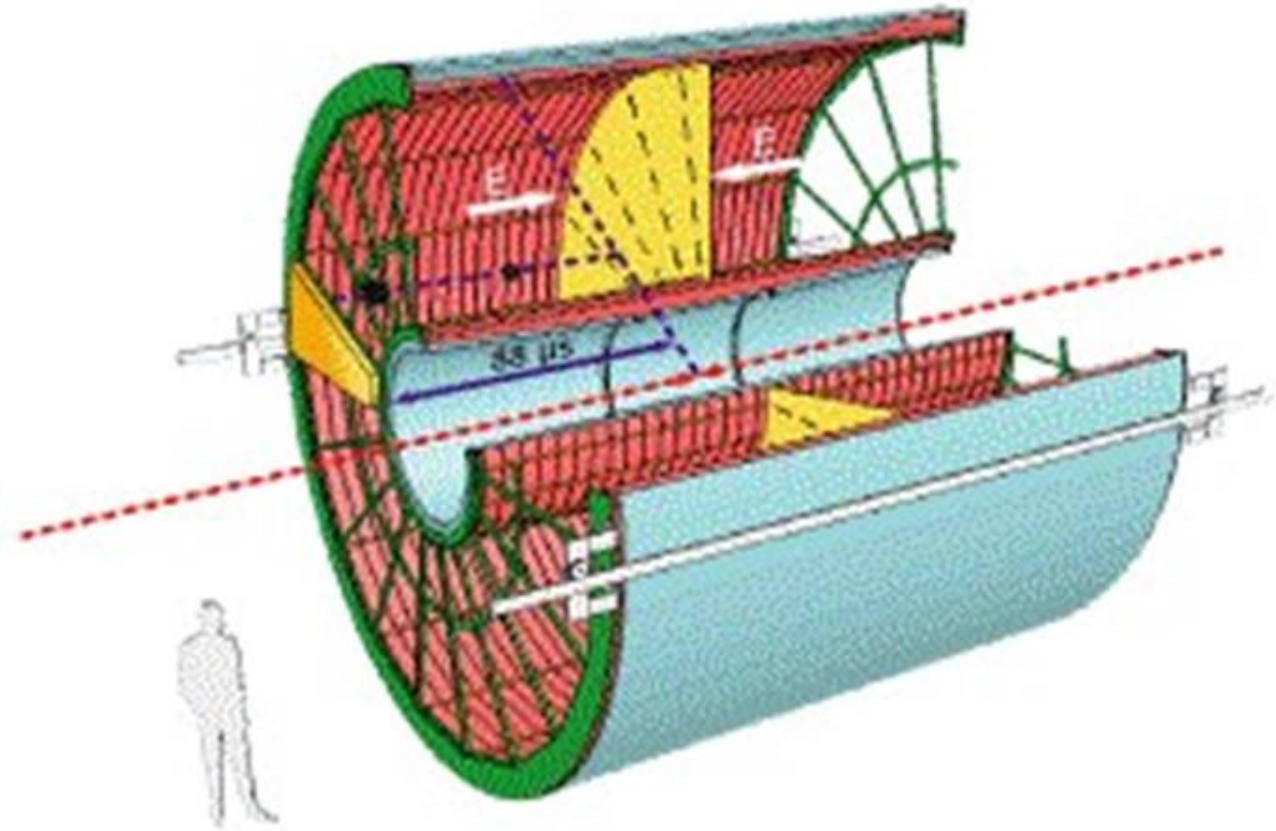
Die TPC



<http://aliceinfo.cern.ch/Public/en/Chapter2/Chap2Experiment-en.html>

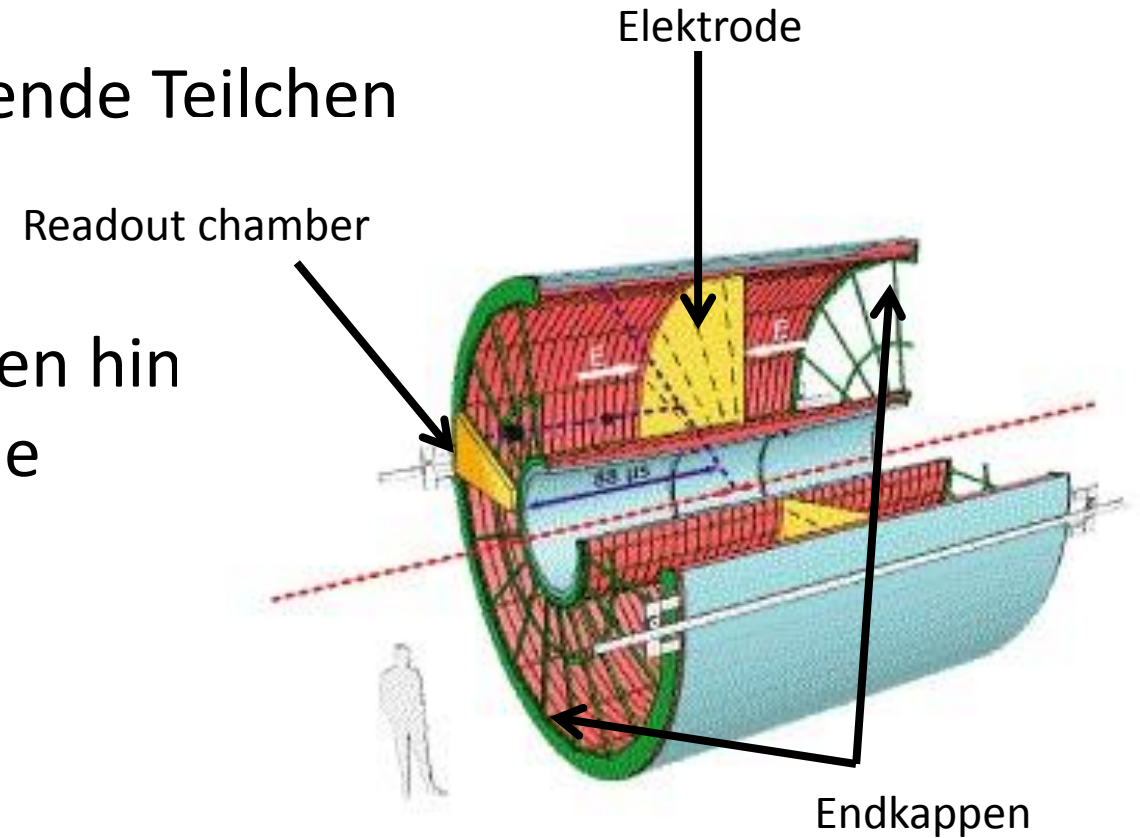
Die TPC

- Spurendriftkammer
- „Herz“ von ALICE
- $V=88\text{m}^3$
- Ne/CO₂-Gas



Funktionsweise der TPC

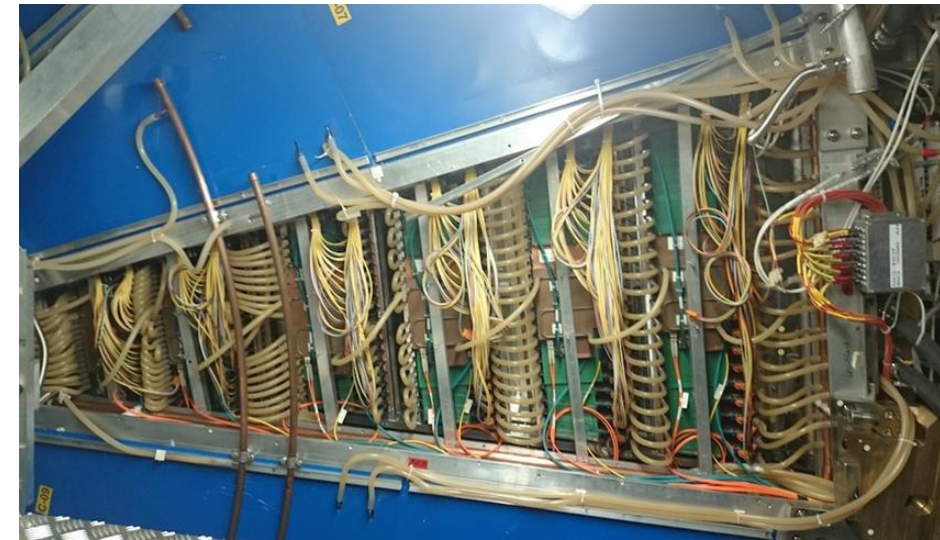
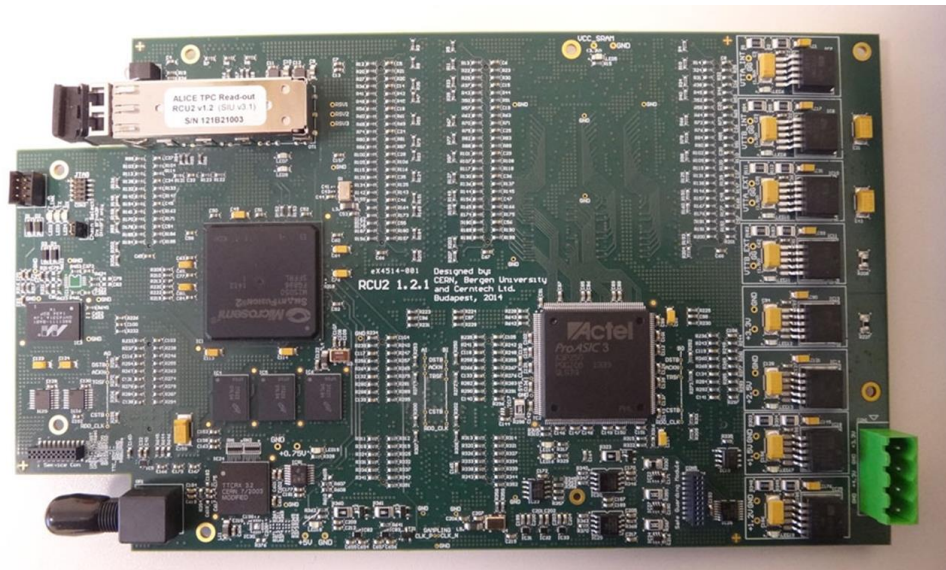
- Ionisieren des Gases durch durchquerende Teilchen
 - Freisetzung von e^-
- Homogenes elektrisches Feld
 - Beschleunigung zu den Endkappen hin
 - Ionisierung weiterer Gasmoleküle
 - Ionenwolke
 - Registrierung durch sog. Pads



http://aliceinfo.cern.ch/Public/en/Chapter2/Chap2_TPC.html

Elektronik der TPC

- 570.000 Pads \rightarrow 570.000 Kanäle
- 128 Kanäle pro Front-End Card (FEC)
- 21-33 FECs pro Readout-Control-Unit (RCU)

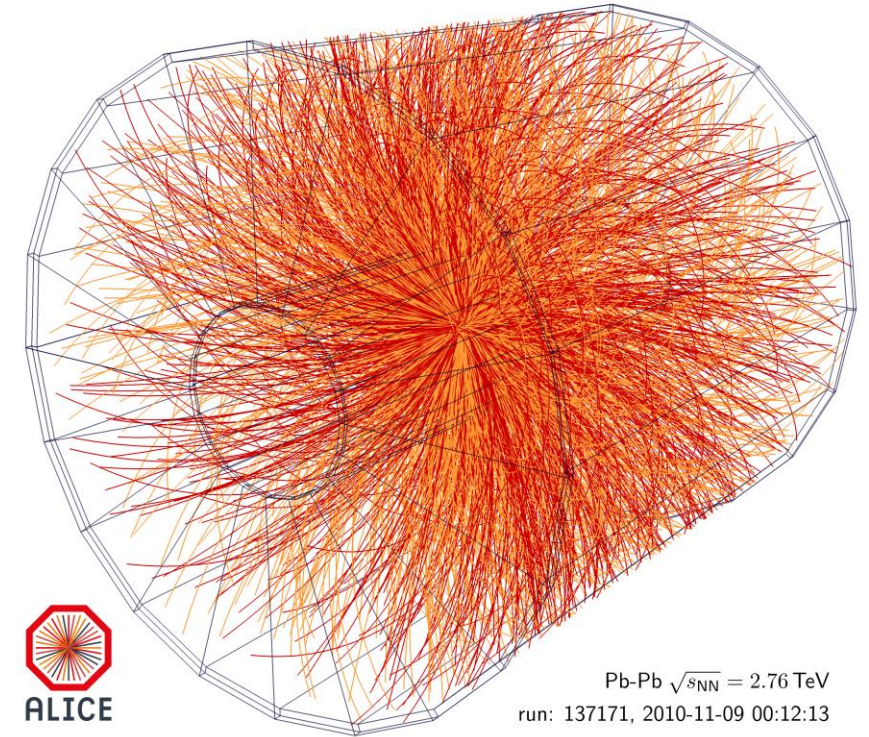


Aufgabe

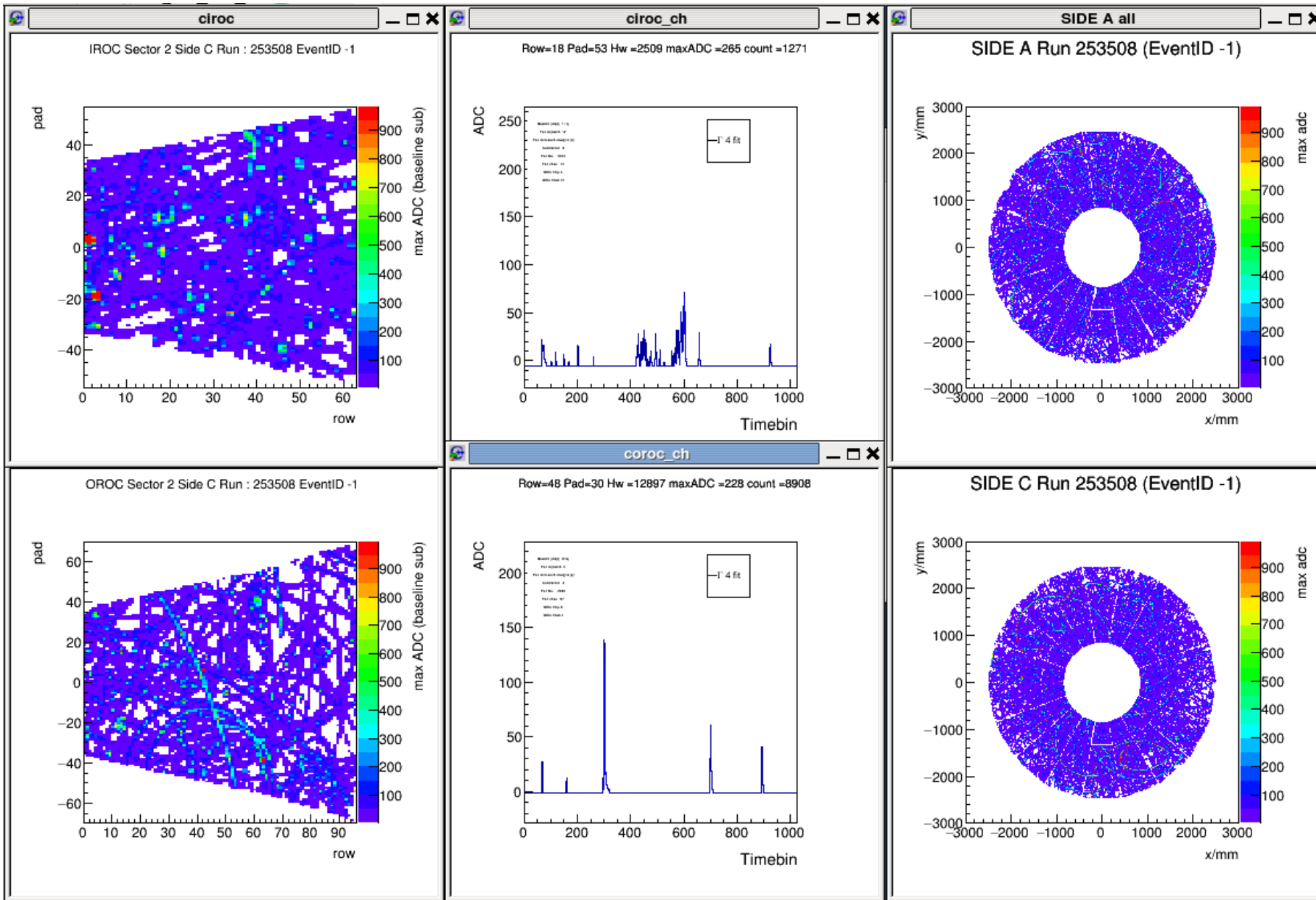
- Simulation der Signale der Teilchen durch Trigger
- Verschiedene Rahmenbedingungen
- Input-Rate schrittweise erhöhen
 - Messung der Output-Rate
 - Ermittlung des Messverhaltens

Wozu das Ganze?

- Bei ALICE: Ionenkollisionen
 - hohe Komplexität
 - hohe Teilchendichte
 - sehr gutes Auflösungsvermögen nötig



<https://cds.cern.ch/record/2032743?ln=de>





TPC_SD LDC status display

LDC name	alone1dc
host	pcphaid001.cern.ch
Number of equipments	1
Number of triggers	26041
Current Trigger rate	0.0
Average Trigger rate	1085.0
Number of sub-events	26041
Sub-event rate	0
Sub-events recorded	26045
Sub-event recorded rate	0
Bytes recorded	1067681320
Byte recorded rate	0 B/s
Nb. evts w/o HLT decision	0

CTP emulator

Sequence: i2a.slm

Examine SLM Load sequence Sequencer

Errors disabled

L1 message format: Complete L1m LHC Gap Veto ON

Automatic START signal selection: Random rate: 7000Hz

Generate SW 'Start signal(s)' # of signals: 1 spacing[m]

of emulation starts: 1 interval [ms]: 1

of repetitive breaks: 0 interval [ms]: 1

Check emulation status Start emulation Break emulation

DATETPC_DAQ::TPC_CONTROL

File View Options Windows Status update

TPC DAQ - Run Control

HI running on pcphaid001 with PID 13340
RC running on pcphaid001 with PID 13161

Disconnected Configuration Connected Run Parameters Ready to start

Start processes

EDM

HLT: mode A

LDC: Local Recording OFF

Data Taking Start Stop Fast Stop Abort

```

tpc@pcphesse17:~
Content of Register ACTFECLIST_B: 0xFF
Resetting board controller
FEC reset
Reset FECERR registers
Reset PAR request registers
Enable access to the ROLM via the RCU Bus
Adding all channels of powered FECs to ROLMs
Enable ROLM and HLM access for readout
Enable control of the ABI via the RCU Bus
Setting ZSTHR register (threshold=0)
Setting FPD to 0x0
Setting data path (BC1CFG) to 0xa
Writing pattern 0x155 to PEDESTAL memories
Give back control of the ABI to fabric
Select TTC L1 as start-of-acquisition
Configure TTC control register
Enable data sorting
Disable skipping of empty channels
Configure full readout
Reset FECERR registers
Reset PAR request registers
Set PAR masks
Arm Sync
rcu0218 /mnt/dcbro/rcu2/bin $ ./config -fall -n10 -e75 -x0
    
```

```

tpc@pcphesse17:~
TTCRX is READY
Using /dev/i2c/002 and /dev/i2c/003
Writing value 0x7f to register 3
L1 Delay is set to 0x2117
L1 Message Latency minimum is set to 0xe0
L1 Message Latency maximum is set to 0x4e20
L2 Latency minimum is set to 0xc80
L2 Latency maximum is set to 0x4e20
Fixed dead time 0x32 (resolution is 10 us)
Number of multi event buffers is set to 4
Status of FSM HALT : 0
dcs0155:/mnt/dcbro/busy $ ./bbinit.sh
TTCRX is READY
Using /dev/i2c/002 and /dev/i2c/003
Writing value 0x7f to register 3
L1 Delay is set to 0x2117
L1 Message Latency minimum is set to 0xe0
L1 Message Latency maximum is set to 0x4e20
L2 Latency minimum is set to 0xc80
L2 Latency maximum is set to 0x4e20
Fixed dead time 0x32 (resolution is 10 us)
Number of multi event buffers is set to 4
Status of FSM HALT : 0
dcs0155:/mnt/dcbro/busy $
    
```

```

tpc@pcphesse17:~
***** Busy Box Monitoring Registers *****
***** FOR BB FW VERSION > 60 (RCU2) *****
Busy Box Fw Version (0x2015) (should be > 60) : 65
Dead Time After L0 (0x2008) : 500 usec
Trigger Receiver CTRL Reg (0x3000) : 0x23
*****
L0 Counter (dec) (0x3014) : 17573
L1 accept Counter (dec) (0x3016) : 48571
L1 reject counter (dec) (0x3018) : 23909
L1 message Counter (dec) (0x301a) : 0
L2 Accept Counter (dec) (0x301c) : 0
L2 Reject Counter (dec) (0x301e) : 48
Number of Decoding ERRORS (0x3024) : 30762
No of seq. or timeout ERRORS (0x3025) : 7188
*****
Event Info 1 (0x303c) : 0x1000
Event Info 2 (0x303d) : 0xa95b
Event Error 1 (0x303e) : 0x22a1
Event Error 2 (0x303f) : 0xd
*****
EventID FIFO count (dec) (0x2001) : 0
Current RequestID (0x200d) : 0x1
Current EventID (0x20021314) : 0x000
Most Recent EventID (0x20051617) : 0x000
*****
Busy Timer (0x201011) : 0xe544ff77
FSM Halt (1=true) (0x200a) : 0
BUSY[14] | MEB Cnt[7:4] | Limit[3:0] (0x2009) : 0x8004
Sparse Rdo Mode=2=MEB (0x2019) : 0x0
Retry Counter (dec) (0x200e) : 65535
*****
Active links
    
```

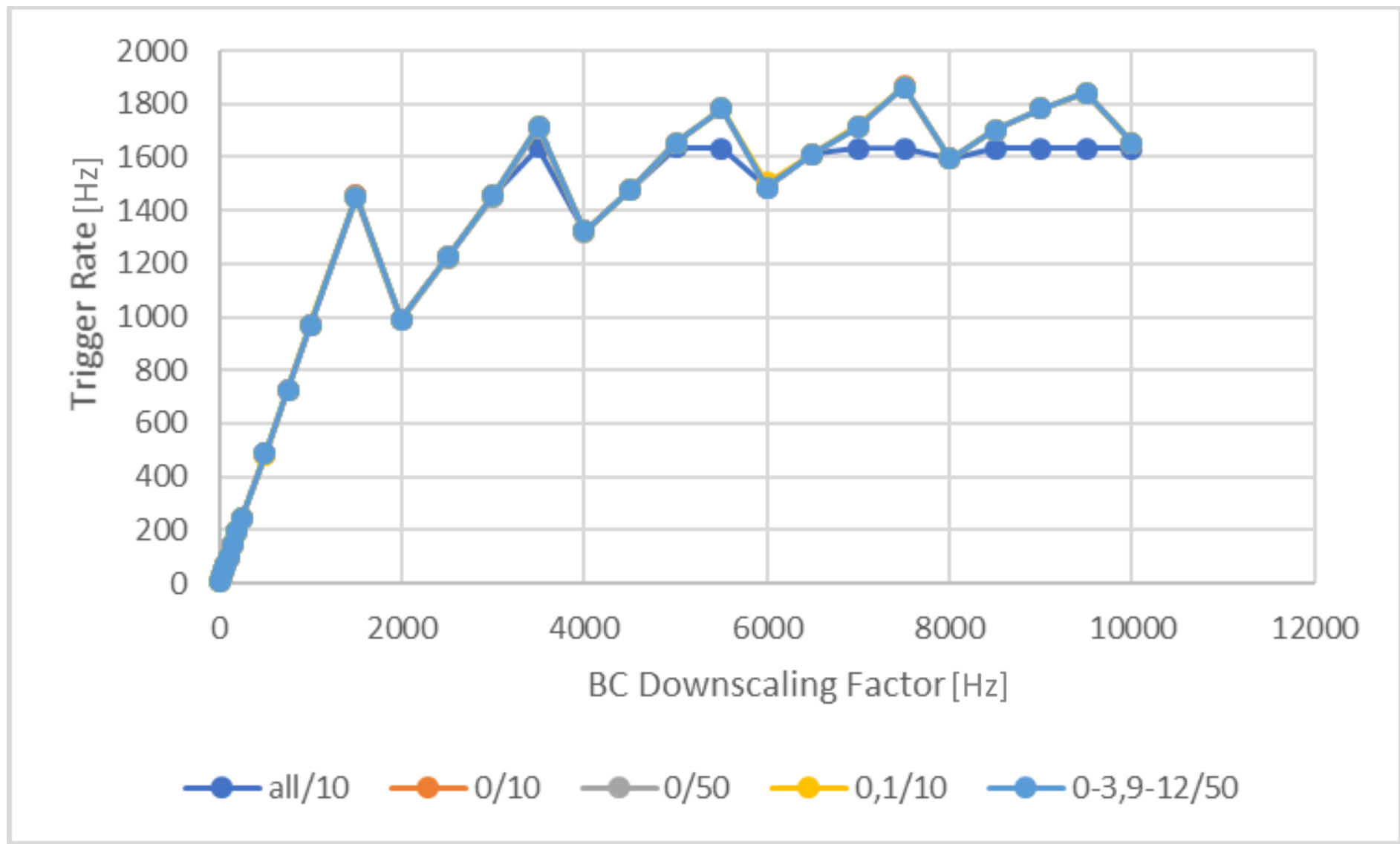
Messungen

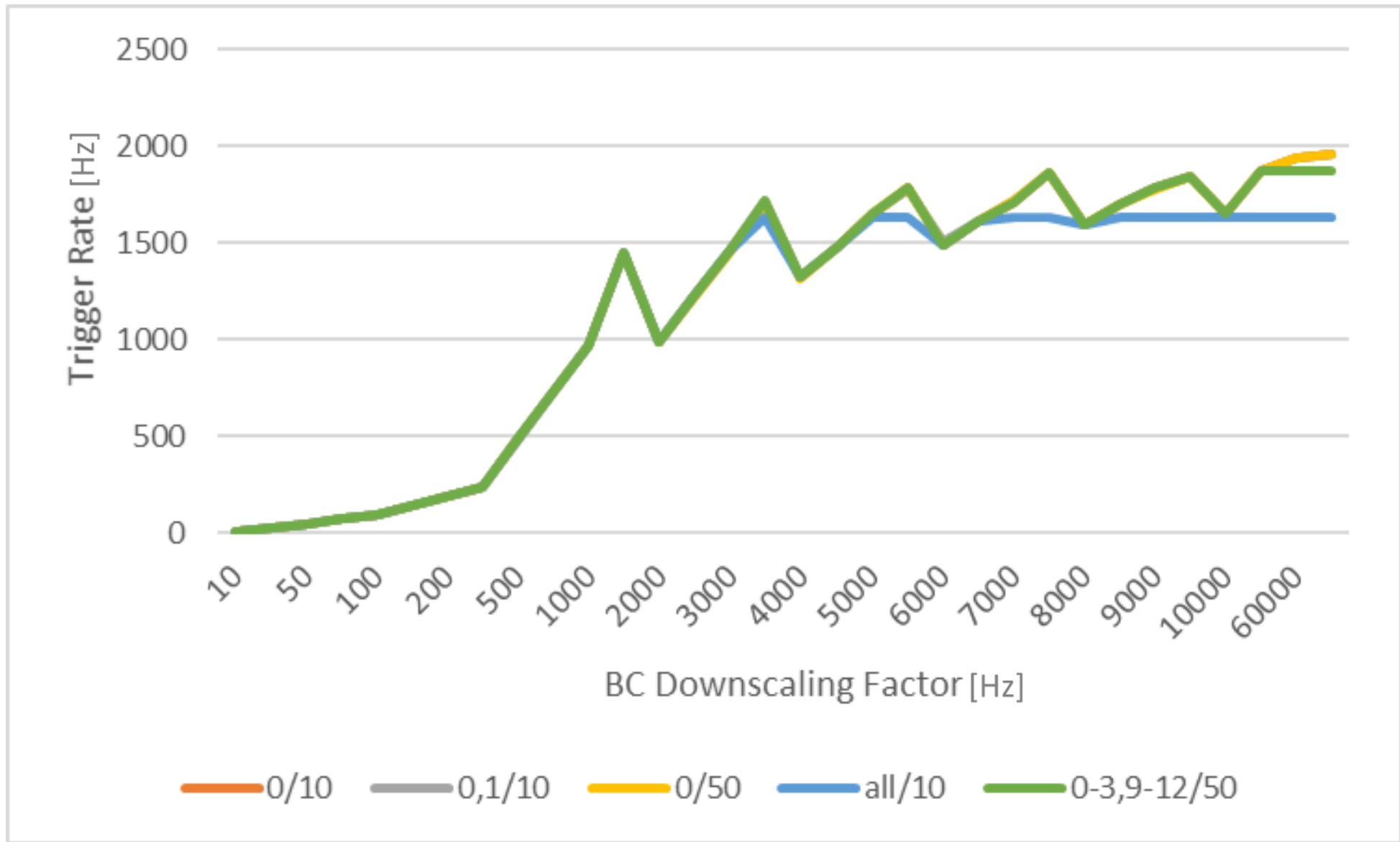
Darstellung der Konfigurationen:

Nummer der eingeschalteten FECs/Anzahl der ausgelesenen Samples

z.B.: 0,1/10

→ FEC Nr. 0 und 1 eingeschaltet, 10 Samples pro Kanal ausgelesen





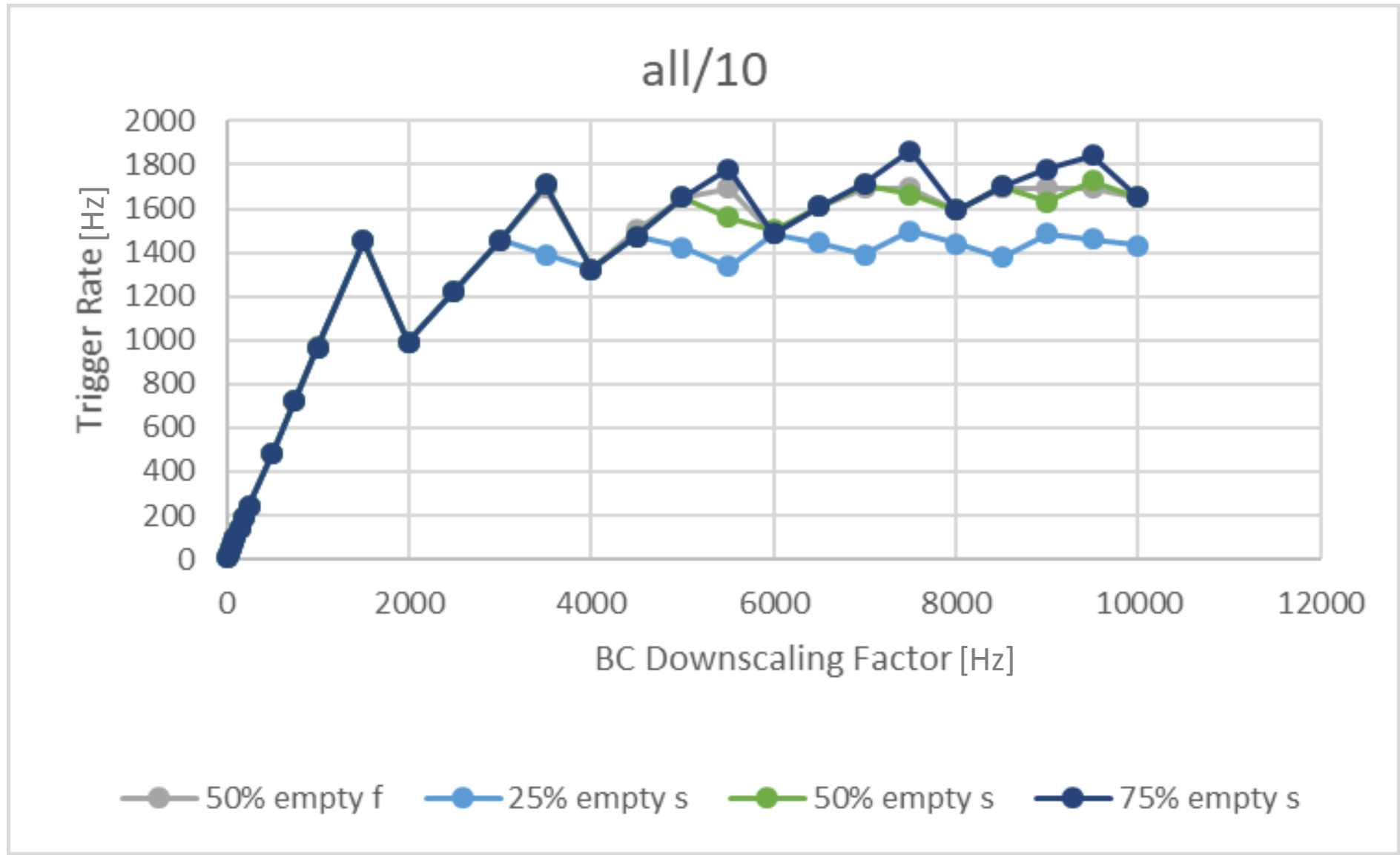
Auslesemodi: Full und Sparse Readout

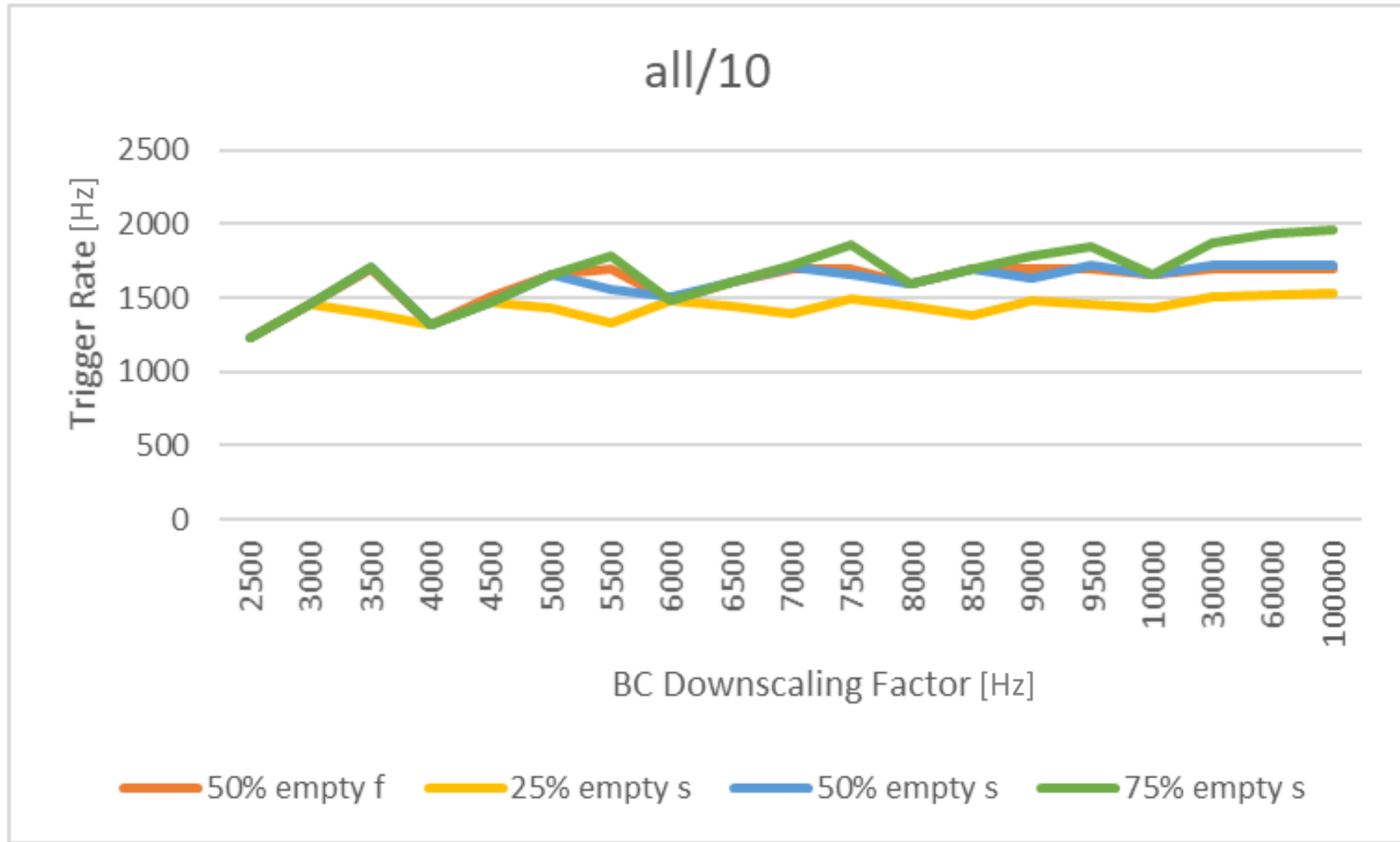
Full Readout:

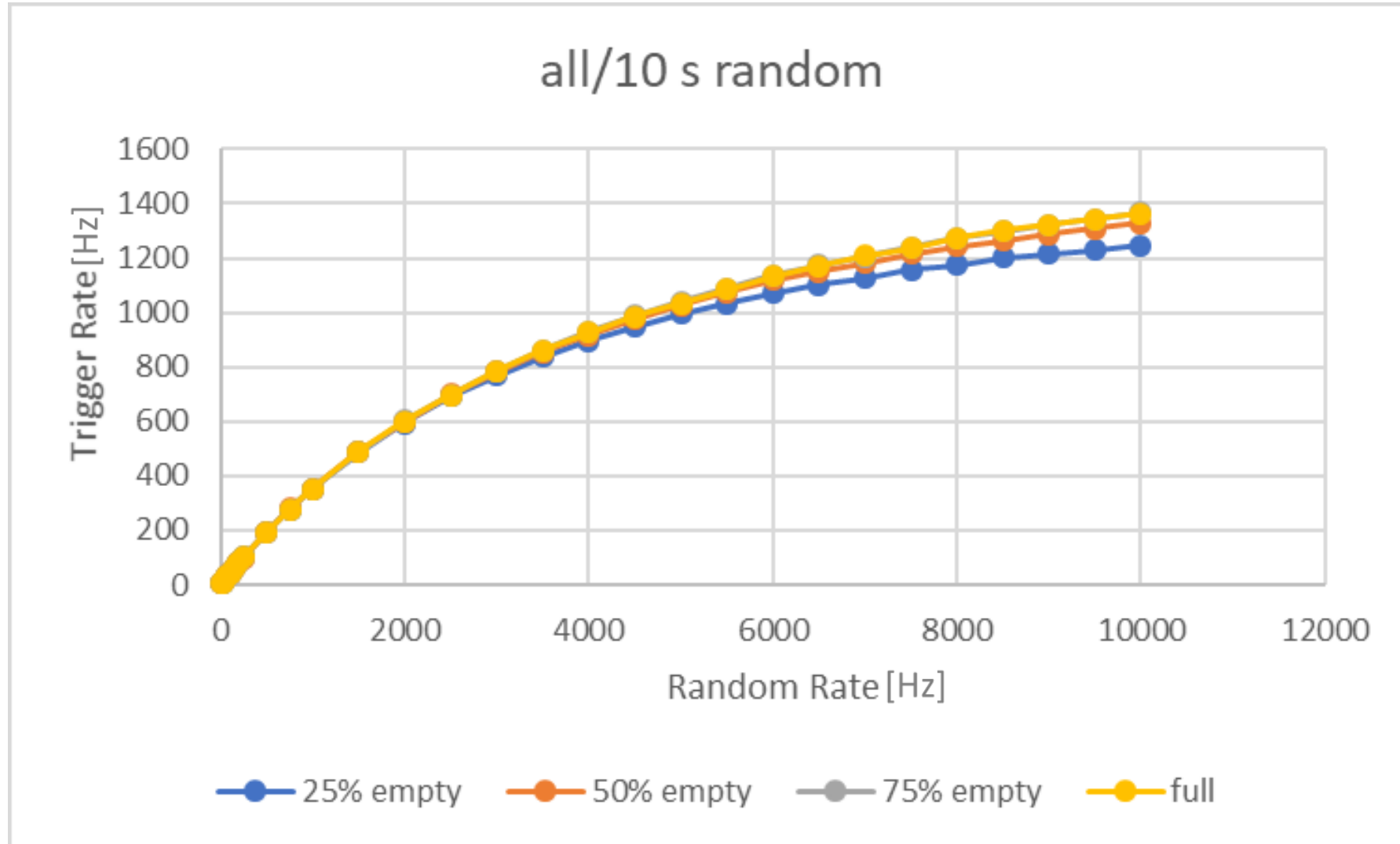
- Alle Kanäle werden ausgelesen
- Leere Kanäle senden nur einen Header

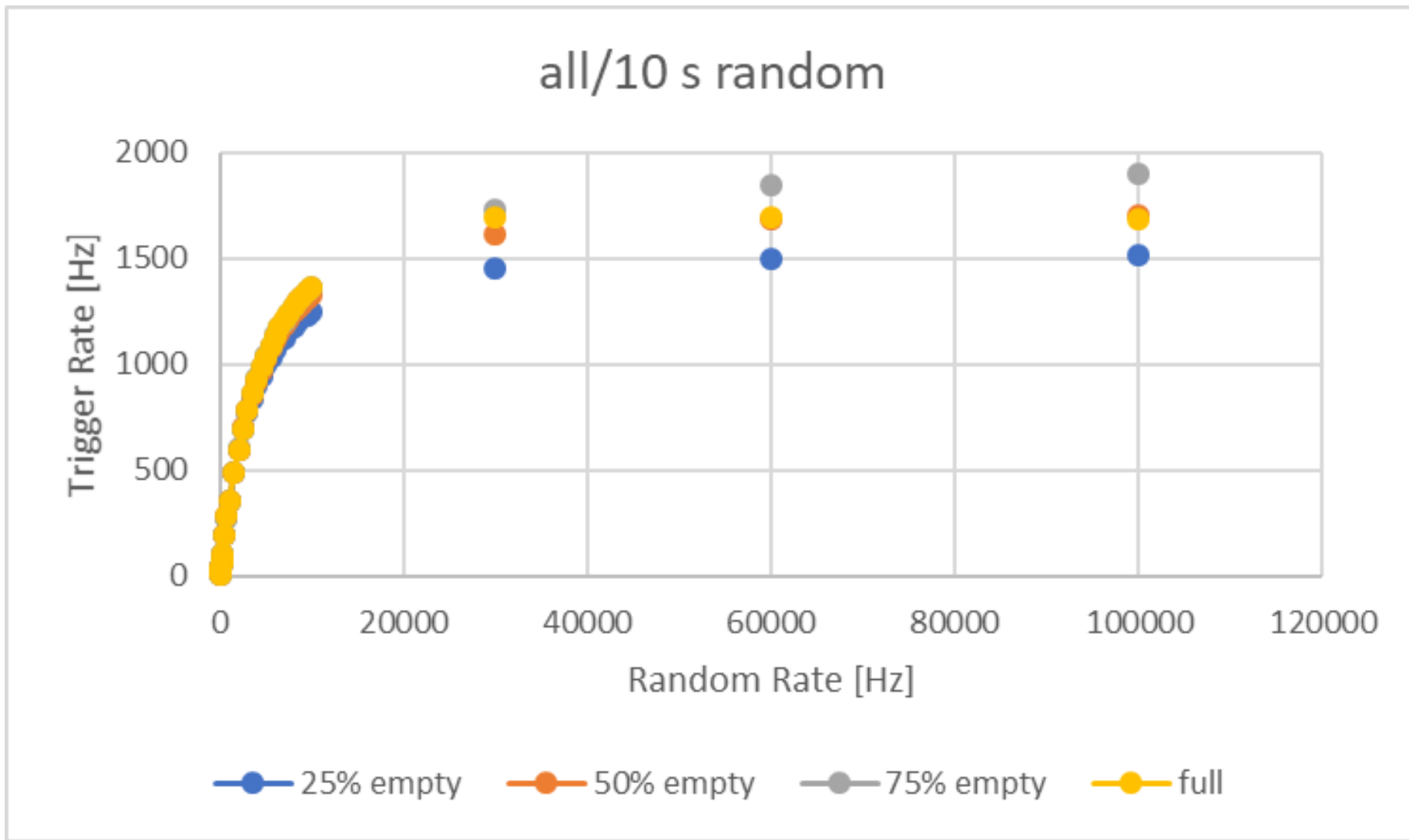
Sparse Readout:

- Ermittlung der Kanäle mit Signalen
- Nur nicht-leere Kanäle werden ausgelesen









Fazit

- Zunehmende FEC-Anzahl
 - Output-Rate sinkt
 - Output-Rate konvergiert schneller
- Random-Rate
 - Kurvenförmigerer Verlauf (\leftrightarrow BC)
- Sparse Readout lohnt sich erst ab hohen Input-Raten bzw. einem Anteil an leeren Kanälen von über 50%