RD53A Test System

USBpix development

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USBpix-based Test System

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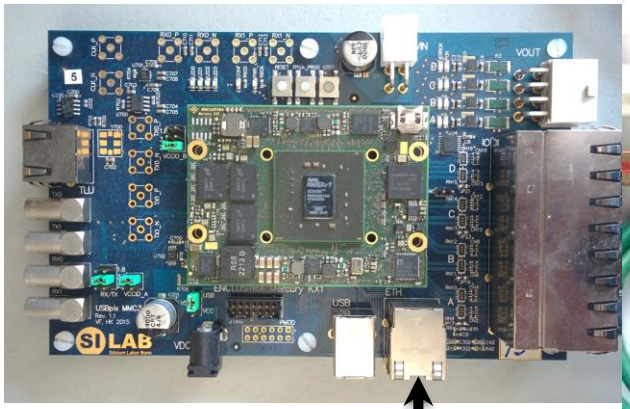
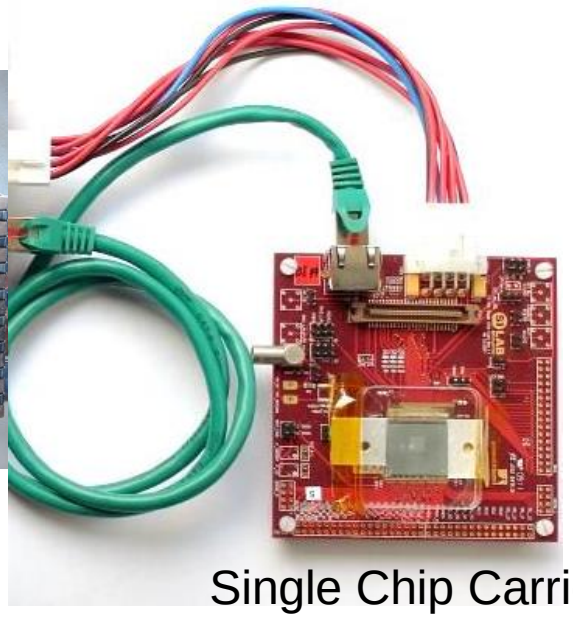
- Current Readout system in Bonn “USBpix 3”
  - Custom design base board with connectors, clock distribution etc.
  - Commercial Kintex 7 FPGA plug-in-board with DDR3 memory etc.
- USBpix 3 will be modified to support high speed serial links.
- Basil framework for hardware access and pyBar DAQ/test software.



MMC3 (“USBpix”)

Ethernet



Single Chip Carrier

Status of SW development

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- FPGA code and HW drivers for CMD encoder and the Aurora receiver work within the digital design simulation environment, now the rest of the FPGA firmware modules is being written.
- Basic idea to deal with high data rate:
  - Fast link only between RD53A chip and FPGA, which handles time-critical tasks.
  - Data reduction by just counting or even discarding certain frames.
  - Filtered data will be transmitted via Gigabit Ethernet through a large FIFO (up to 1 GByte) to avoid bottlenecks in the case of bursts.
- Ethernet speed with SiTCP core tested: ~ 700 Mbit/s
- Large DDR3 memory FIFO: Evaluation of “AXI Virtual FIFO”, which translates between a memory-mapped device (DDR3) and a FIFO-like AXI-Stream interface.

Aurora Protocol

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- We had to upgrade to a new Aurora IP core version, in order to synthesize code for the Kintex 7 FPGA (v7 → v11).
- Signal “RX_channel_up” was never assigned, Aurora core initialization phase never finished.
- Problem: The new Aurora version needs channel bonding (CB) frames, even in the case of single lane mode. Previous version didn’t.
- Temporary solution: Instead of sending CC (clock compensation) frames, now I send CB frames: Changes in “aurora_frame_top.sv”.
- Should we consider sending both frames?