Annealing of TID Effects of SMART sLHC Prototype SSD and Test Structures

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Motivation

Many investigations of irradiated detectors concentrate on the charge collection from the bulk..
But detectors performance depends on parameters influenced by the surface condition:

interstrip capacitance (noise),
interstrip resistance (strip isolation),
breakdown (high voltage operation after bulk damage),

Irradiation with gamma's are probing the detector surface

Treatment of surface very different for p-type and n-type detectors

For p-type, p-spray dose varies widely, influencing the strip isolation and breakdown

Expect effects in Si-SiO_2 interface to saturate at the 100 kRad level
(at this level very little effects in the bulk expected)

Status of the stable surface very interesting for long-term operation

TID effects are known to exhibit large annealing effects, which establishes the stable surface condition.

Structures Investigated

Type	Dimension	Measurements	Frequency
MOS Capacitor	Circular Area =3.14mm^2	C-V	10 kHz
Capacitance TS	Length = 1.15 cm Pitch = 50, 100 um Implant = 15, 25 um Poly width = 10 um Metal = 23, 33 um	Cint-V C-V i-V	~ 1 MHz 10 kHz n.a.
SSD	Length = 4.46 cm Pitch = 50, 100 um Implant = various	Cint-V C-V i-V	~ 1 MHz 10 kHz n.a.

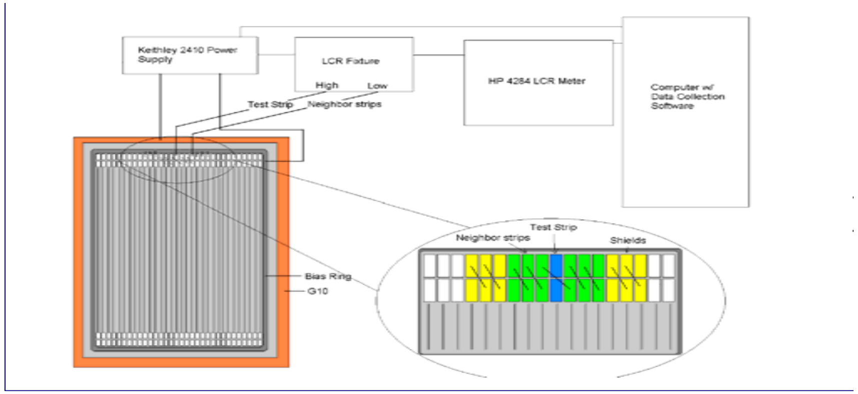
Wafers Investigated

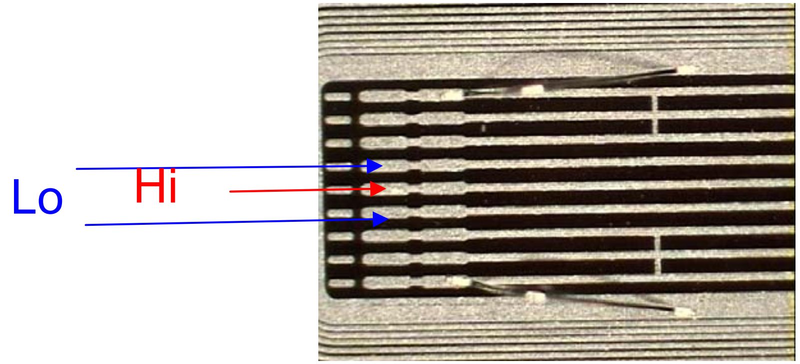
Wafer Type	Wafer #	Thickness [um]	P-spray Dose [cm^{-2}]	SSD / TS / MOS
n FZ	W1254		n.a.	TS, MOS
p FZ	W084	200	$5*10^{12}$	TS, MOS
p FZ	W014	200	$3*10^{12}$	SSD
p FZ	W037	200	$5*10^{12}$	SSD
p MCz	W044	300	$3*10^{12}$, no passivation	TS, MOS
p MCz	W253	300	$5*10^{12}$, no passivation	TS, MOS
p MCz	W066	300	$3*10^{12}$, no passivation	SSD
p MCz	W182	300	$5*10^{12}$, no passivation	SSD

SSD Investigated

SSD	Substrate	P-spray Dose **[cm^{-2}].**	Pitch (µm)	# strips	Implant Width (µm)	Poly Width (µm)	Metal Width (µm)
14-5	FZ 200	$3*10^{12}$	50	64	15	10	27
14-8	FZ 200	$3*10^{12}$	100	32	35	30	43
37-5	FZ 200	$5*10^{12}$	50	64	15	10	27
37-8	FZ 200	$5*10^{12}$	100	32	35	30	43
66-8	MCz	$3*10^{12}$	100	32	35	30	43
182-5	MCz	$5*10^{12}$	50	64	15	10	27
182-8	MCz	$5*10^{12}$	100	32	35	30	43

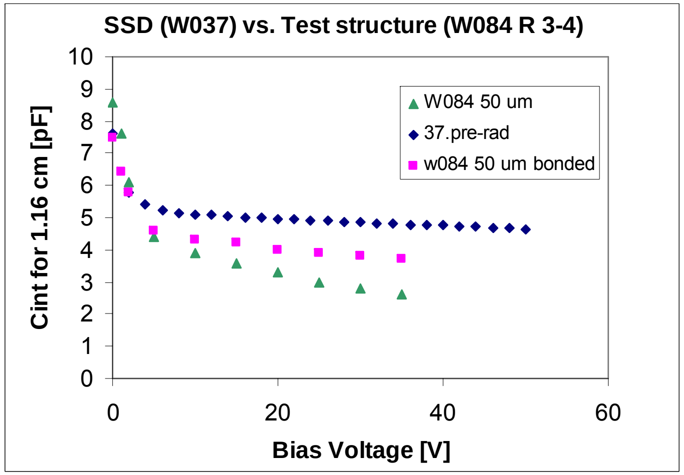
Device Preparation





Mini-SSD
one strip vs. 3 next neighbor pairs
3 following neighbor pairs
bonded to bias (shield).

TS:
one strip vs. next neighbor pair
un-bonded and unbiased
except 3 following neighbor pairs
bonded to bias (shield).



T.S. Pre-rad:
Large difference shield bonded and un-bonded
T.S. Post-rad:
No difference shield bonded and un-bonded

Ratio between mini-SSD and T.S. =1.2
(3 pairs vs. 1 pair)

Irradiation and Annealing

Gamma irradiation in the UCSC ^{60}Co source 3.15 kRad/hr

Irradiate in steps of one day (~70 kRad) and re-measure,
with a few days to weeks in-between steps

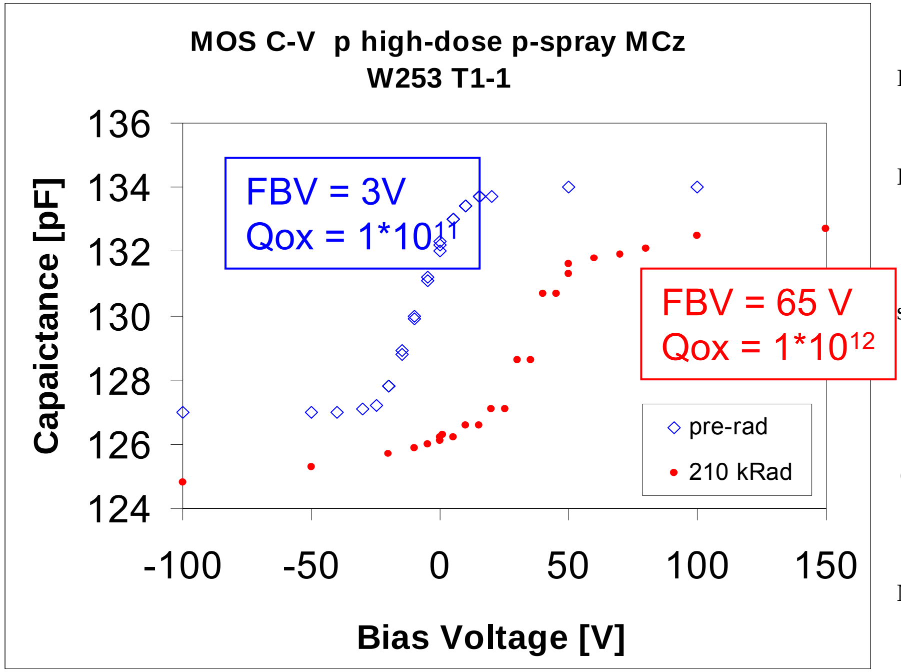
After TID of ~ 500 - 700 kRad, start 3 annealing steps:

1 week room temperature
1 week accelerated anneal at 60°C
1 week accelerated anneal at 60°C
Re-measure after every step

2nd week of 60°C does not change the values: stable state is reached.

Saturation and Annealing behavior consistent between structures and wafers
Saturation and Annealing behavior very different for different parameters

MOS Cap →
Doping Density Nd, Flatband Voltage FBV, Oxide Charge Qox



In accumulation: $C_{\max} = C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$

In depletion: $\frac{1}{C_{depl}} = \frac{1}{C_{ox}} + \frac{1}{C_{sc}}$ where $C_{sc} = \frac{\varepsilon_{Si}}{w_d}$

so that: $C_{sc-\min} = \frac{\varepsilon_{Si}}{w_{d-\max}} = \frac{\varepsilon_{Si}}{\sqrt{\frac{2\cdot\varepsilon_{Si}\cdot 2\varphi_F}{q\cdot N_A}}}$ where $2\varphi_F = 2\cdot\frac{kT}{q}\ln\left(\frac{N_A}{n_i}\right)$

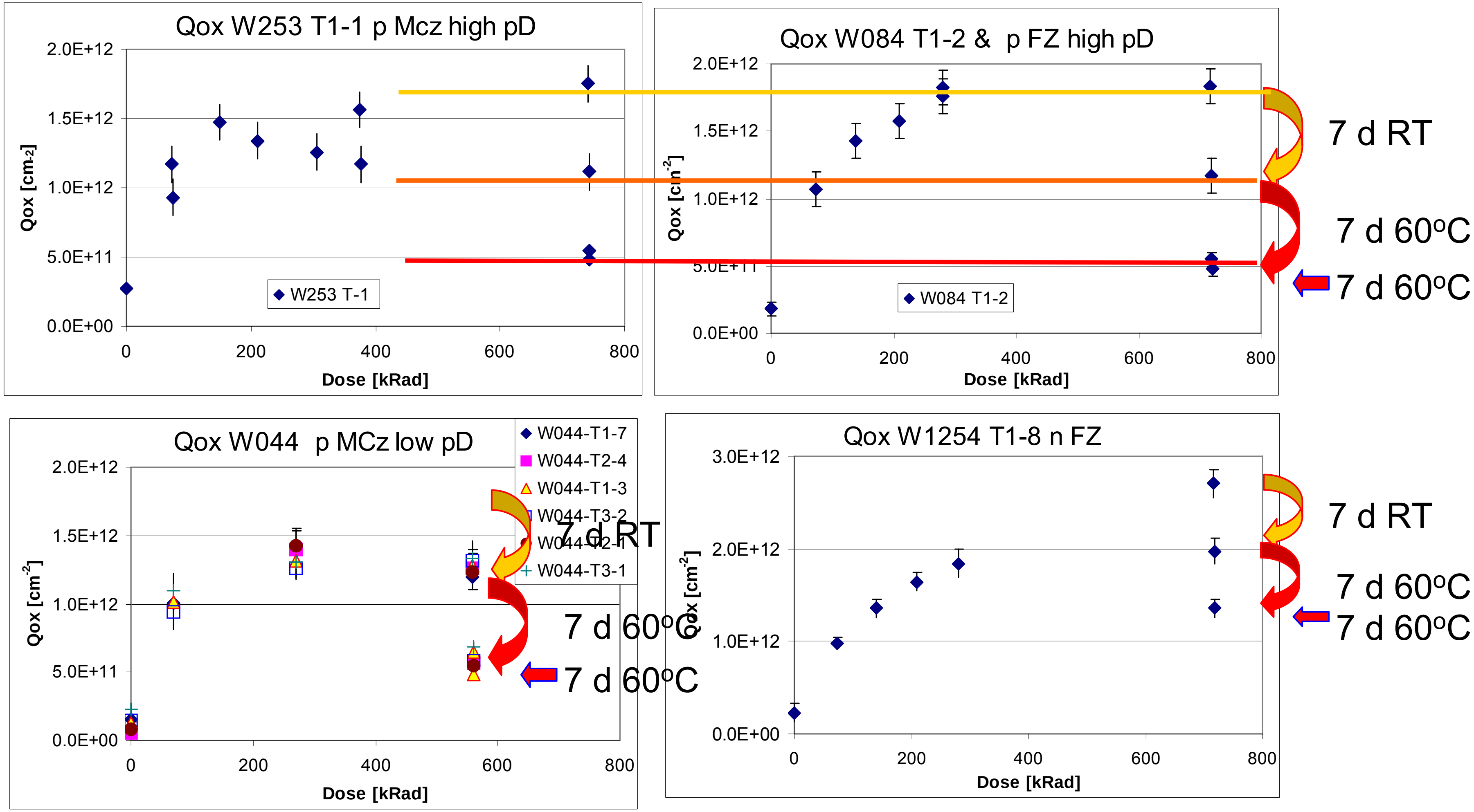
$$C_{sc-FB} = \frac{\varepsilon_{Si}}{L_{Debye}} = \frac{\varepsilon_{Si}}{\sqrt{\frac{\varepsilon_{Si}\cdot kT}{q^2\cdot N_A}}}$$

$$V_{FB} = \phi_{MS} - \frac{Q_{ox}}{C_{ox}}$$

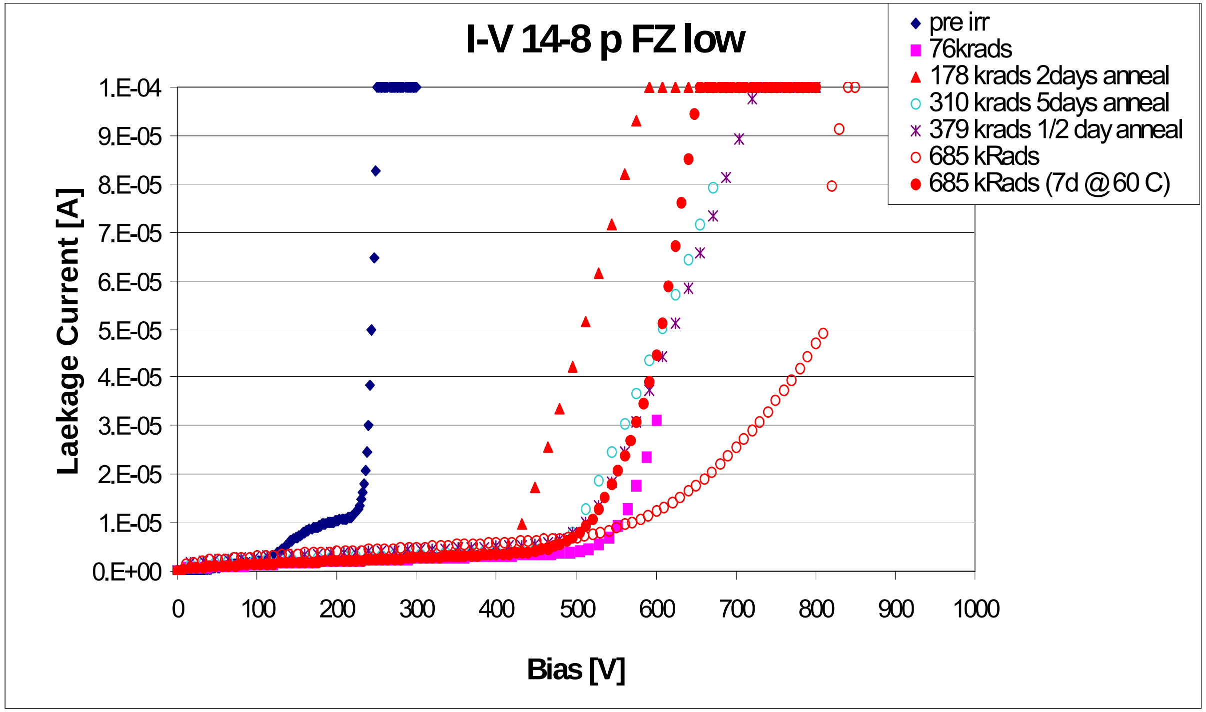
NOTE THAT ALL CAPACITANCES in Formulae are given per UNIT AREA:

Oxide Charge vs. Dose and Anneal Steps:

Saturation before 150 kRad (p-only), Annealing to 1/3 of saturation value



Breakdown Voltage



Large TID effect
on breakdown voltage

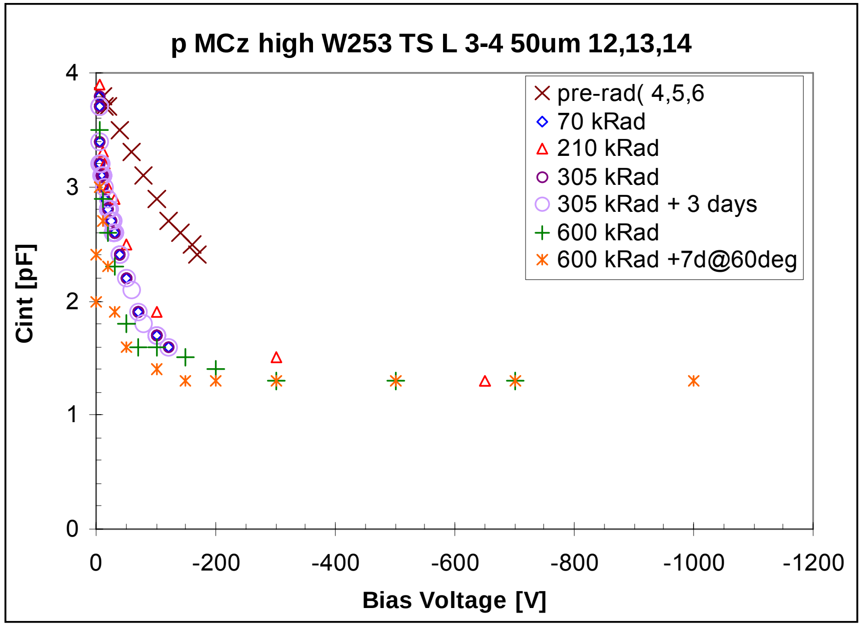
considerable annealing

Table IV Breakdown Voltage

Device	Breakdown Voltage [V]				
	pre-rad	75 kRad	300 kRad	~650 kRad	~650 kRad +7d @60 °C
66-8 p MCz low	250	550	900		
182-8 p MCz high	70	>200	350	>1000	500
14-8 p FZ low	240	600	600	700	600
37-8 p FZ high	70	200	300		

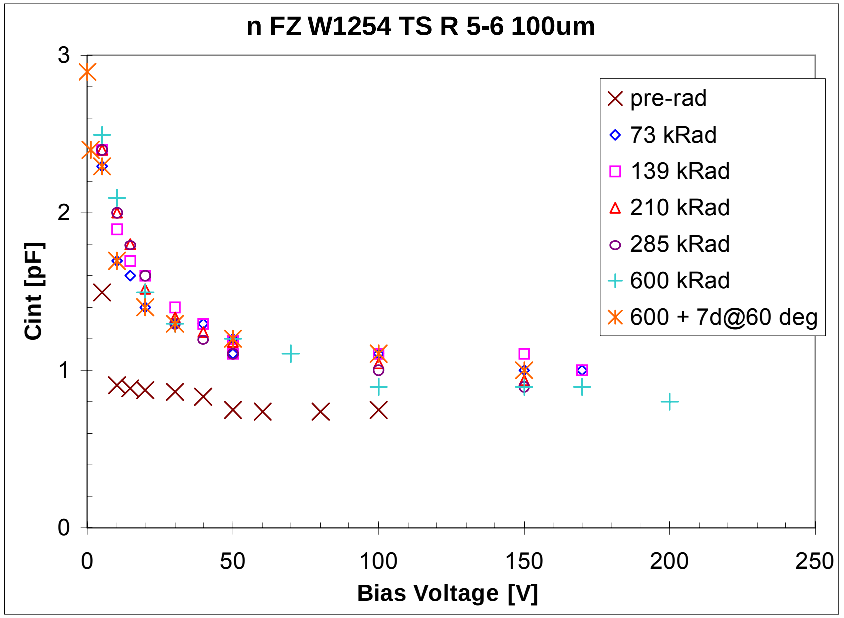
?Annealing of
breakdown voltage
leads to value
independent
of wafer type and p-spray?

Cint vs. Dose and Annealing for T.S.



Large TID effect
on bias voltage dependence of
interstrip capacitance of all p-type TS

Saturation at 70 kRad
No or very little annealing

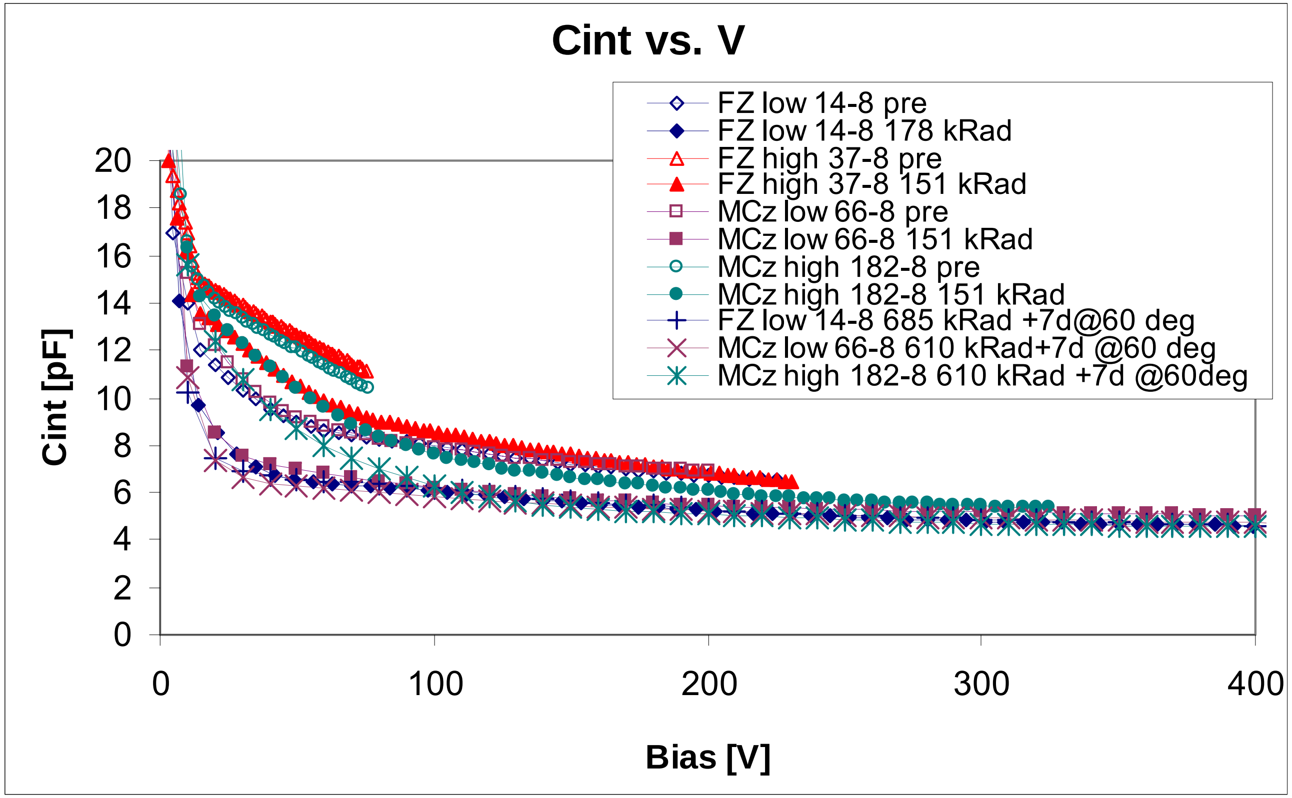


In n-type, large TID effect
on bias voltage dependence of
interstrip capacitance

Saturation at 70 kRad
No or very little annealing

Cint pre-rad after saturation and anneal

(4.45 cm mini-SSD, 100 µm pitch)



C_{int} decreases rapidly with TID for p-type SSD high p-spray dose, slower decrease up to 600 kRad Wafers 14 and 37 are FZ, wafers 66 and 182 MCz. Little difference between different wafers, large dependence on the p-spray.

Geometrical value is reached at moderate voltage after TID irradiation.

The amount of annealing is limited.

Conclusions

The performance of p-type SSD with p-spray isolation
can be improved with gamma irradiation of modest dose.
(We are now pre-irradiating the high p-spray dose SSD to be irradiated with neutrons at Louvain.).

	Saturation Dose [kRad]	Value reached	Effect of Annealing [%]	
Qox	150	$0.5\ 10^{12}$	70%	
Cint	75 (500)	1.2 pF/cm	<10%	
Breakdown Voltage	300 ?	550	20%	

MCz and FZ behave similar TID behavior
Large dependence on p-spray dose.
Saturation of effects, but at different dose for different parameters
Large annealing in Qox and breakdown voltage, but not in Cint
→ different types of TID surface damage ?