Upgrade of the silicon part

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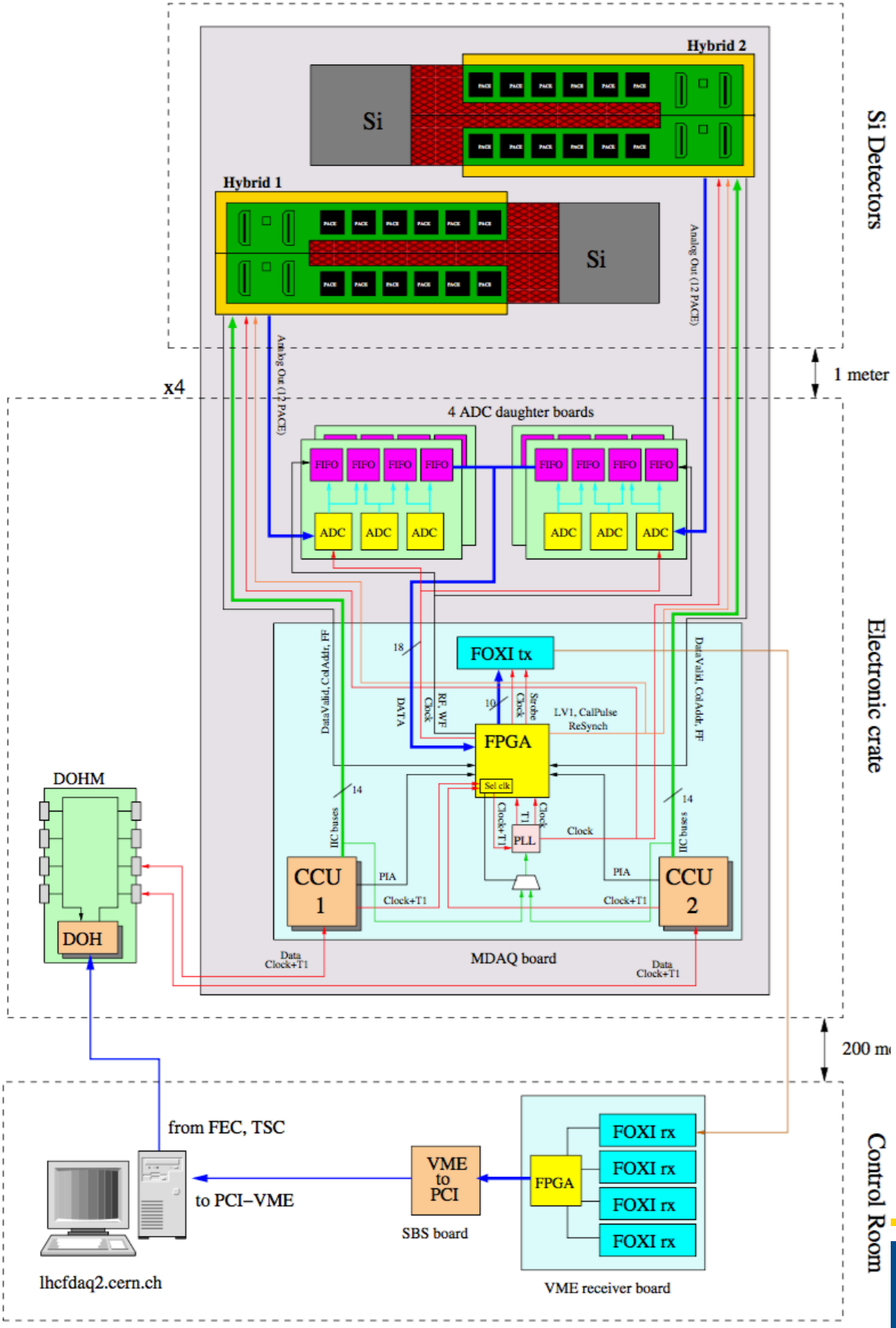
Why silicon upgrade

- We have to define the main reason for silicon upgrade
- Proton-Light Ion Run?
- Other 'parasitic' run that could happen in next few years?
  - P-Xe in 2017
- This presentation will not focus on a possibile far future new experiment, but on a 'simple' upgrade of the silicon part of the existing LHCf detector

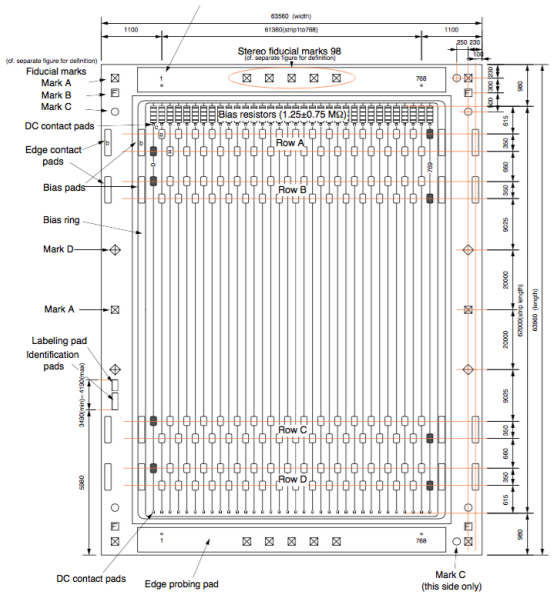
The main parts of LHCf silicon subdetector

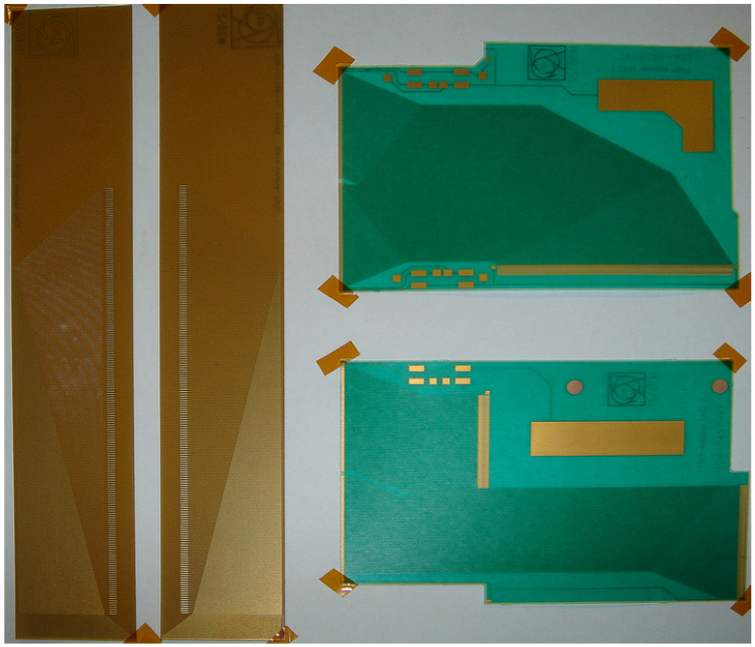
- Silicon detectors
- Front end hybrids
  - Pace3 chips
- Power distribution board
- MDAQ boards
- Control ring to control PACE3
- Optical link for data and VME receiver


Si Detectors
Hybrid 2
Si
Hybrid 1
Si
Analog Out (12 PACE)
Analog Out (12 PACE)
x4
1 meter
4 ADC daughter boards
FIFO
ADC
Electronic crate
FOXI tx
DataValid, ColAddr, FF
18
DATA
RF, WF
Clock
19
Strobe
Clock
LV1, CalPulse
ReSynch
FPGA
Sel clk
14
IIC buses
Clock+T1
T1
Clock
PLL
Clock
PIA
CCU 1
CCU 2
DOHM
DOH
Data
Clock+T1
MDAQ board
200 m
Control Room
from FEC, TSC
to PCI–VME
lhcfdaq2.cern.ch
VME to PCI
SBS board
FPGA
FOXI rx
VME receiver board

Silicon detectors and kapton fanouts

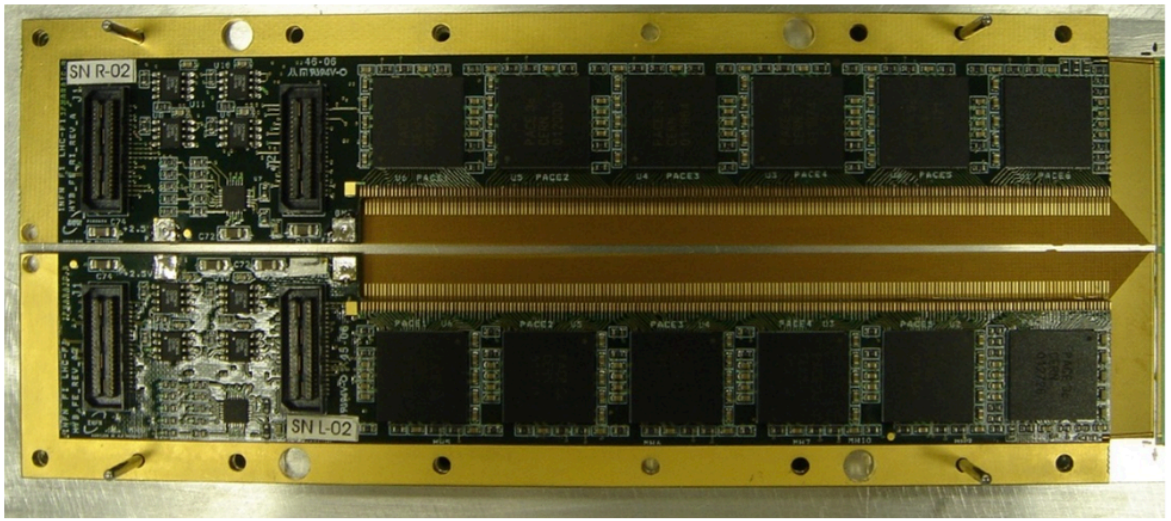
- This part has already been modified before the 13 TeV p-p run to increase dynamic range, new sensors with a particular bonding pattern → Ok
- I think is not possible and not necessary to upgrade it
  - Not necessary because no physics limitations due to sensors
  - Not possible because of money





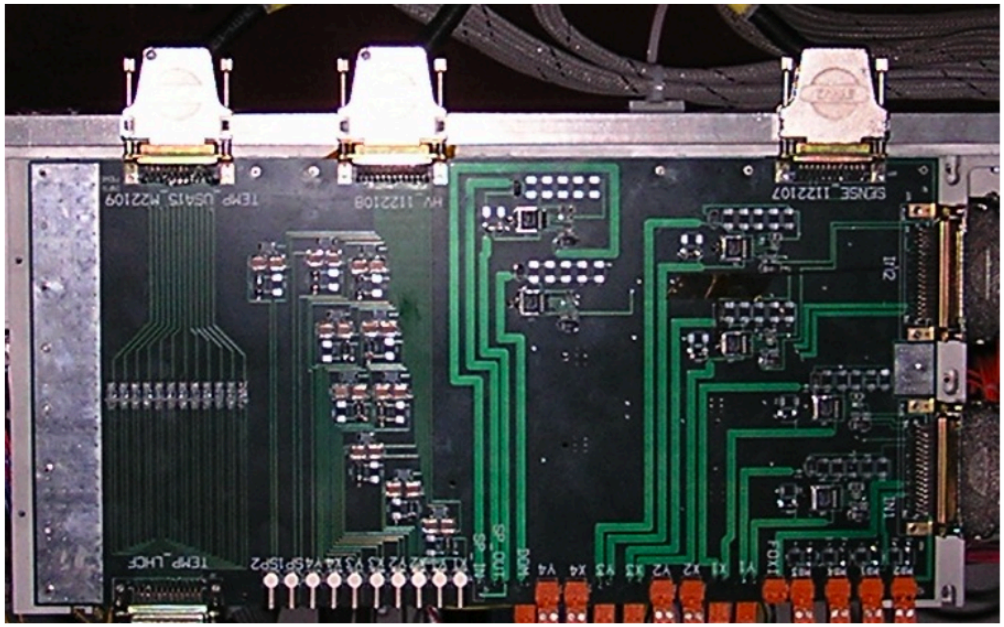
Front end hybrids and Pace3 chips

- The hybrids have been completely rebuilt few years ago for:
  - Solve few minor problems existing in the old version
    - Reset signal was missing
    - Few chips were broken
    - Assembly of new kapton fanout in the Hybrid zone
- I think it is not possible to upgrade this part because no more PACE3 chips are available from CMS
  - It is completely not realistic to think to use different chips
  - The dynamic range is adequate

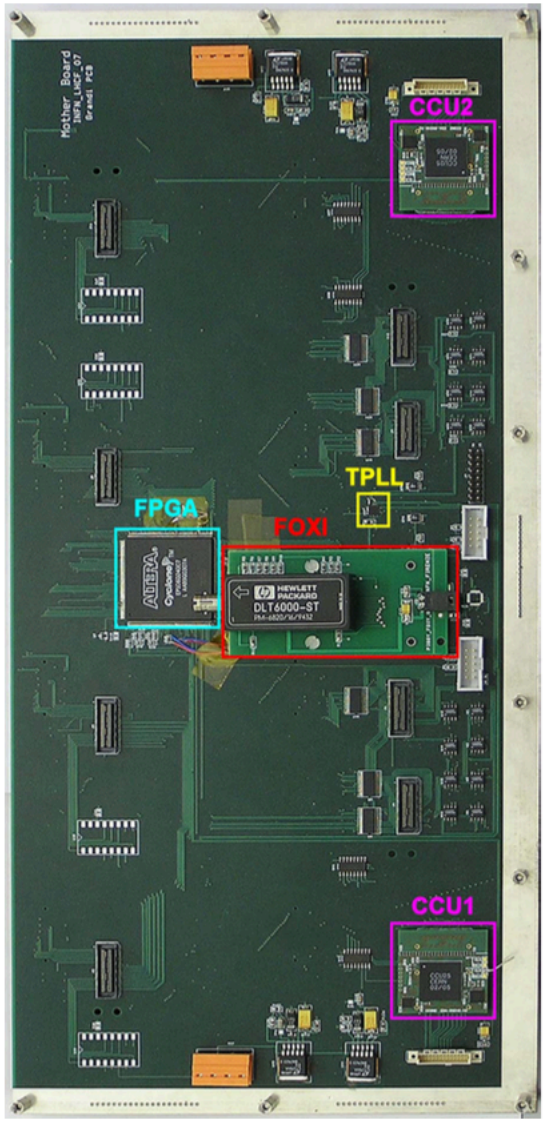


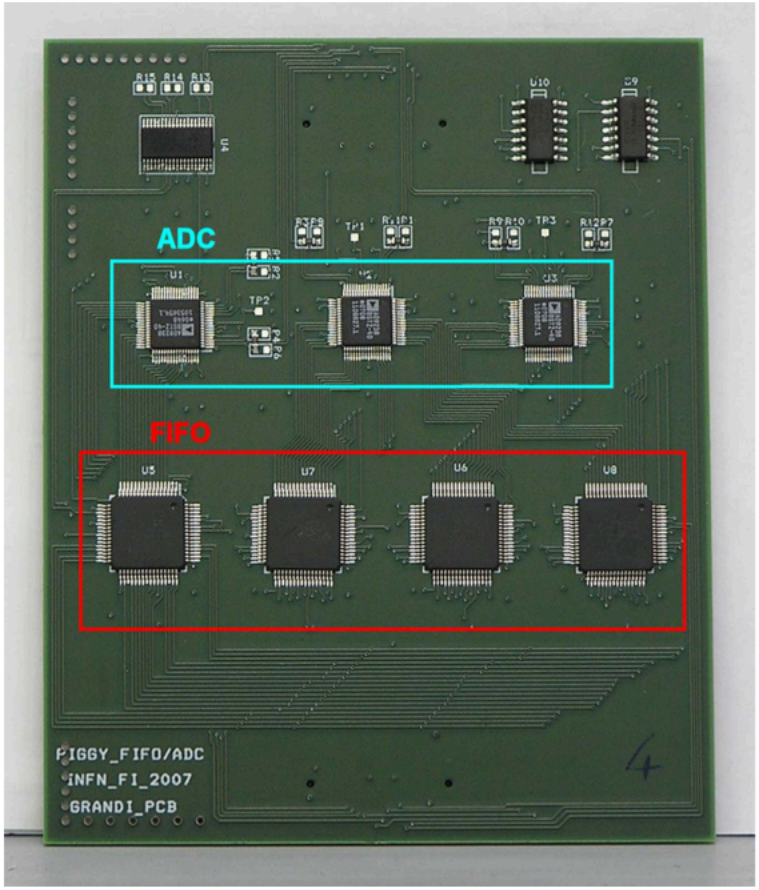
Power distribution board

- The Power Distribution Board is used to handle the voltage generator for all the silicon part
  - Linear regulators
  - Sense wires connection for Agilent Power Supply
- A problem on connectors appeared during the first p-Pb run
- Connectors have been changed
- No major issues



MDAQ Boards


CCU2
TPLL
FPGA
FOXI
HEWLETT PACKARD
DLT6000-ST
CCU1


ADC
FIFO
PIGGY_FIFO/ADC
INFN_FI_2007
GRANDI_PCB

MDAQ Boards

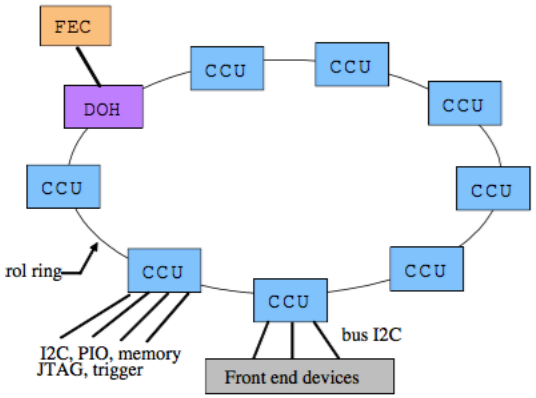
- The MDAQ Boards are used to:
  - Generate the control signals for the Pace3 chips by using custom chips developed by CERN
    - CCU
    - Clock re-generator
  - ADC conversion
  - DAQ sequence handling with Finite State Machine on Altera FPGA
  - Temporary data storage on FIFO
  - Interface the data with the optical link transmission
  - Interface with the ring to control the Pace3

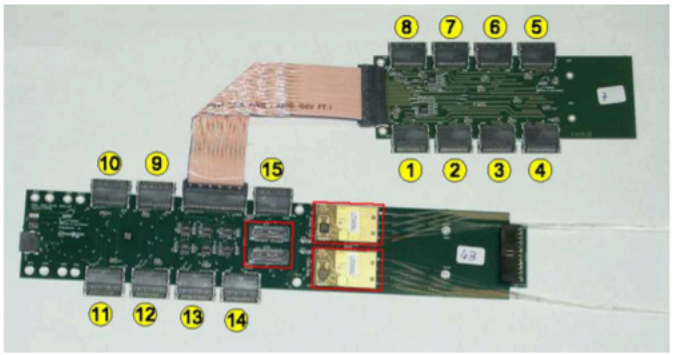
MDAQ Boards

- Some critical issues related to MDAQ are present:
  - Boards are very large, and difficult to handle
    - Very large electronic box is necessary
  - Interface with the FOXI transmitter is very weak for the mechanical point of view
- Can we do new MDAQ boards?
- In principle it is possible, even if:
  - No anymore custom chips to regenerate the clock are available from Cern
  - No anymore ADC chips are available form CERN
- We can study how to implement new MDAQ boards with commercial chips

Control ring for Pace3

- A dedicated control ring is necessary to:
  - Send commands to Pace3 chips
  - Distribute clock, reset and trigger
  - Handle the redundancy (never used up to now!)
- The system is working well and can be used it again
- The only real problem is the PC used to control the ring
  - FEC and TSC boards
  - Driver not working on recent Linux distribution
  - A very old and not safe PC should be used





Optical link for data and VME Receiver

- Most critical issue
- The Taxi chips are very obsolete
- Some optical fibers in the tunnel are damaged and spares have been used
- The VME receiver board is always creating problems
  - Works only in some slots
  - CRC errors are often present in variable fraction
- The Data Transmission system should be completely redesigned
- This is the most important and necessary item for Silicon Upgrade

Optical link for data and VME Receiver

- For the moment we do not have a real proposal
- Should we use optical or copper link?
  - Fast Gbit ethernet protocol?
- How we install new cables or new fibers in the tunnel?
- Which receiver board should we use?
- The system on the Front End side should be interfaced with the MDAQ boards
  - New or old MDAQ boards?