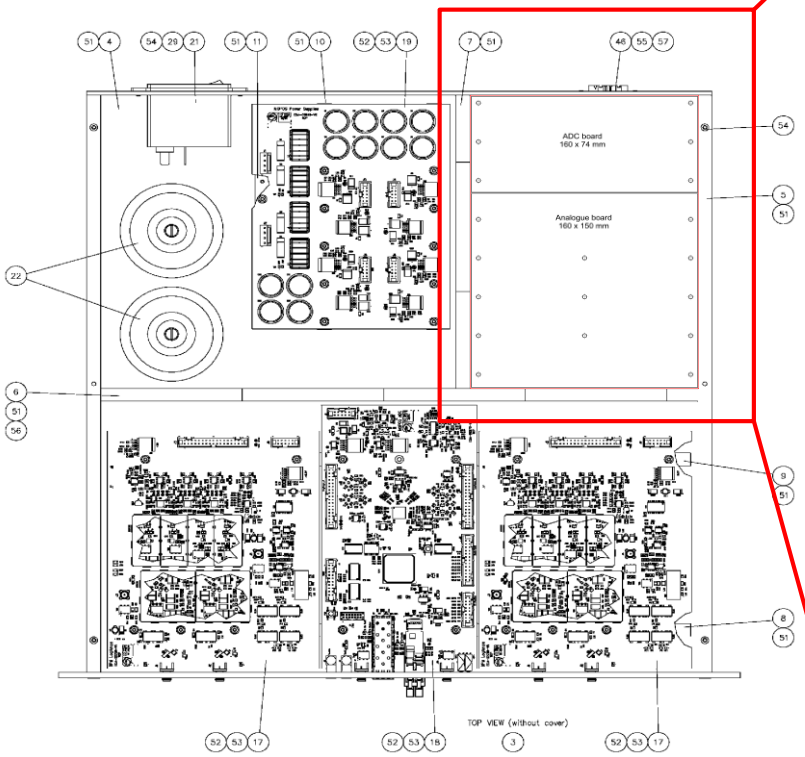
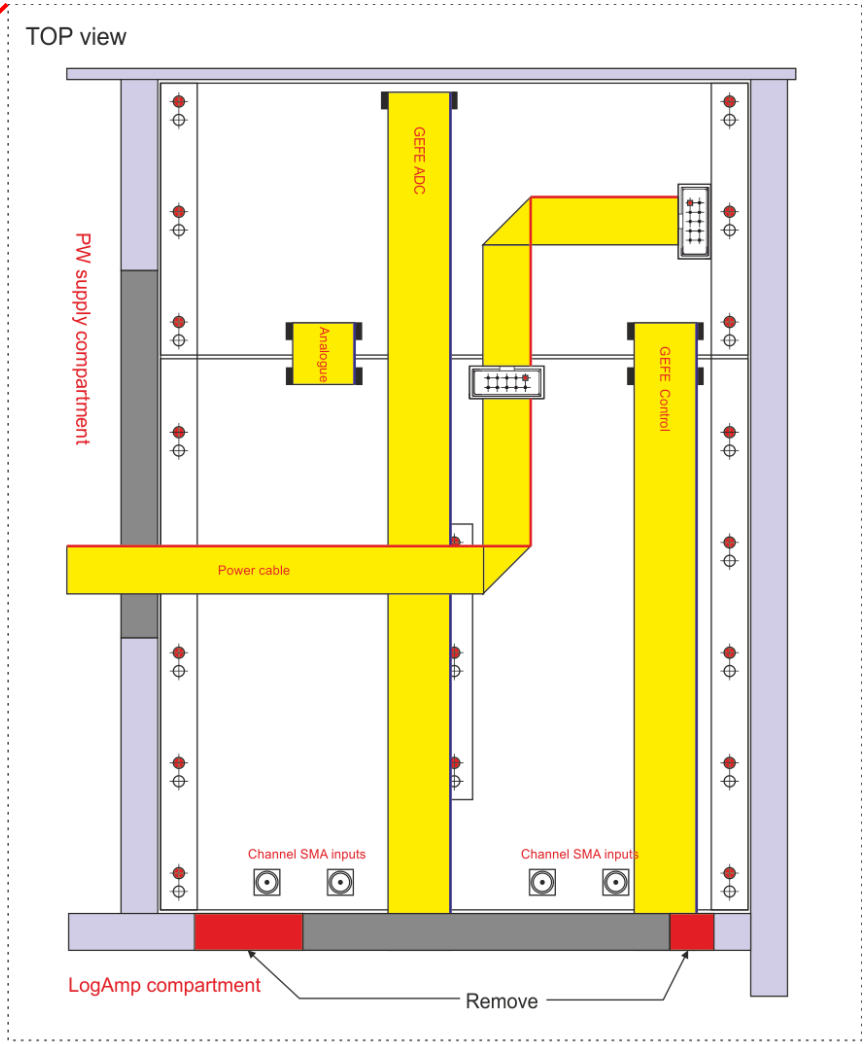
DOR(OS) integration status and plans

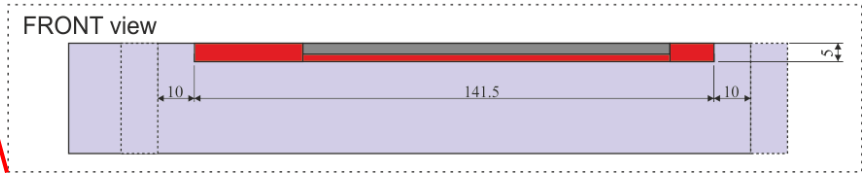
Jakub Olexa, Marek Gasior

- Mechanics
- Components radiation testing
- Schematics & PCB
- Firmware

DOR(OS) 4 ALPS - Mechanics







DOR(OS) 4 ALPS - components radiation testing

Status:

- 15 components tested (tests issued in 2016)
- Available results for 5 DUTs:
  - **Critical components** for the design (a lot of R&D time invested and no good potential replacements)
    - RF switches MASW-007587 & MASWSS0144 – **OK** up to 750 Gy (EDMS 1735615 v.1)
    - RF amplifier THS3201 – **OK** up to 750 Gy (EDMS 1738241 v.1)
      Not recommended for new designs since 2016 !!!
      - We propose to make a stock ASAP before the prices go up.
        Current price 4 $/pc vs 2.5 in 2015.
      - 5 pcs / channel = 20 pcs / board (2 planes)
      - For 300 MOPOS Fes 6k pcs required
      - We propose to buy 10k, that is some 40 kCHF required
      - Can be used also in the LHC DOROS
  - Less critical / replaceable
    - Prog. opamp PGA103 – **OK** up to 750 Gy (EDMS 1729244 v.1)
    - Precision opamp AD8676 – Recoverable **SEL** @ 550 Gy (EDMS 1729267 v.1)

Plans:

- Radiation tests scheduled for 2017:
  - More components on analogue front-end and ADCs
    - The components list completed and issued for tests
  - Whole LHC DOROS FE to be tested in CHARM
    - Awaiting the test time slot

DOR(OS) 4 ALPS - schematics & PCBs

Analogue board

Status:

- Analogue board development in progress:
  - Documents sent to the PCB workshop
  - The PCB will be designed in Altium – requesting new components for the library

Plans:

- Production of 5 analogue boards expected for end of March

Rad-hard ADC board

Status:

- Waiting for the results of the ADC radiation tests

Plans:

- Develop the final card based on the ADC radiation results

- The new analogue board can be evaluated using the existing LHC ADC boards
  - Based on the 8-channel $\Delta/\sum$ ADS1278. Its 3 versions are on the radiation testing list
  - Requires minor modifications on the PLL part to adapt for a new sampling frequency, otherwise can be used as is

DOR(OS) 4 ALPS - firmware

Status:

- Preparation of the development platform
  - Latest version of the VFC card installed in cfv-866-bidev8 (slot 15)
  - Front-end chassis with Pw supply, LogAmps and GEFE v2
- Ready to start testing the setup with the latest MOPOS firmware

Plans:

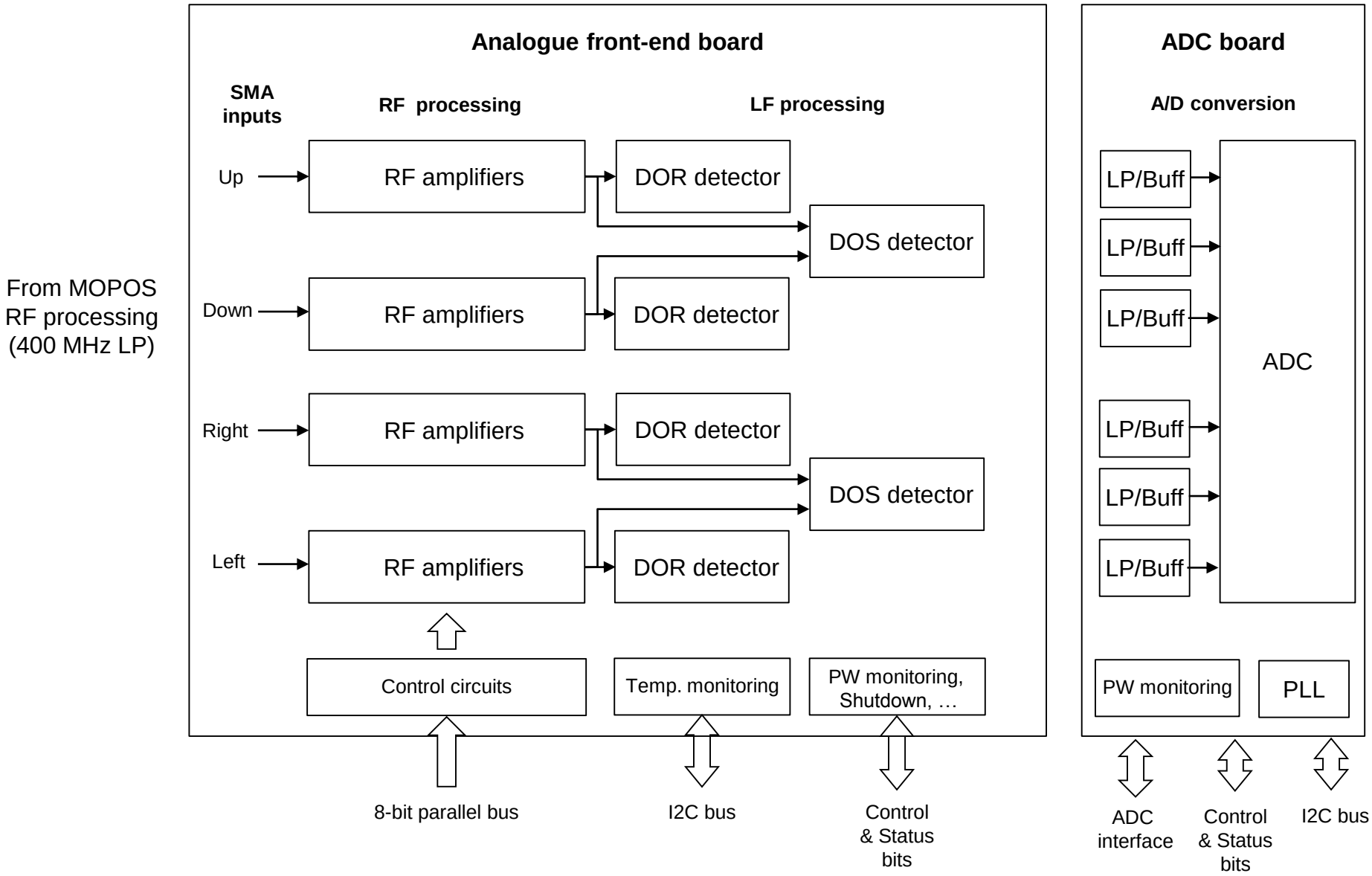
- Upload the latest firmware to the VFC and GEFE and test the chain with MOPOS firmware
- Start development of the DOROS firmware

Thank you for your attention!

Question(s)?

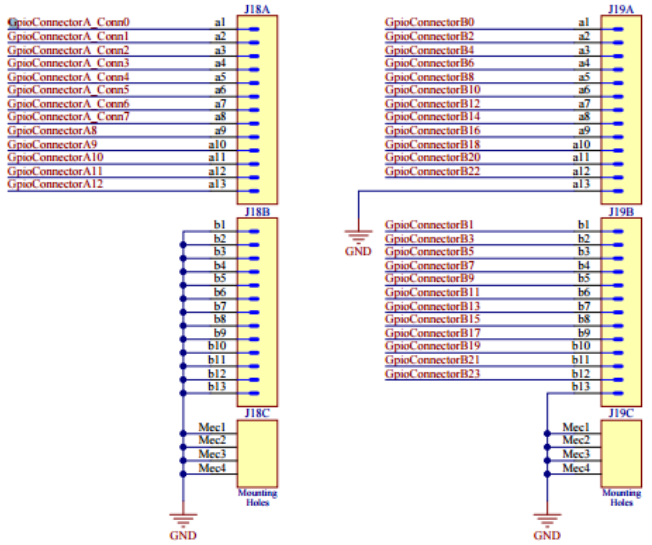
DOR(OS) 4 ALPS - basic block diagram

- Basic block diagram of the DOR(OS) front-end hardware



DOR(OS) 4 ALPS - interfacing with MOPOS

- Two connectors available on GEFE front-end (EDA-03168-v2)
  - 13-pin interleaved with GND, suitable for higher speed transmission
    - Pin count compatible only with ADCs with serial interfaces
    - Space for a few extra signals, like PLL lock and reset
  - 24-pin with two GND lines, adequate for slow control signals
    - Front-end parallel bus (8-bits + 2 strobes)
    - Place for I2C bus for optional functionality, like temperature, etc.
    - Place for optional signals like PW status



- Some 10 bits available in the GBTX stream from the GEFE front-end to the back-end
  - 400 Mbit/s
  - Used for ADC and auxiliary data serial transmission

- More bits available in the other direction from back-end to GEFE front-end
  - Will be used for controls

DOR(OS) 4 ALPS - ADC candidates

List of ADC test candidates suitable for DOROS application:

- AD7609 - 8-Channel Differential DAS with 18-Bit, Bipolar, Simultaneous Sampling ADC, (SAR)
  - Pin configurable SAR ADC, SPI interface
- AD7768 - 8-Channel, 24-Bit, Simultaneous Sampling, ADCs with Power Scaling, CRC-checks, (ΔΣ)
  - Partial pin configurable SAR ADC, CRC – checking with reset, SPI interfaces for data and control

- ADS855x - 16-Bit, Six-Channel, Simultaneous Sampling ADC, (SAR)
  - Pin configurable SAR ADC, SPI interface
- ADS1278 - Octal, Simultaneous Sampling, 24-Bit Analog-to-Digital Converters, (ΔΣ)
  - Pin configurable, available in consumer, high temperature (HT) and aerospace (EP) versions
- ADS1178 - Octal, Simultaneous Sampling, 16-Bit Analog-to-Digital Converters, (ΔΣ)

- LTC2321-16 - Dual, 16-Bit, 2Msps, Differential Input ADC with Wide Input Common Mode Range, (SAR)
  - Pin configurable, no missing codes for 16-bits

ANALOG DEVICES

8-Channel Differential DAS with 18-Bit, Bipolar, Simultaneous Sampling ADC

Data Sheet **AD7609**

FEATURES

- 8 simultaneously sampled inputs
- True differential inputs
- True bipolar analog input ranges: ±10 V, ±5 V
- Single 5 V analog supply and 2.3 V to 5.25 V V_{DRIVE}
- Fully integrated data acquisition solution
  - Analog input clamp protection
  - Input buffer with 1 MΩ analog input impedance
  - Second-order antialiasing analog filter
  - On-chip accurate reference and reference buffer
  - 18-bit ADC with 200 kSPS on all channels
  - Oversampling capability with digital filter
- Flexible parallel/serial interface
- SPI/QSPI™/MICROWIRE™/DSP compatible
- Performance
  - 7 kV ESD rating on analog input channels
  - 98 dB SNR, −107 dB THD
  - Dynamic range: up to 105 dB typical
  - Low power: 100 mW
  - Standby mode: 25 mW
- 64-lead LQFP package

APPLICATIONS

- Power line monitoring and protection systems
- Multiphase motor control
- Instrumentation and control systems
- Multiaxis positioning systems
- Data acquisition systems (DAS)

COMPANION PRODUCTS

External References: ADR421, ADR431
Digital Isolators: ADuM1402, ADuM5000, ADuM5402
Power: ADIsimPower, Supervisor Parametric Search
Additional companion products on the AD7609 product page

Table 1. High Resolution, Bipolar Input, Simultaneous Sampling DAS Solutions

Resolution	Single-Ended Inputs	True Differential Inputs	Number of Simultaneous Sampling Channels
18 Bits	AD7608	AD7609[1]	8
16 Bits	AD7606		8
	AD7606-6		6
	AD7606-4		4
14 Bits	AD7607		8

[1] Protected by U.S. Patent Number 8,072,360 B2.

FUNCTIONAL BLOCK DIAGRAM

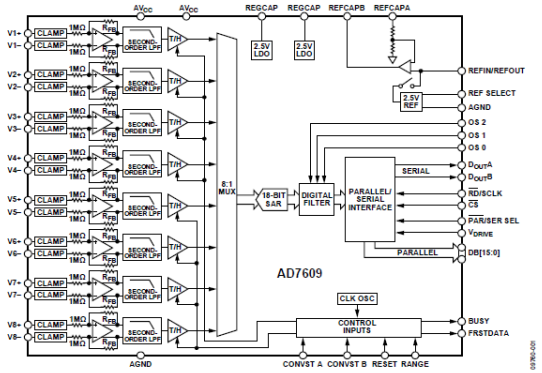


Figure 1.

Rev. B Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support www.analog.com

ANALOG DEVICES

8-/4-Channel, 24-Bit, Simultaneous Sampling ADCs with Power Scaling, 110.8 kHz BW

Data Sheet **AD7768/AD7768-4**

FEATURES

- Precision ac and dc performance
- 8-/4-channel simultaneous sampling
  - 256 kSPS maximum ADC output data rate per channel
  - 108 dB dynamic range
  - 110.8 kHz maximum input bandwidth (−3 dB bandwidth)
  - −120 dB total harmonic distortion (THD) typical
  - ±2 ppm of full-scale range (FSR) integral nonlinearity (INL), ±50 µV offset error, ±30 ppm gain error
- Optimized power dissipation vs. noise vs. input bandwidth
  - Selectable power, speed, and input bandwidth (BW) modes
    - Fast: highest speed; 110.8 kHz BW, 51.5 mW per channel
    - Median: half speed, 55.4 kHz BW, 27.5 mW per channel
    - Eco: lowest power, 13.8 kHz BW, 9.375 mW per channel
  - Input BW range: dc to 110.8 kHz
  - Programmable input bandwidth/sampling rates
- Cyclic redundancy check (CRC) error checking on data interface
- Daisy-chaining
- Linear phase digital filter
  - Low latency sinc5 filter
  - Wideband brick wall filter: ±0.005 dB pass-band ripple from dc to 102.4 kHz
- Analog input precharge buffers
- Power supply
  - AVDD1 = 5.0 V, AVDD2 = 2.25 V to 5.0 V
  - IOVDD = 2.5 V to 3.3 V or IOVDD = 1.8 V
- 64-lead LQFP package, no exposed pad
- Temperature range: −40°C to +105°C

APPLICATIONS

- Data acquisition systems: USB/PXI/Ethernet
- Instrumentation and industrial control loops
- Audio test and measurement
- Vibration and asset condition monitoring
- 3-phase power quality analysis
- Sonar
- High precision medical electroencephalogram (EEG)/ electromyography (EMG)/electrocardiogram (ECG)

FUNCTIONAL BLOCK DIAGRAM

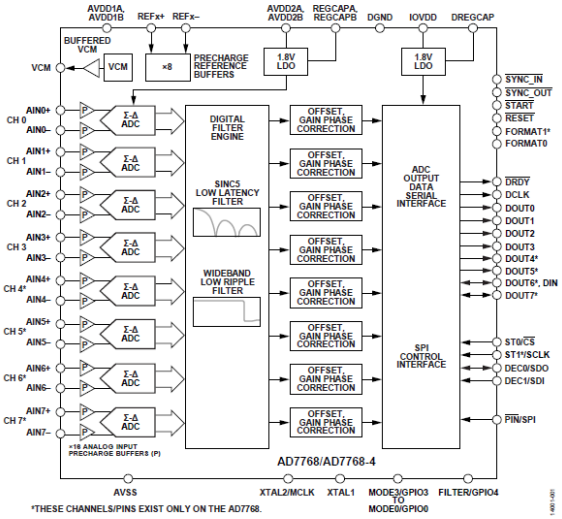


Figure 1.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700

Technical Support
www.analog.com

TEXAS INSTRUMENTS

ADS1174
ADS1178

www.ti.com SBAS373B–OCTOBER 2007–REVISED SEPTEMBER 2008

Quad/Octal, Simultaneous Sampling, 16-Bit Analog-to-Digital Converters

FEATURES

- Simultaneously Sample Four/Eight Channels
- Selectable Operating Modes:
  High-Speed: 52kSPS Data Rate, 31mW/ch
  Low-Power: 10kSPS Data Rate, 7mW/ch
- AC Performance:
  25kHz Bandwidth
  97dB SNR
  –105dB THD
- DC Performance:
  2μV/°C Offset Drift
  2ppm/°C Gain Drift
- Digital Filter:
  Linear Phase Response
  Passband Ripple: ±0.005dB
  Stop Band Attenuation: 100dB
- Selectable SPI™ or Frame Sync Serial Interface
- Simple Pin-Driven Control
- Low Sampling Aperture Error
- Specified from –40°C to +105°C
- Analog Supply: 5V
- I/O Supply: 1.8V to 3.3V
- Digital Core Supply: 1.8V

APPLICATIONS

- 3-Phase Power Monitors
- Defibrillators and ECG Monitors
- Coriolis Flow Meters
- Vibration/Modal Analysis

DESCRIPTION

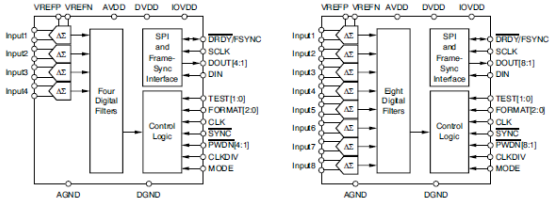
The ADS1174 (quad) and ADS1178 (octal) are multiple delta-sigma (ΔΣ) analog-to-digital converters (ADCs) with data rates up to 52k samples-per-second (SPS), which allow synchronous sampling of four and eight channels. These devices use identical packages, and are also compatible with the high-performance 24-bit ADS1274 and ADS1278, permitting drop-in upgrades.

The delta-sigma architecture offers near ideal 16-bit ac performance (97dB SNR, –105dB THD, 1LSB linearity) combined with 0.005dB passband ripple and linear phase response.

The high-order, chopper-stabilized modulator achieves very low drift (2μV/°C offset, 2ppm/°C gain) and low noise ($1LSB_{PP}$). The on-chip finite impulse response (FIR) filter provides a usable signal bandwidth up to 90% of the Nyquist rate with 100dB of stop band attenuation while suppressing modulator and signal out-of-band noise.

Two operating modes allow for optimization of speed and power: High-speed mode (31mW/Ch at 52kSPS), and Low-power mode (7mW/Ch at 10kSPS).

A $\overline{SYNC}$ input control pin allows the device conversions to be started and synchronized to an external event. SPI and Frame-Sync serial interfaces are supported. The device is fully specified over the extended industrial range (–40°C to +105°C) and is available in an HTQFP-64 PowerPAD™ package.



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TEXAS INSTRUMENTS

ADS1274
ADS1278

www.ti.com SBAS367F – JUNE 2007 – REVISED FEBRUARY 2011

Quad/Octal, Simultaneous Sampling, 24-Bit Analog-to-Digital Converters

Check for Samples: ADS1274, ADS1278

FEATURES

- Simultaneously Measure Four/Eight Channels
- Up to 144kSPS Data Rate
- AC Performance:
  70kHz Bandwidth
  111dB SNR (High-Resolution Mode)
  –108dB THD
- DC Accuracy:
  0.8μV/°C Offset Drift
  1.3ppm/°C Gain Drift
- Selectable Operating Modes:
  High-Speed: 144kSPS, 106dB SNR
  High-Resolution: 52kSPS, 111dB SNR
  Low-Power: 52kSPS, 31mW/ch
  Low-Speed: 10kSPS, 7mW/ch
- Linear Phase Digital Filter
- SPI™ or Frame-Sync Serial Interface
- Low Sampling Aperture Error
- Modulator Output Option (digital filter bypass)
- Analog Supply: 5V
- Digital Core: 1.8V
- I/O Supply: 1.8V to 3.3V

APPLICATIONS

- Vibration/Modal Analysis
- Multi-Channel Data Acquisition
- Acoustics/Dynamic Strain Gauges
- Pressure Sensors

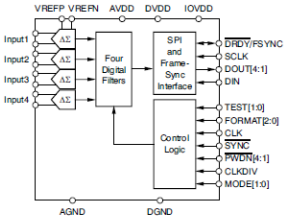
DESCRIPTION

Based on the single-channel ADS1271, the ADS1274 (quad) and ADS1278 (octal) are 24-bit, delta-sigma (ΔΣ) analog-to-digital converters (ADCs) with data rates up to 144k samples per second (SPS), allowing simultaneous sampling of four or eight channels. The devices are offered in identical packages, permitting drop-in expandability.

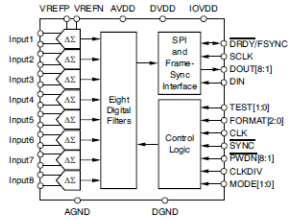
Traditionally, industrial delta-sigma ADCs offering good drift performance use digital filters with large passband droop. As a result, they have limited signal bandwidth and are mostly suited for dc measurements. High-resolution ADCs in audio applications offer larger usable bandwidths, but the offset and drift specifications are significantly weaker than respective industrial counterparts. The ADS1274 and ADS1278 combine these types of converters, allowing high-precision industrial measurement with excellent dc and ac specifications.

The high-order, chopper-stabilized modulator achieves very low drift with low in-band noise. The onboard decimation filter suppresses modulator and signal out-of-band noise. These ADCs provide a usable signal bandwidth up to 90% of the Nyquist rate with less than 0.005dB of ripple.

Four operating modes allow for optimization of speed, resolution, and power. All operations are controlled directly by pins; there are no registers to program. The devices are fully specified over the extended industrial range (–40°C to +105°C) and are available in an HTQFP-64 PowerPAD™ package.



ADS1274



ADS1278

TEXAS INSTRUMENTS

ADS8556, ADS8557, ADS8558
SBAS404D – OCTOBER 2006 – REVISED FEBRUARY 2016

ADS855x
16-, 14-, 12-Bit, Six-Channel, Simultaneous Sampling Analog-to-Digital Converters

1 Features

- Family of 16-, 14-, 12-Bit, Pin- and Software-Compatible ADCs
- Six SAR ADCs Grouped in Three Pairs
- Maximum Data Rate Per Channel with Internal Conversion Clock and Reference:
  ADS8556: 630 kSPS (PAR) or 450 kSPS (SER)
  ADS8557: 670 kSPS (PAR) or 470 kSPS (SER)
  ADS8558: 730 kSPS (PAR) or 500 kSPS (SER)
- Maximum Data Rate with External Conversion Clock and Reference:
  800 kSPS (PAR) or 530 kSPS (SER)
- Pin-Selectable or Programmable Input Voltage Ranges: Up to ±12 V
- Excellent Signal-to-Noise Performance:
  ADS8556: 91.5 dB, ADS8667: 85 dB,
  ADS8668: 73.9 dB
- Programmable and Buffered Internal Reference:
  0.5 V to 2.5 V and 0.5 V to 3.0 V
- Comprehensive Power-Down Modes:
  – Deep Power-Down (Standby Mode)
  – Partial Power-Down
  – Auto-Nap Power-Down
- Selectable Parallel or Serial Interface
- Operating Temperature Range: –40°C to 125°C

2 Applications

- Power Quality Measurement
- Protection Relays
- Multi-Axis Motor Control
- Programmable Logic Controllers
- Industrial Data Acquisition

3 Description

The ADS855x contains six low-power, 16-, 14-, or 12-bit, successive approximation register (SAR) based analog-to-digital converters (ADCs) with true bipolar inputs. Each channel contains a sample-and-hold circuit that allows simultaneous high-speed multi-channel signal acquisition.

The ADS855x supports data rates of up to 730 kSPS in parallel interface mode or up to 500 kSPS if the serial interface is used. The bus width of the parallel interface can be set to eight or 16 bits. In serial mode, up to three output channels can be activated.

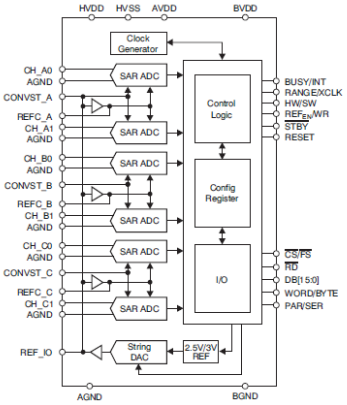
The ADS855x is specified over the full industrial temperature range of –40°C to 125°C and is available in an LQFP-64 package.

Device Information(1)

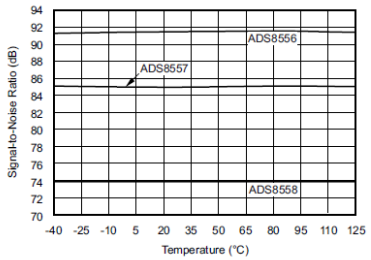
PART NUMBER	PACKAGE	BODY SIZE (NOM)
ADS8556	LQFP (64)	10.00 mm × 10.00 mm
ADS8557		
ADS8558		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Block Diagram



SNR vs Temperature



LINEAR TECHNOLOGY

LTC2321-16

Dual, 16-Bit, 2Msps Differential Input ADC with Wide Input Common Mode Range

FEATURES

- **2Msps Throughput Rate**
- **±4LSB INL (Typ)**
- **Guaranteed 16-Bit, No Missing Codes**
- **$8V_{P-P}$ Differential Inputs with Wide Input Common Mode Range**
- **81dB SNR (Typ) at f_{IN} = 500kHz**
- **–90dB THD (Typ) at f_{IN} = 500kHz**
- No Cycle Latency
- Guaranteed Operation to 125°C
- Single 3.3V or 5V Supply
- Low Drift (20ppm/°C Max) 2.048V or 4.096V Internal Reference
- 1.8V to 2.5V I/O Voltages
- CMOS or LVDS SPI-Compatible Serial I/O
- Power Dissipation 31mW/Ch (Typ)
- Small 28-Lead (4mm × 5mm) QFN Package

APPLICATIONS

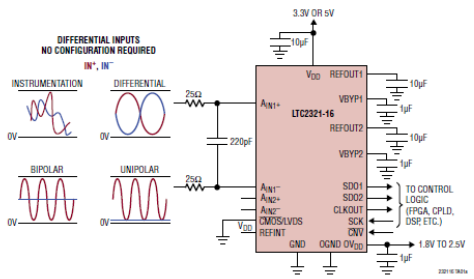
- High Speed Data Acquisition Systems
- Communications
- Remote Data Acquisition
- Imaging
- Optical Networking
- Automotive
- Multiphase Motor Control

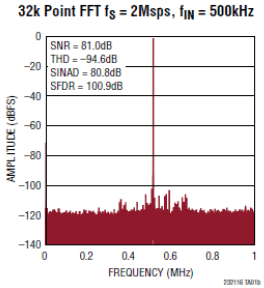
DESCRIPTION

The LTC®2321-16 is a low noise, high speed dual 16-bit successive approximation register (SAR) ADC with differential inputs and wide input common mode range. Operating from a single 3.3V or 5V supply, the LTC2321-16 has an $8V_{P-P}$ differential input range, making it ideal for applications which require a wide dynamic range with high common mode rejection. The LTC2321-16 achieves ±4LSB INL typical, no missing codes at 16 bits and 81dB SNR.

The LTC2321-16 has an onboard low drift (20ppm/°C max) 2.048V or 4.096V temperature-compensated reference. The LTC2321-16 also has a high speed SPI-compatible serial interface that supports CMOS or LVDS. The fast 2Msps per channel throughput with no cycle latency makes the LTC2321-16 ideally suited for a wide variety of high speed applications. The LTC2321-16 dissipates only 31mW per channel and offers nap and sleep modes to reduce the power consumption to 5µW for further power savings during inactive periods.

TYPICAL APPLICATION





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