Contribution ID: **152** Type: **Oral**

Design and Characterisation of the Monolithic Matrices of the H35DEMO Chip

Wednesday, 13 September 2017 11:30 (25 minutes)

The H35DEMO chip is a HV/HR-MAPS demonstrator of 18.49 mm x 24.4 mm, fabricated with a 0.35 µm HVCMOS process from AMS in four different substrate resistivities. The chip is divided into four independent matrices with a pixel size of 50 µm x 250 µm. Two of the matrices include all the digital readout electronics at the periphery. This contribution describes the two standalone matrices of the H35DEMO chip and will present the results of two testbeams carried out with unirradiated and irradiated samples with different substrate resistivities.

Summary

High Voltage/High Resistivity Depleted Monolithic Active Pixels (HV/HR-DMAPS) is a technology which is being investigated for the 5th layer of the Inner Tracker of the ATLAS detector at HL-LHC. Currently, several groups have started to develop some demonstrators in order to validate this technology at large scale in different CMOS processes. The H35DEMO is the first HV/HR-DMAP demonstrator built. It was fabricated with a 350nm HVCMOS process in 4 different substrate resistivities: 20, 80, 200, and 1000 Ω•cm. It includes four different matrices with a pixel size of 50 µm x 250 µm. The pixels of two of them include analog front-end electronics and have to be readout with an FEI4 chip. In the other two, the pixels also include analog readout electronics together with digital electronics to readout them out in the periphery.

The two standalone matrices are composed of 16 rows and 300 columns. One of the pixel matrices is called nMOS because the analog front-end electronics are mainly composed of a preamplifier, a shaper, and a discriminator that only uses nMOS transistors. In these pixels, the pMOS transistors are built in the DNWELL which is the collecting node. If a CMOS discriminator was used instead of a nMOS, the large voltage commutations would inject noise directly to the DNWELL. Two different types of nMOs discriminators were implemented. The first half of the matrix contains a simple nMOS comparator while the second half contains a more complex nMOS discriminator which compensates the time-walk. The output of the discriminators is converted to a CMOS signal in a readout cell (ROC) connected to each pixel by means of a CMOS discriminator. The second matrix is called CMOS and the pixels are like those of the nMOS matrix but with no nMOs discriminator. The output of the shaper is discriminated by a CMOS comparator placed at the readout cell connected to the pixel. The ROCs are the same for both matrices and are placed at the periphery arranged in a matrix of 120 columns and 40 rows. They store an 8-bits global time stamp into a DRAM when a hit is detected. The architecture of these cells is column drain and the layout was made full custom in order to embed all the electronics in 125 x 20 µm2. Each column is terminated with an End Of Column (EOC). It stores the time stamp and data of the read pixel.

The readout of the matrix is asynchronous, zero suppressed and triggerless. The matrix is handled by a control unit and reads sequentially the content of each EOC cell at 40MHz. The read data is passed to 2 serializers that transmit the data off-chip at 320MHz through LVDS pads.

A first testbeam was carried out at CERN in late 2016. Unirradiated samples of 200Ω•cm were used and efficiencies of around 97% were measured. A new testbeam campaign was done during April 2017 at Fermilab. This campaign was more extensive and irradiated samples with different substrate resistivities were tested. The results of this testbeam will be presented during the conference.

Primary author: CASANOVA MOHR, Raimon (Universitat Autònoma de Barcelona (ES))

Co-authors: TERZO, Stefano (IFAE Barcelona (ES)); CAVALLARO, Emanuele (IFAE - Barcelona (ES)); FORSTER, Fabian Alexander (IFAE Barcelona (ES)); PUIGDENGOLES OLIVE, Carles (IFAE - Institut de Física d'Altes Energies-Universitat Autònoma); GRINSTEIN, Sebastian (IFAE - Barcelona (ES)); PERIC, Ivan (KIT - Karlsruhe Institute of Technology (DE)); BENOIT, Mathieu (UNIGE); VILELLA FIGUERAS, Eva (University of Liverpool (GB))

Presenter: CASANOVA MOHR, Raimon (Universitat Autònoma de Barcelona (ES))

Session Classification: ASIC

Track Classification: ASIC