CBC3: A CMS micro-strip readout ASIC with logic for track-trigger modules at HL-LHC

STFC RAL: Mark Prydderch, S. Bell, M. Charrier, L. Jones, P.Murray, D. Braga†

Imperial College: G. Auzinger, J. Borg, G. Hall, M. Pesaresi, M. Raymond, K. Uchida

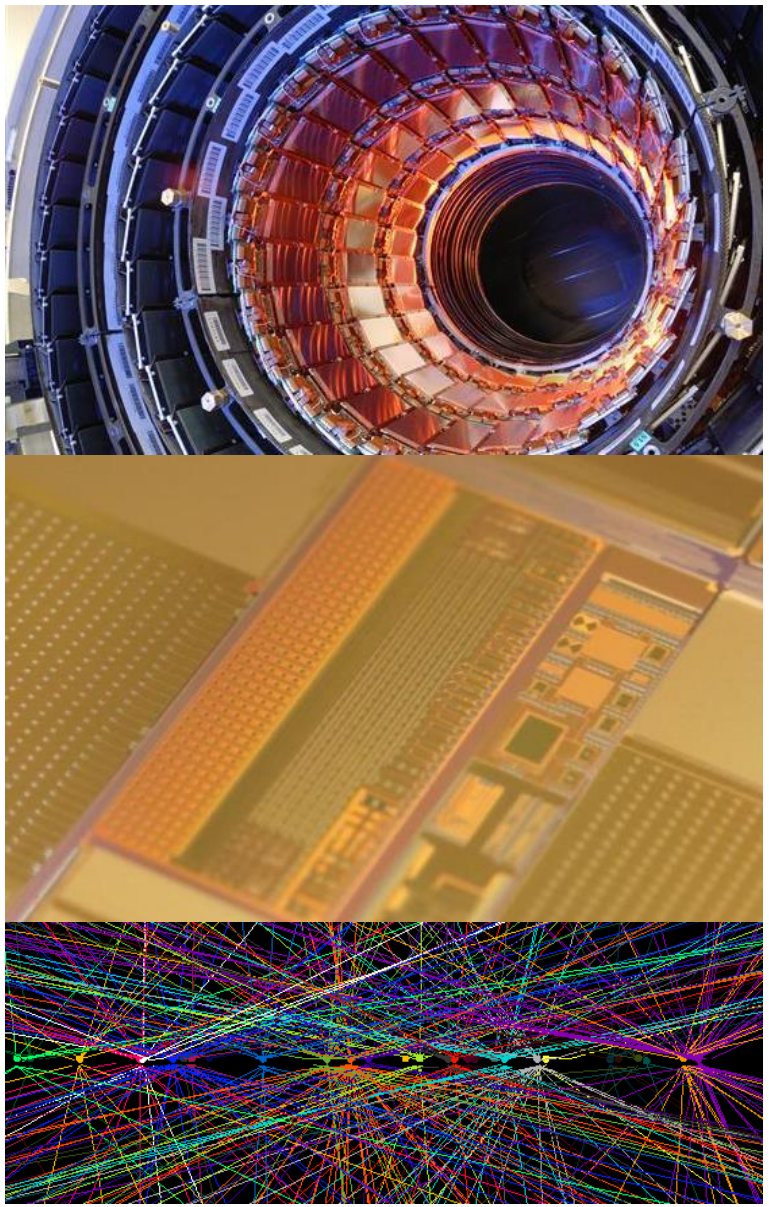
University of Bristol: J. Goldstein, S. Seif El Nasr

†Now at Fermilab

Imperial College London

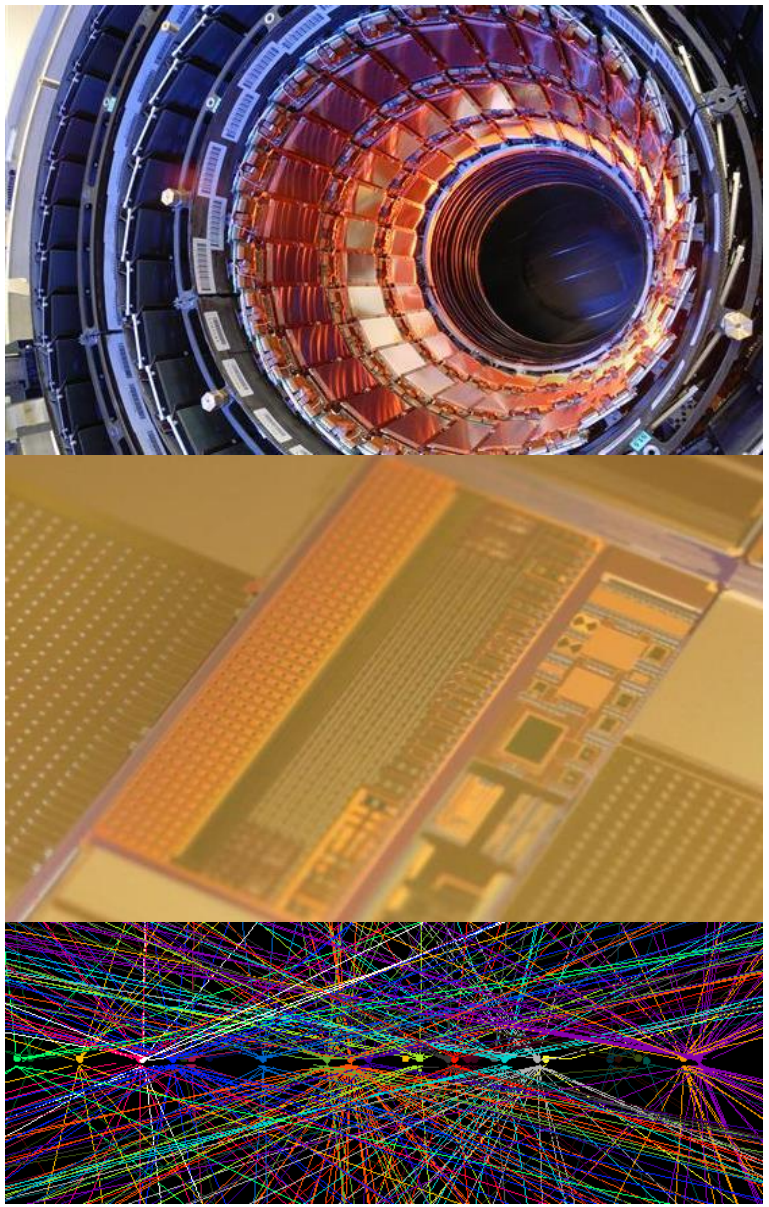
Science & Technology Facilities Council

Outline



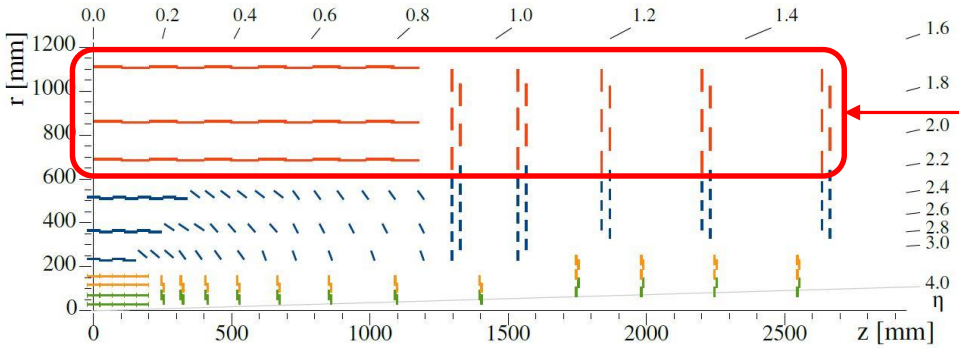
- Background
- CBC3 Features
- CBC3 Single Chip Testing
- Future work
- Summary & Conclusion

Outline

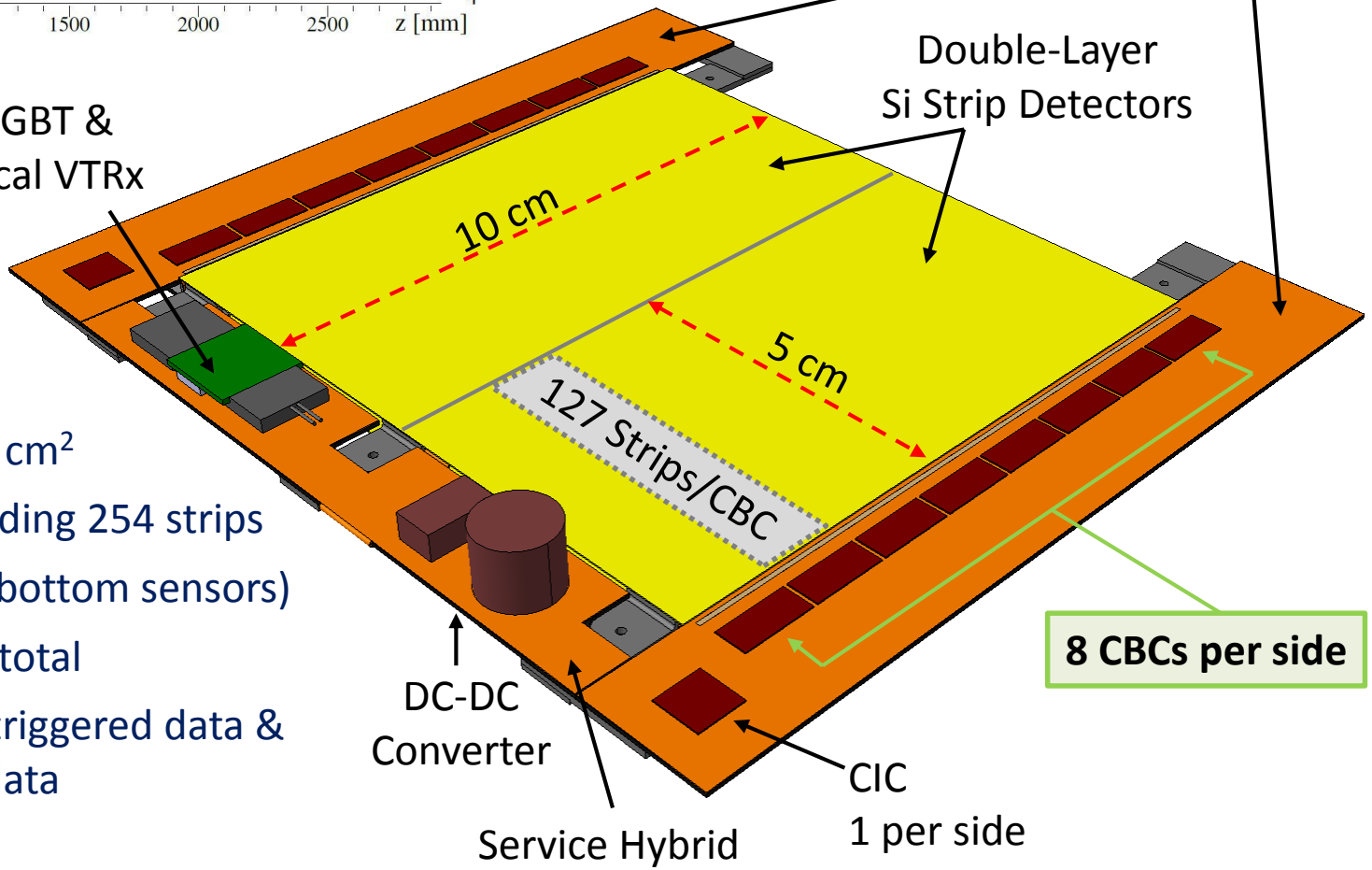


- **Background**
- CBC3 Features
- CBC3 Single Chip Testing
- Future work
- Summary & Conclusion

Where to find the CBC



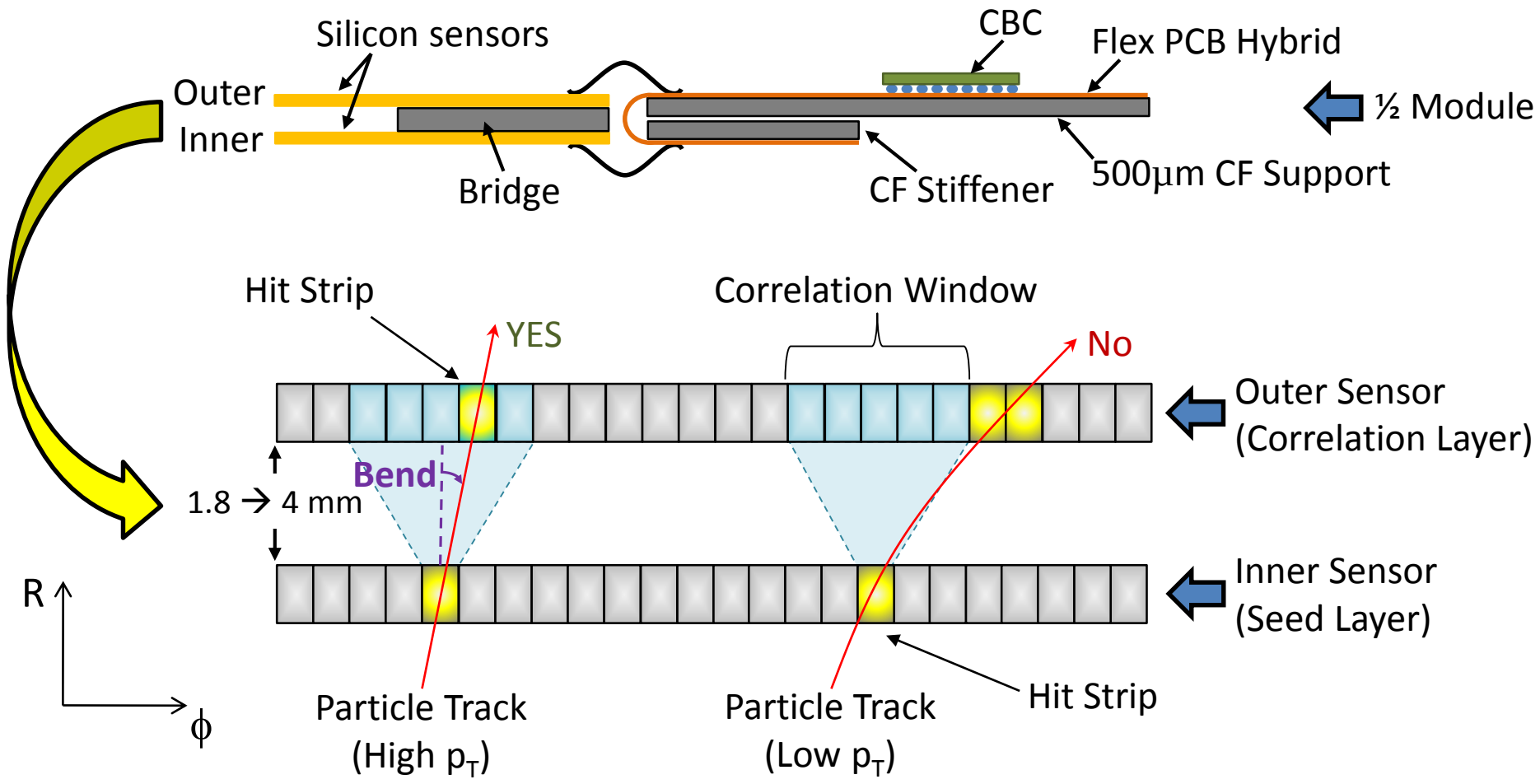
- 2S Modules: Two-strip double-layers
- 7680 modules
- ~31M channels



Each 2S Module:

- Sensor Area ~100 cm^2
- 16 CBCs, each reading 254 strips (127 from top & bottom sensors)
- 4064 Channels in total
- Readout both L1 triggered data & Primitive trigger data

Basic 2S Module Concept



- High-PT tracks (**Stubs**) can be identified if cluster centre in top layer lies within a correlation window in R-Φ (rows)
- p_T cut given by: module radius (z), sensor separation and correlation window

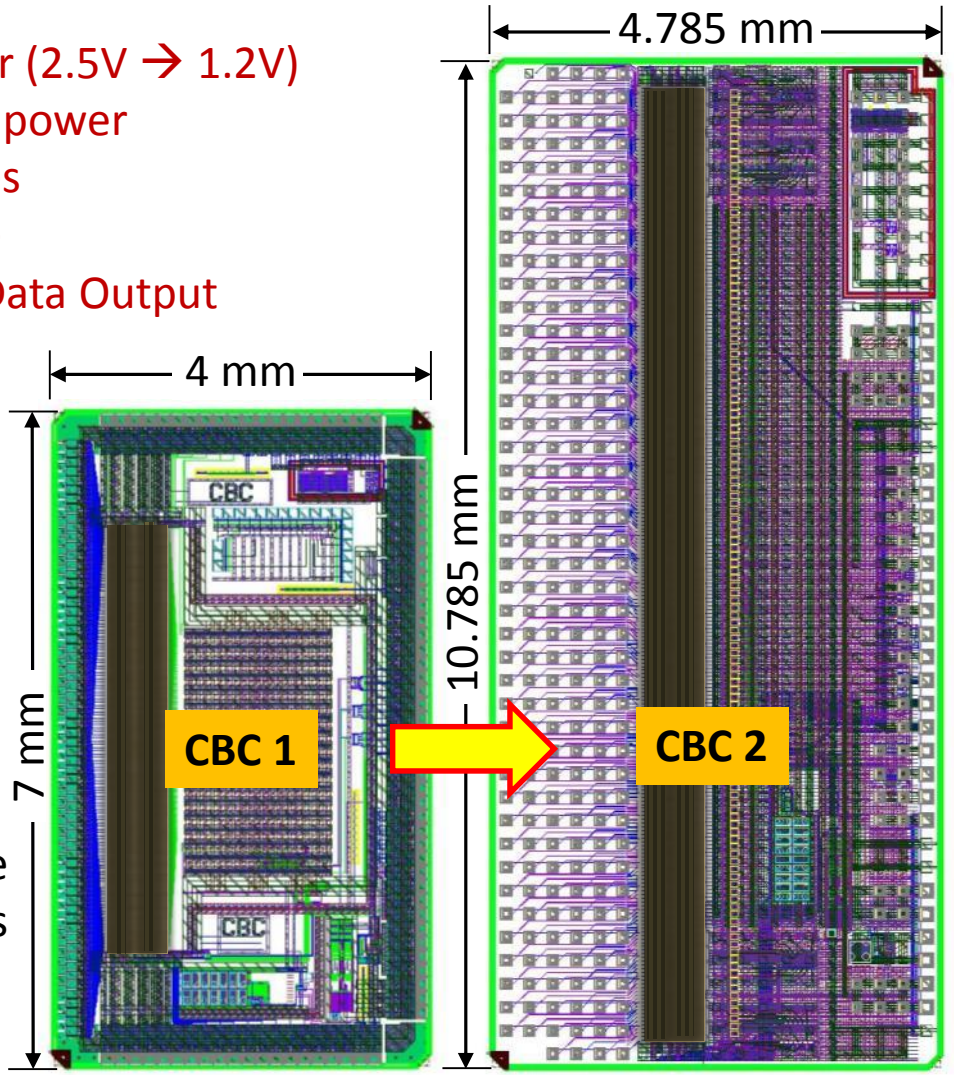
CBC1 & CBC2

Common features:

- I^2C Interface
- DC – DC Converter (2.5V → 1.2V)
- LDO for analogue power
- Bandgap for biases
- 256 deep Pipeline
- 40MHz Serial L1 Data Output

CBC1 (2011)

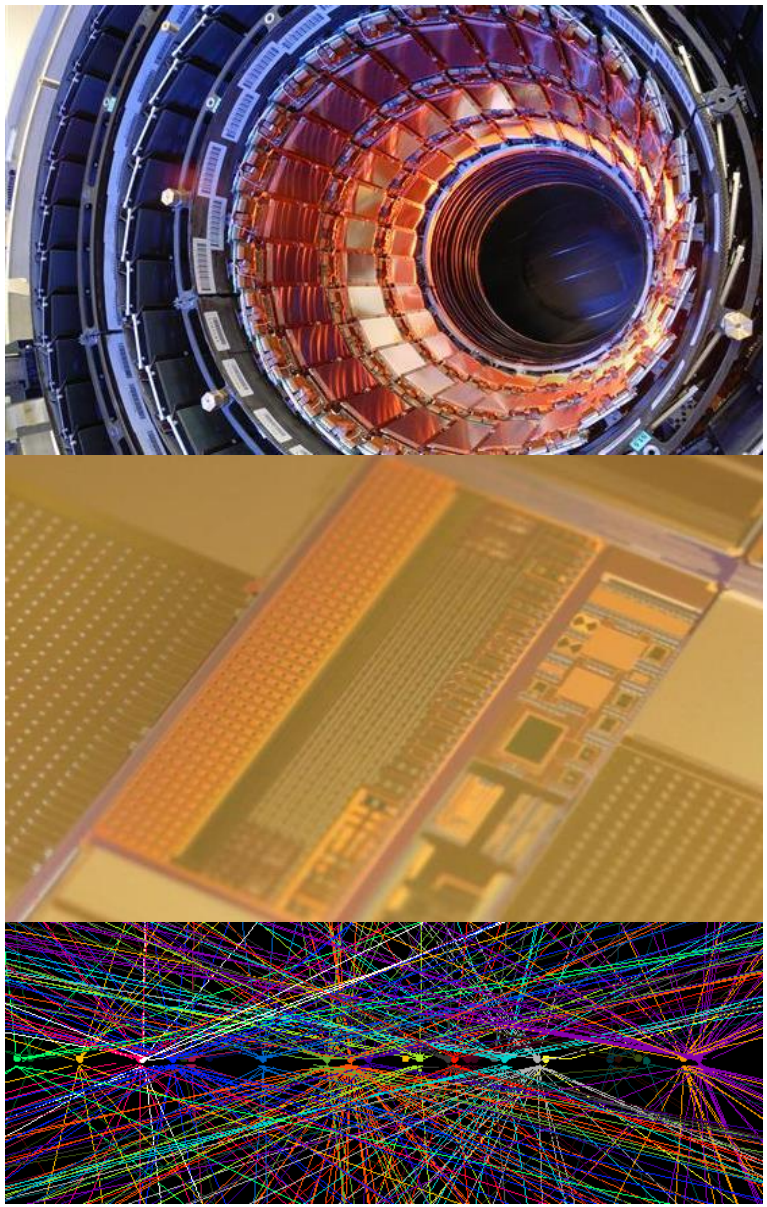
- 128 Dual polarity channels
- Wire Bonded
- APV style serial command scheme
- Analog Test Inputs



CBC2 (2013)

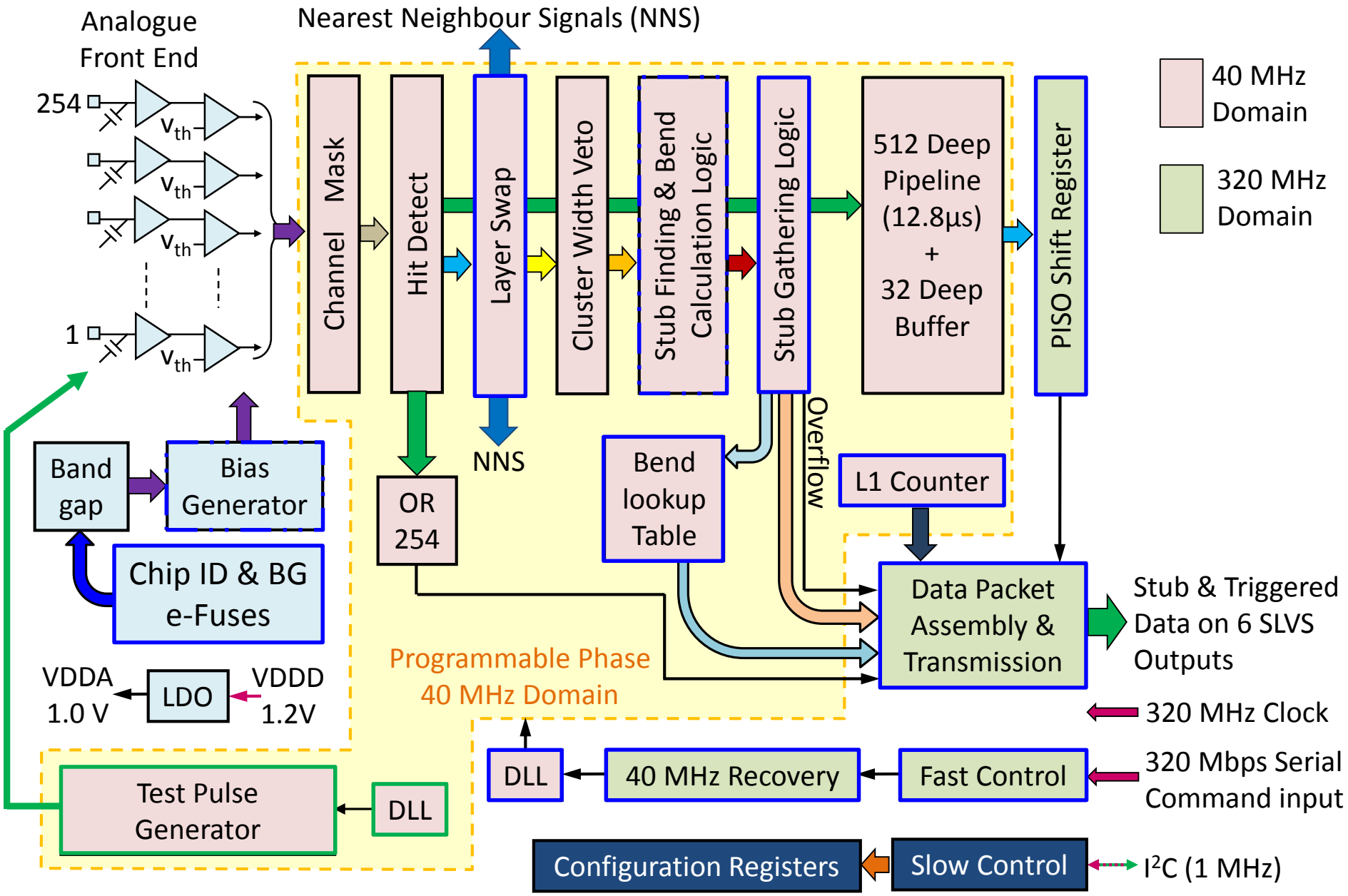
- 254 Dual polarity channels
- C4 Bump Bonded
- Direct command inputs
- On-chip Test Pulse Generator with DLL
- Correlation logic for stub formation
- Cluster width veto
- 40MHz serial readout of Stub Data
- Analogue Mux for bias monitoring
- Front-end circuit improvements
- Improved DC-DC converter (CERN)

Outline

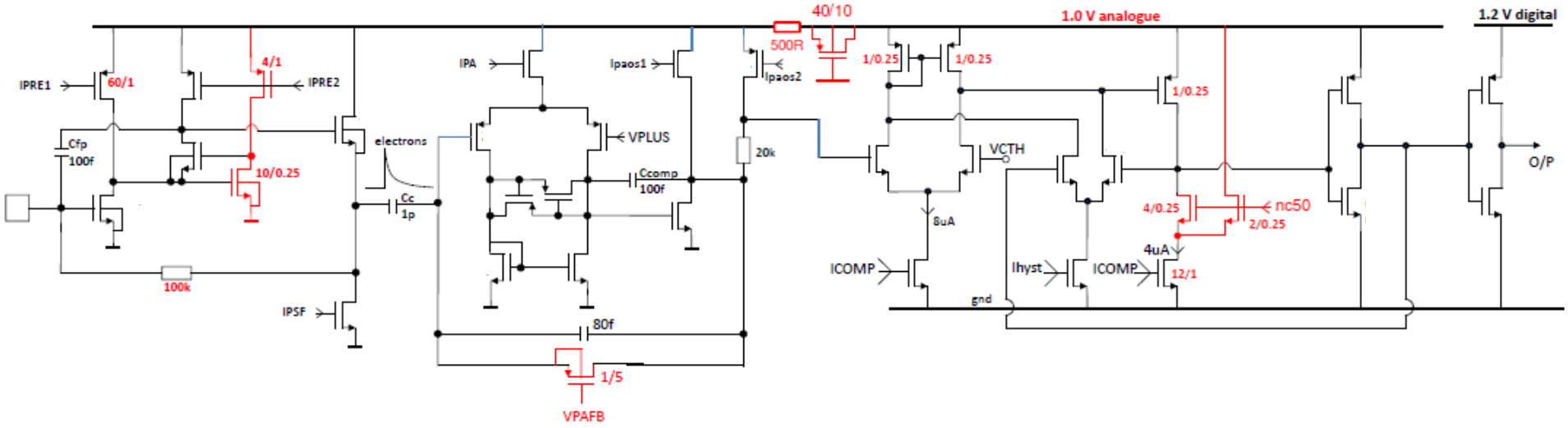


- Background
- **CBC3 Features**
- CBC3 Single Chip Testing
- Future work
- Summary & Conclusion

CBC3 Architecture



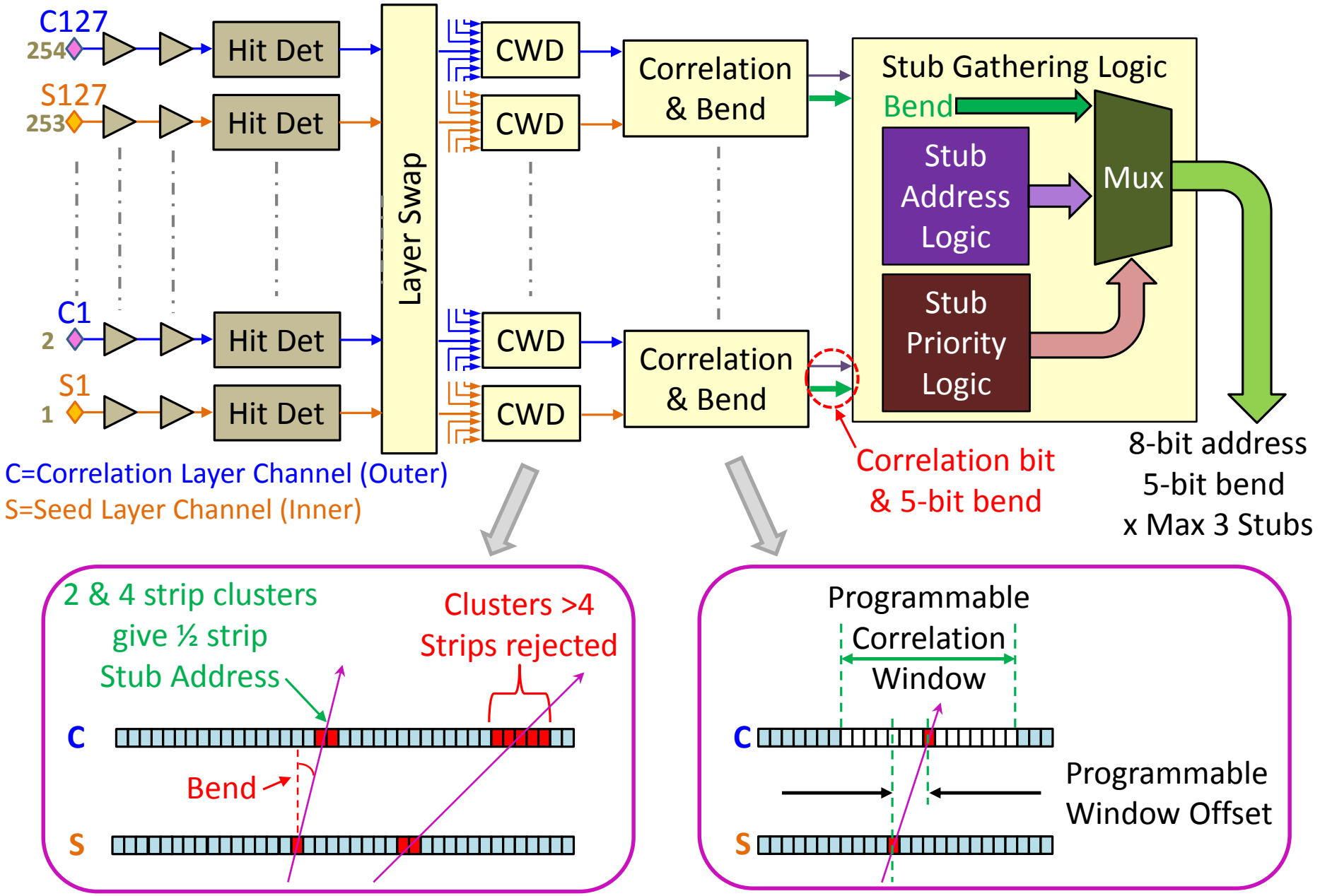
CBC3 Front End Changes



- Single Polarity (electrons)
- Faster Pulse Shape
- 3x Bias current range for larger detector capacitances
- New preamp regulated cascode to eliminate “Shadow effect” observed when many channels fire
- New postamp feedback bias scheme (not shown)
- Current neutral comparator
- Adjusted for 1V operation

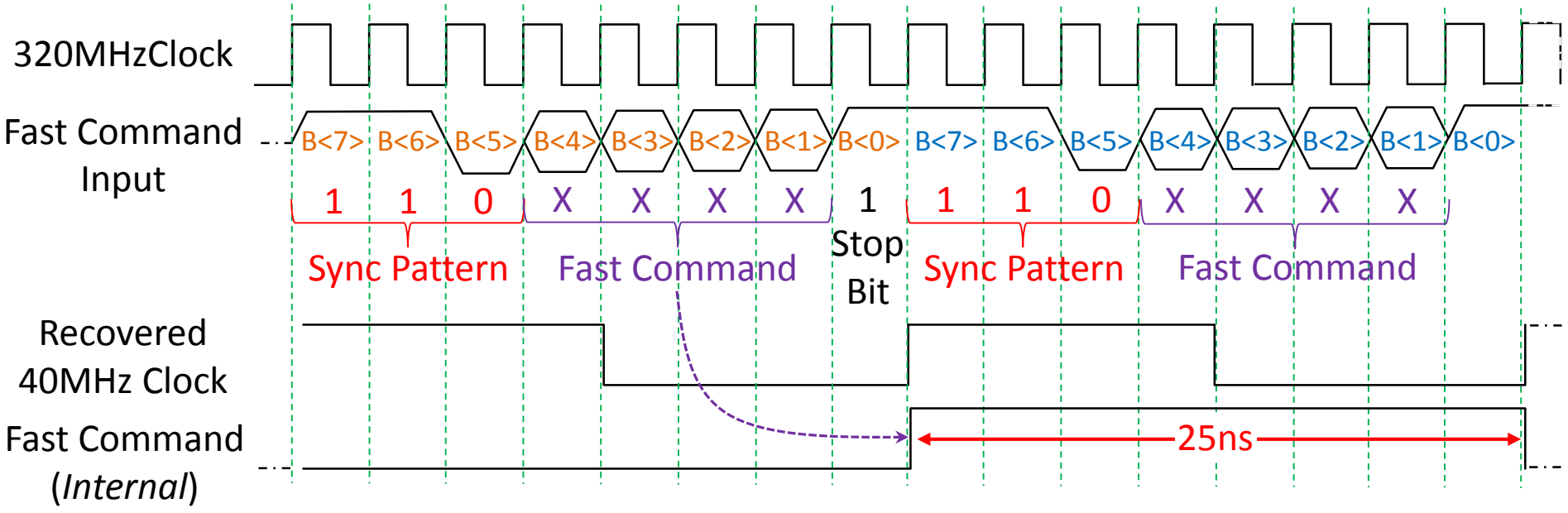
} Eliminate common-mode effects observed when many channels fire

Stub Logic

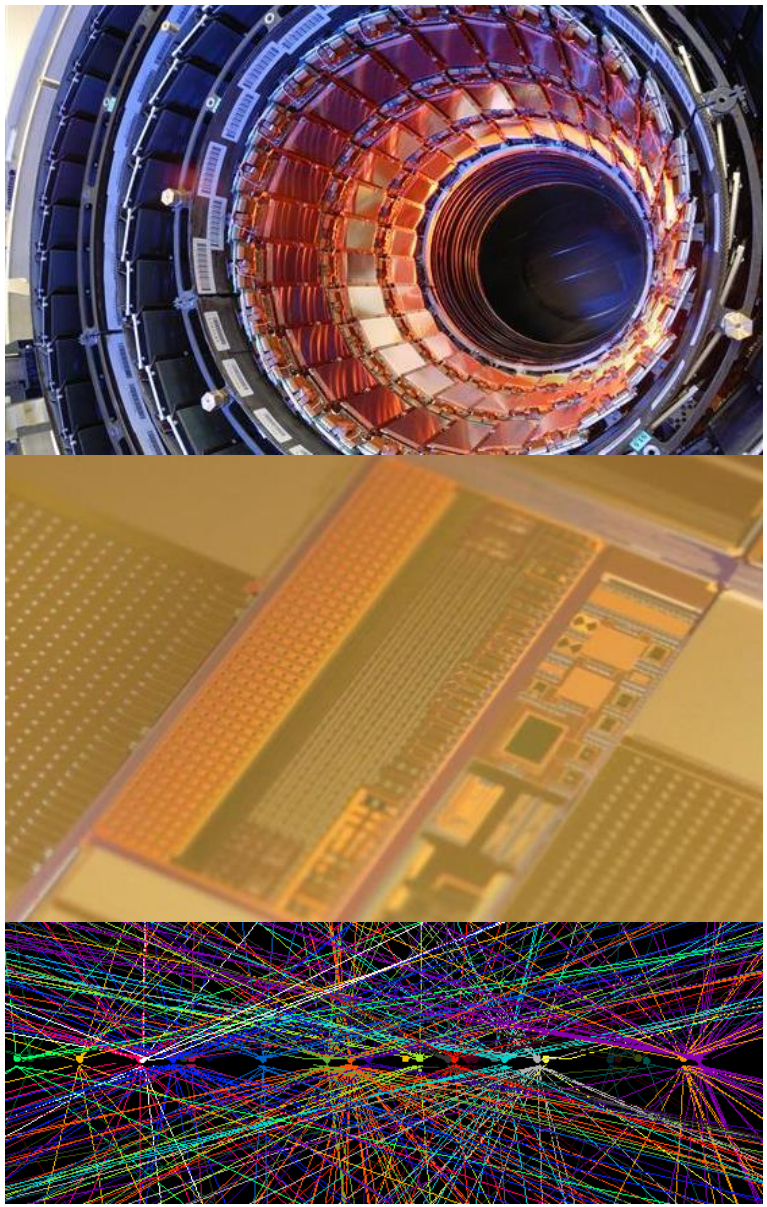

C127
254
S127
253
C1
2
S1
1
Hit Det
Hit Det
Hit Det
Hit Det
Layer Swap
CWD
CWD
CWD
CWD
Correlation & Bend
Correlation & Bend
Stub Gathering Logic
Bend
Stub Address Logic
Stub Priority Logic
Mux
C=Correlation Layer Channel (Outer)
S=Seed Layer Channel (Inner)
Correlation bit & 5-bit bend
8-bit address
5-bit bend
x Max 3 Stubs
2 & 4 strip clusters give ½ strip Stub Address
Clusters >4 Strips rejected
C
Bend
S
Programmable Correlation Window
C
S
Programmable Window Offset

Fast Command Interface

Fast Command	B7	B6	B5	B4	B3	B2	B1	B0
Fast Reset	1	1	0	1	0	0	0	1
Trigger	1	1	0	0	1	0	0	1
Test Pulse Trigger	1	1	0	0	0	1	0	1
Orbit Reset	1	1	0	0	0	0	1	1
Orbit Reset & *Fast Reset*	1	1	0	1	0	0	1	1
Orbit Reset & *Trigger*	1	1	0	0	1	0	1	1
Orbit Reset & *Test Pulse Trigger*	1	1	0	0	0	1	1	1



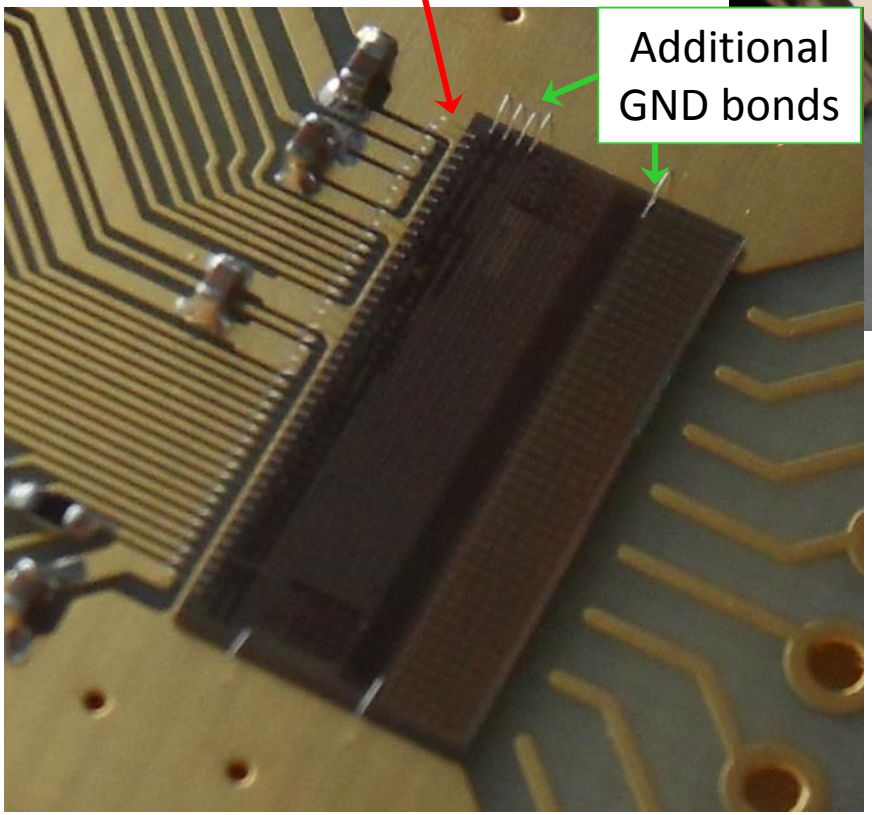
Outline

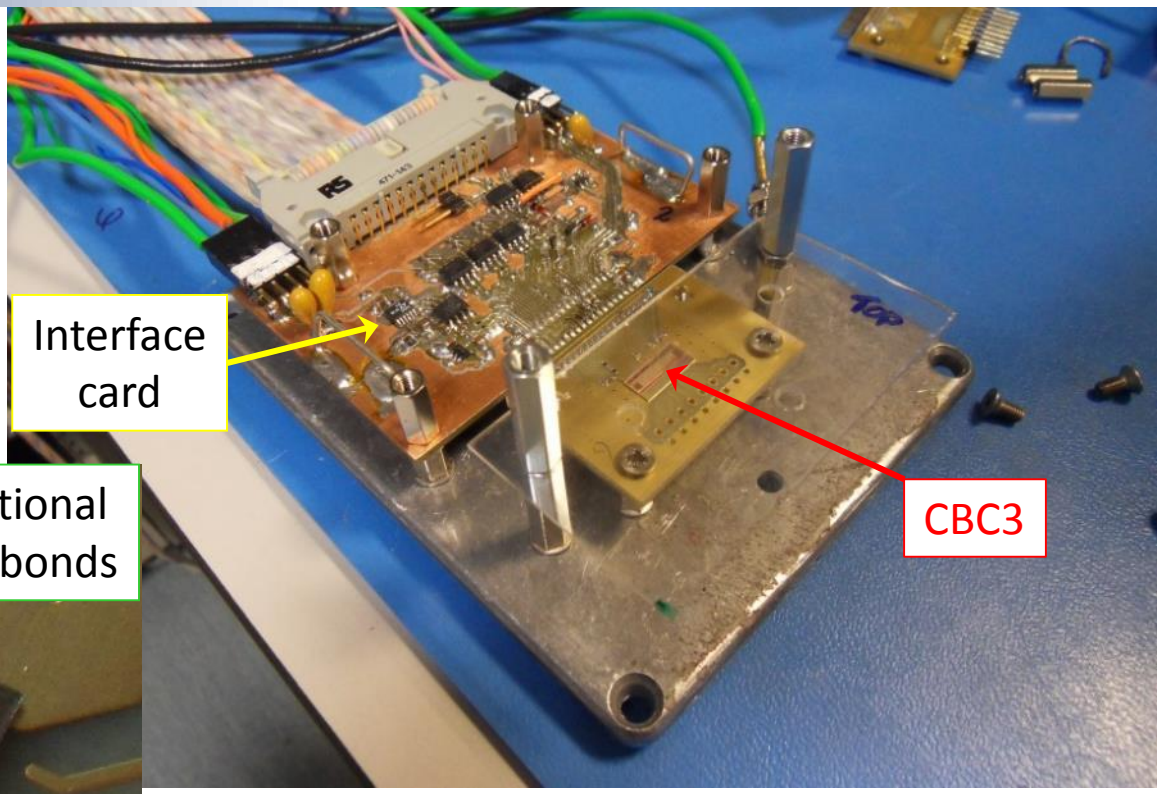


- Background
- CBC3 Features
- **CBC3 Single Chip Testing**
- Future work
- Summary & Conclusion

Single Chip Test PCB

- Tests carried out at Imperial
- Back-edge column of pads reserved for wafer probing - can be wire-bonded

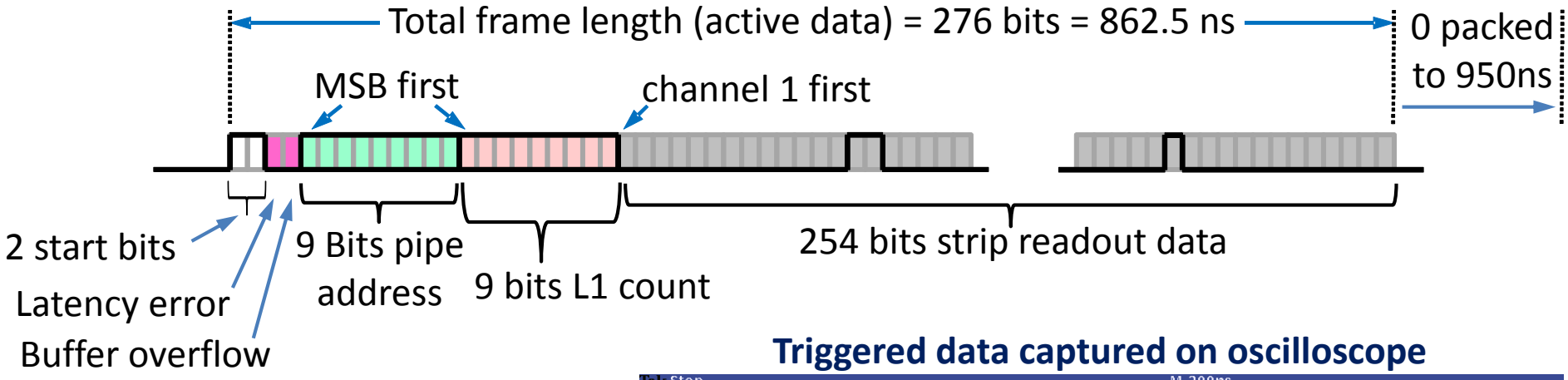




- **All CBC3 results so far are from a wire-bonded single chip setup**
  - (chips diced from first wafer)
- ~Same setup used for ionizing and SEU tests

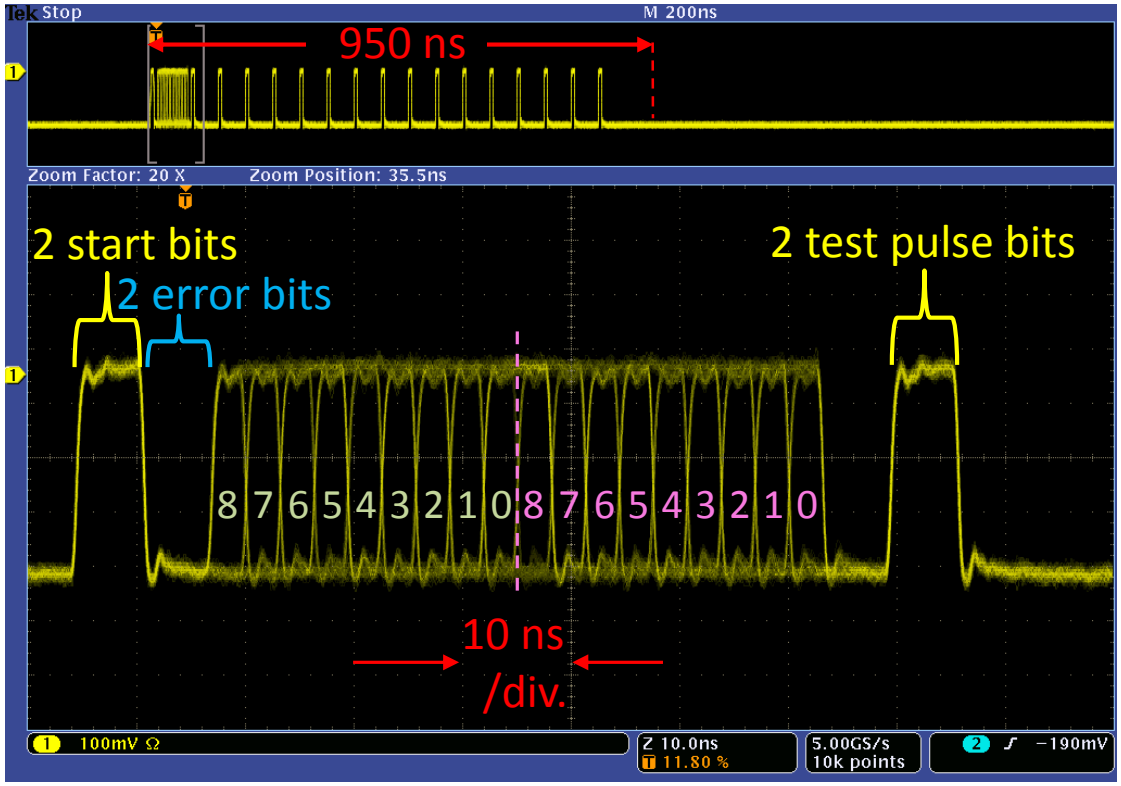
Triggered Data Readout

Triggered data packet format

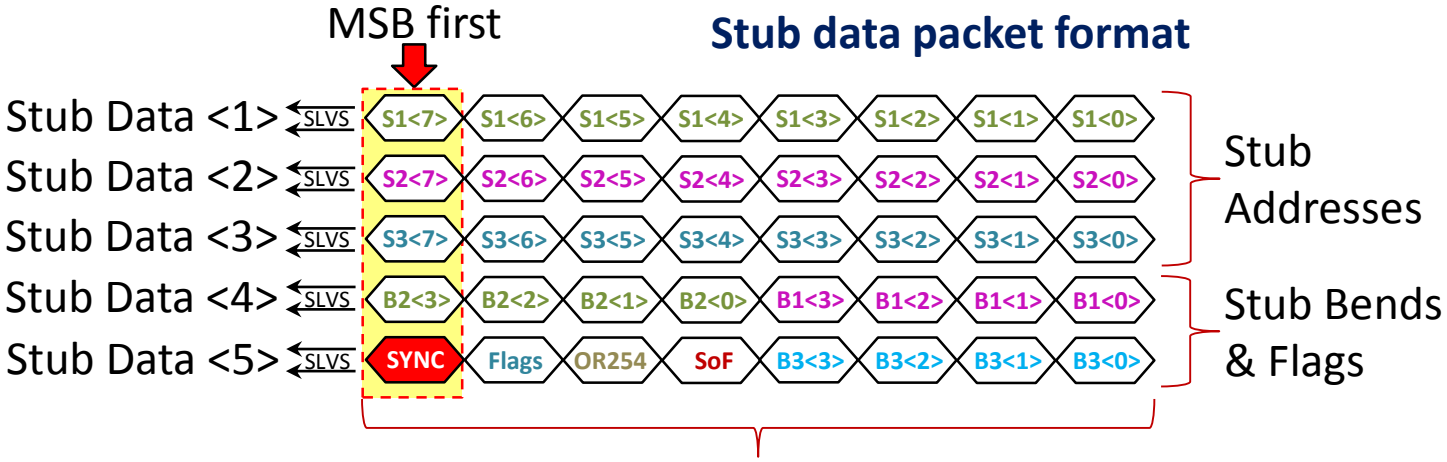


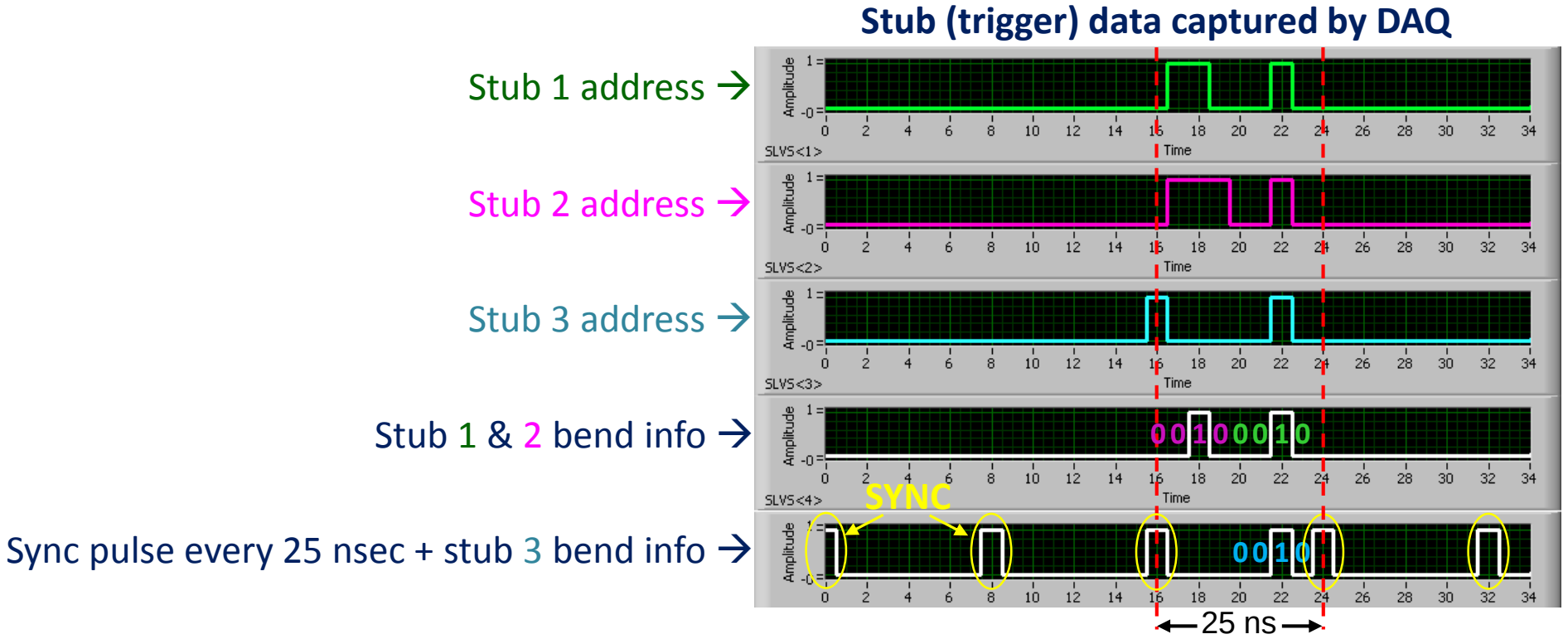
- 320 Mbps triggered output data
- Frame length 950 ns
- Header contains the pipeline address that the data originates from + L1 counter value (reset every orbit)
- SLVS output driver
- On-chip test pulse used

Triggered data captured on oscilloscope

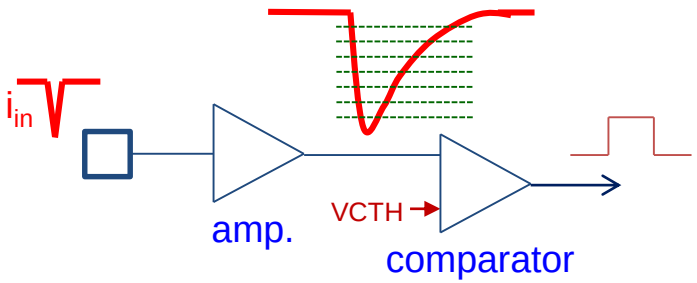


Stub Data Readout



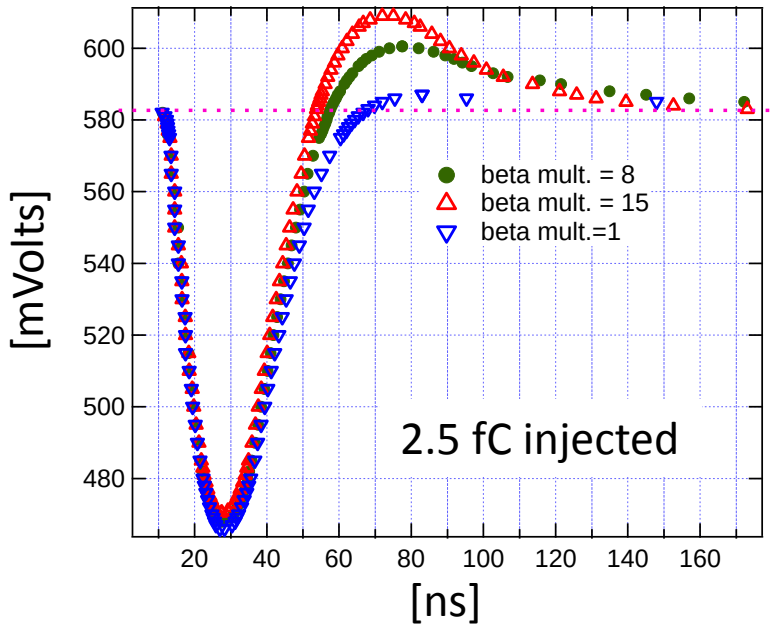


Front End Pulse Shape

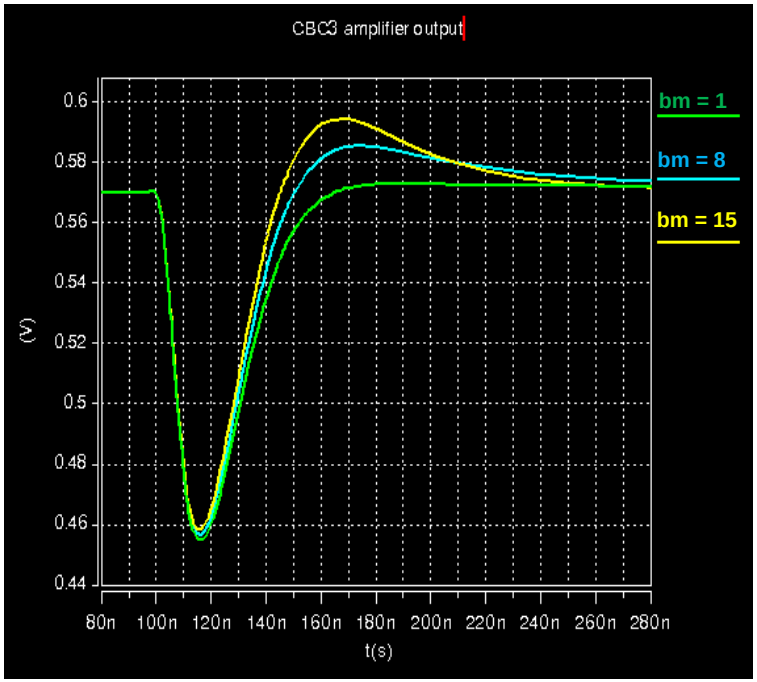


- We can measure the analogue pulse shapes by sweeping the charge injection time for different comparator thresholds

Measurement



Simulation

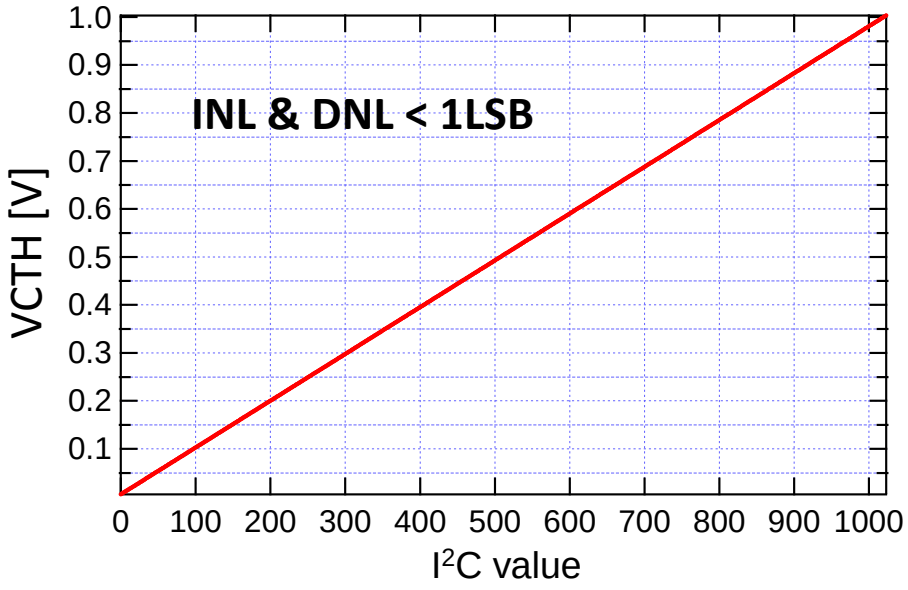


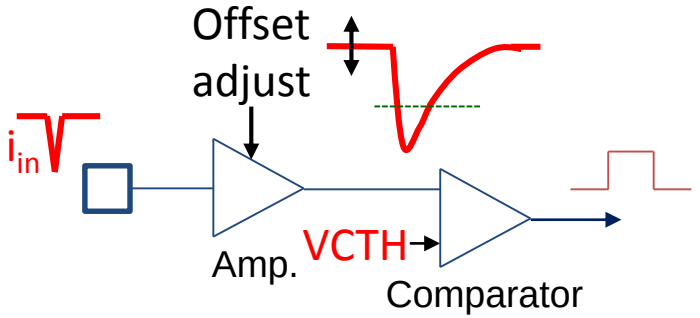
- Good pulse shape agreement between simulation and measurement
- CBC3 pulse shape duration reduced (cf. CBC2) to achieve single BX resolution
- Varying 4-bit beta multiplier setting gives some control over output pulse duration

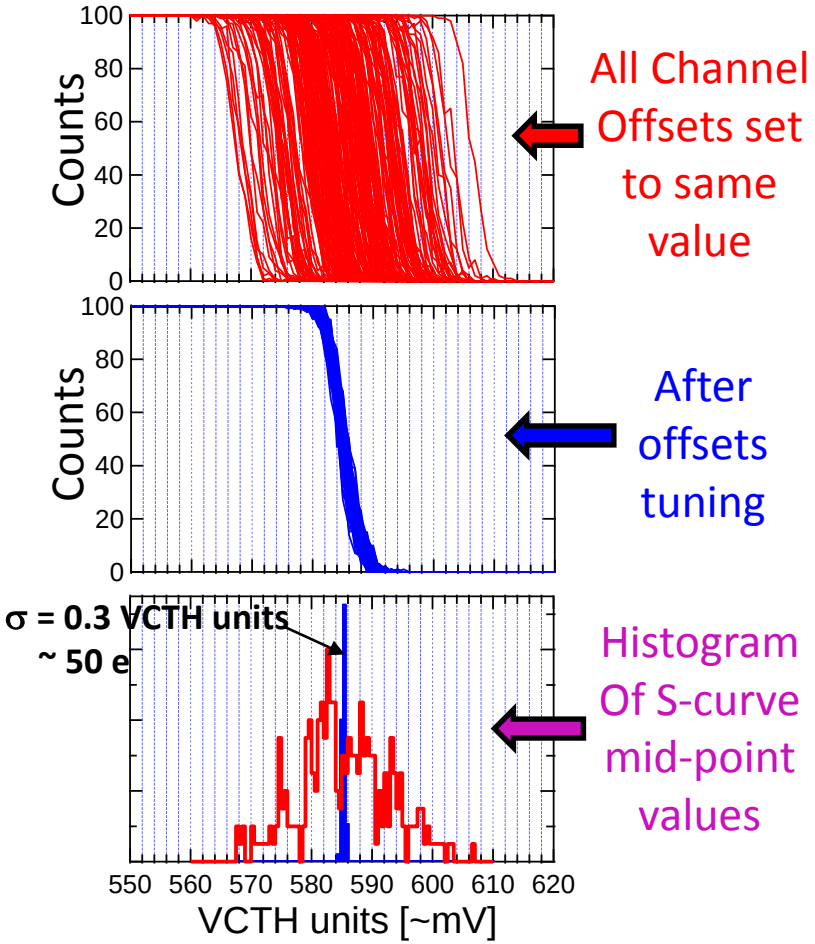
S-curves & Channel Offsets Tuning

- Sweep global comparator threshold to generate s-curves
- Tune offsets to compensate for channel-to-channel differences
- After tuning, the channel offsets distribution has **σ** of ~50 electrons

VCTH now generated by 10-bit resistor ladder DAC

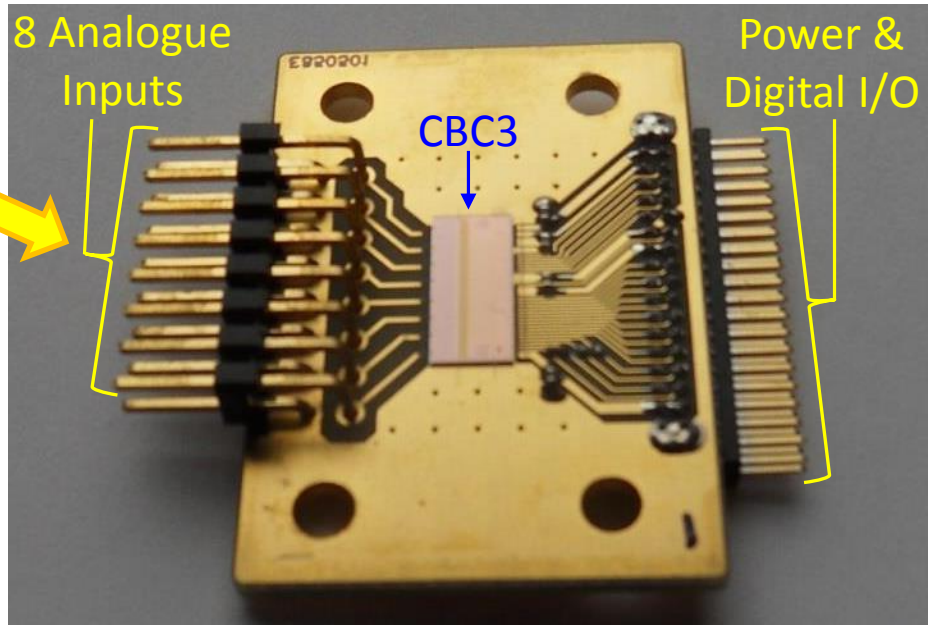




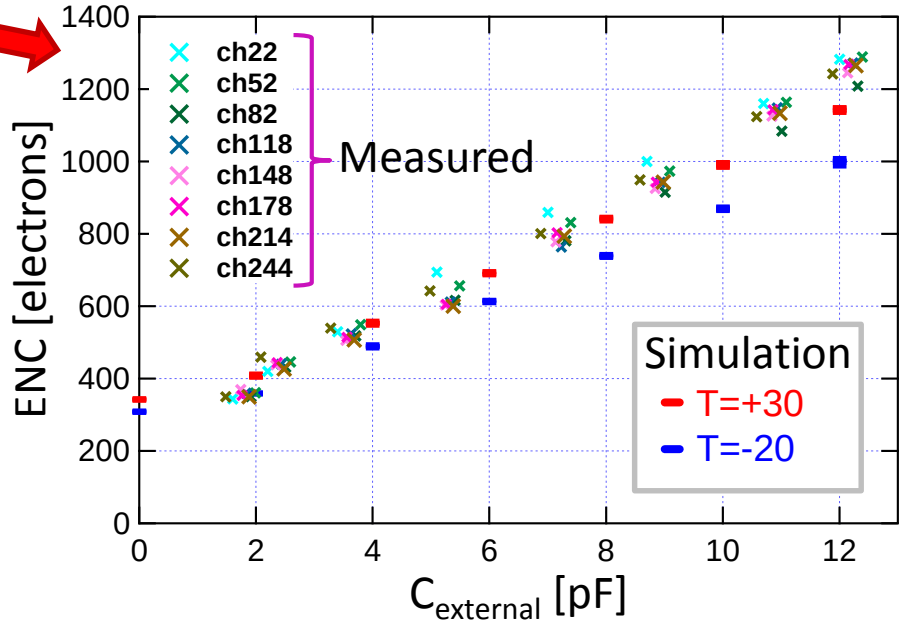


Noise, Gain & Power

- Single chip test board has provision to bond 8 inputs
- CBC3 bump-bond pads have wire-bondable finish (**unlike CBC2's C4 pads**)
- Can make use of this to inject external charge and add external capacitance to measure noise



- Single-chip setup noise performance looks ok (even with a wire-bonded chip)



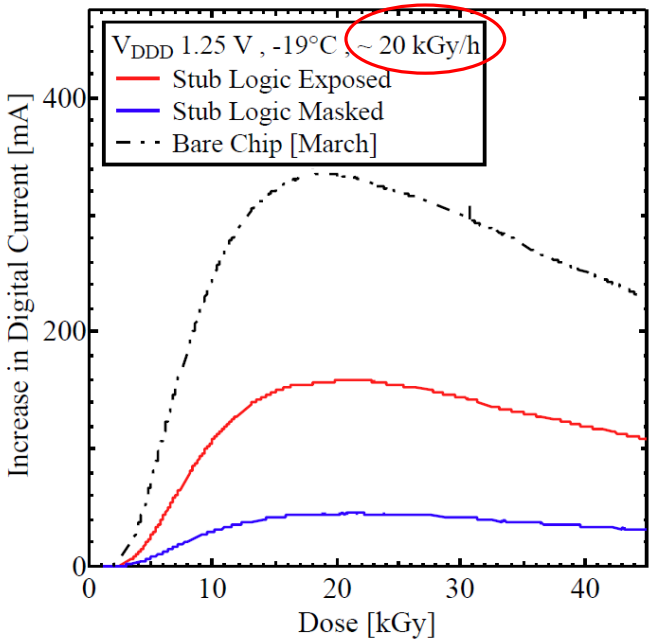
- Measured Gain 47 mV/fC with ~5% spread

- 350 µW/Channel Analogue
- 160 µW/Channel Digital

Radiation Studies

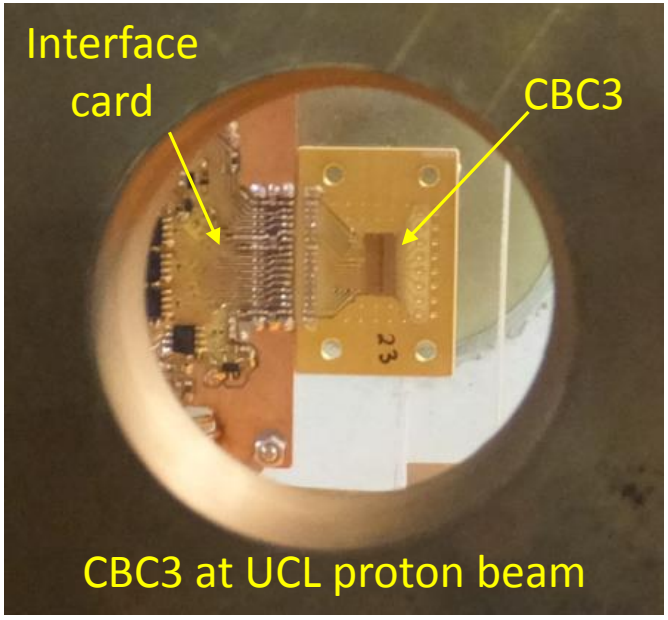
Ionising Radiation Tests at CERN:

- CBC3 irradiated to > 400 kGy
- No change in performance (noise, pedestals,…)
- Transient increase in digital current in few Mrad region falls back to pre-irradiation values at higher doses
- Current dominated by leakage in stub-finding logic
- At HL-LHC dose-rate (9 Gy/hr) & temp (-15°) the effect will be negligible (pessimistic assumptions)
  - ~1.3% max. increase in module power consumption

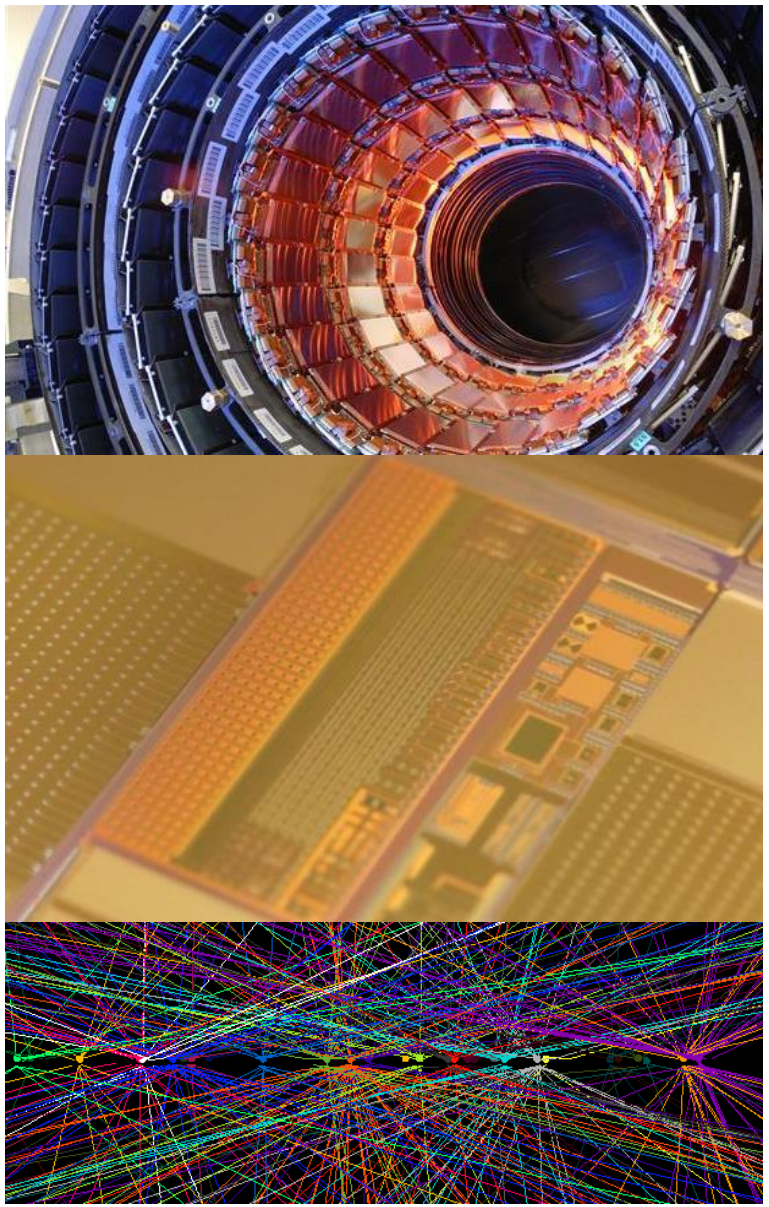


SEU Tests on Proton Beam at UCL (Louvain):

- ~15 hours of beam corresponds to ~1000 hours @ HL-LHC
- Detected 25 single bit flips altogether in I^2C registers
  - ~ 8x reduction cf. CBC2
- Corresponds to ~1.5 bit-flips/day per chip at HL-LHC (pessimistic assumptions)
- Considering periodic reconfiguration vs minor changes to circuit



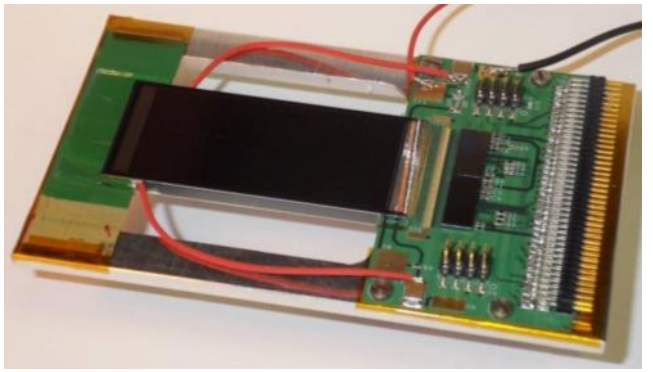
Outline

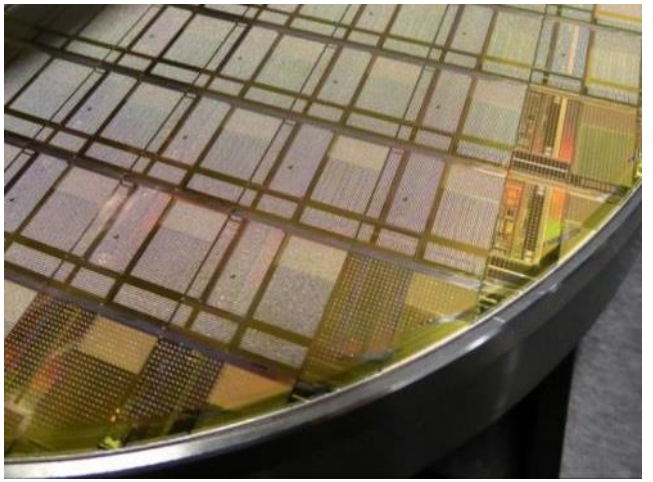


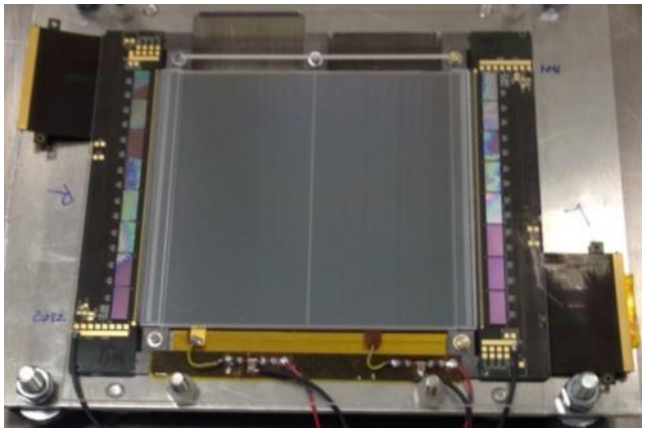
- Background
- CBC3 Features
- CBC3 Single Chip Testing
- **Future work**
- Summary & Conclusion

Future Work

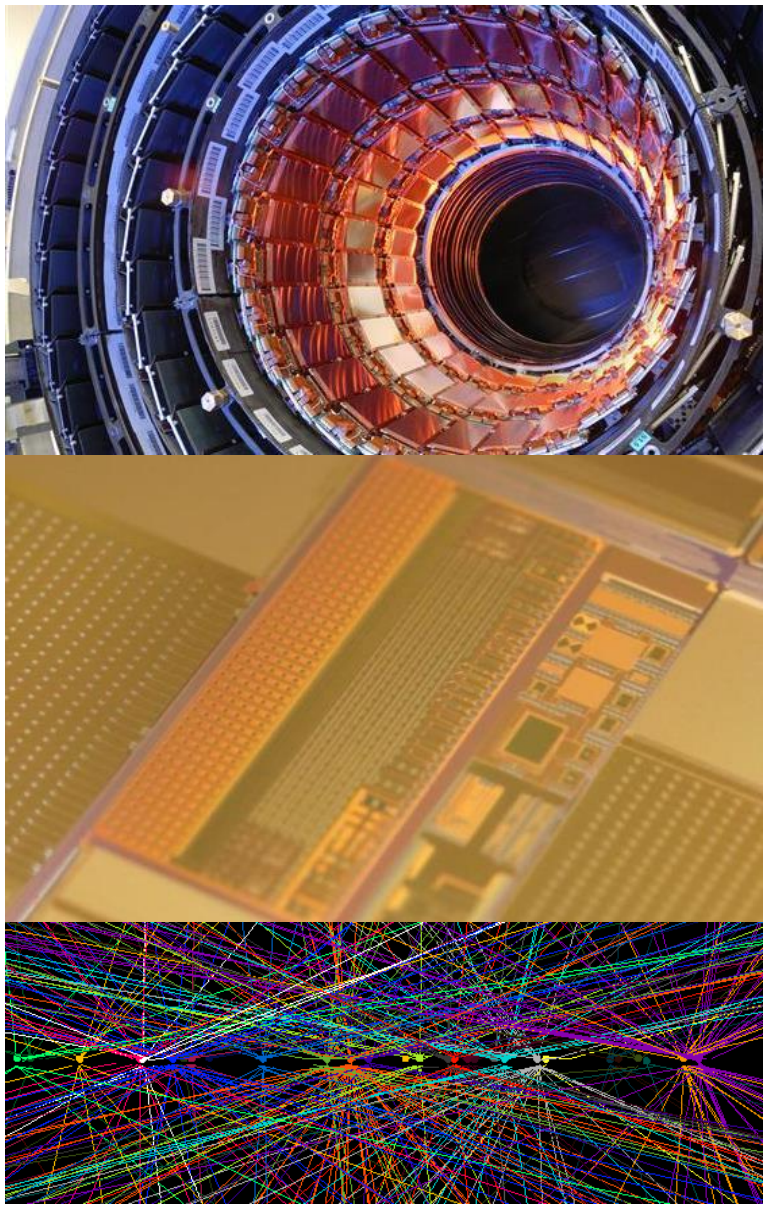
- Test the CBC3 2 chip Module
  - Verify performance when bumped
  - Verify nearest neighbour logic for Stubs
- CBC 3.1
  - Add invalid Stub rejection function
  - Add Nearest Neighbour I/O test feature for wafer testing completeness
  - Improve Triggered Data Serialiser robustness to Clock 40 DLL phase shifts
  - Improve configuration register SEU robustness (**TBC**)
- Manufacture CBC3.1
- Test CBC3.1
- Production Wafers







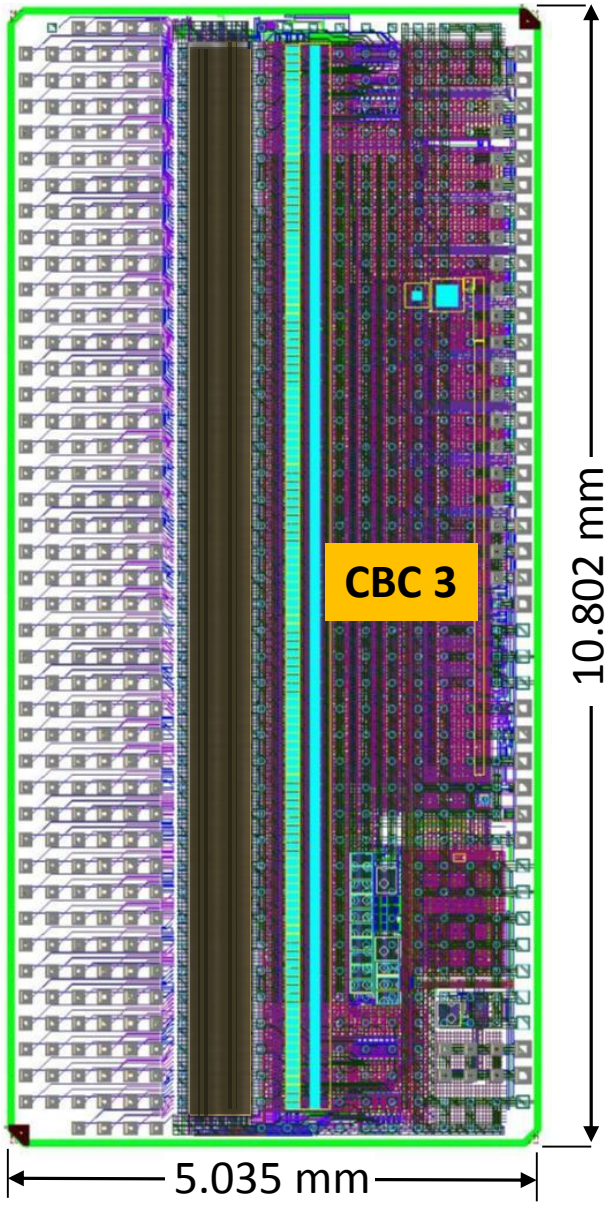
Outline



- Background
- CBC3 Features
- CBC3 Single Chip Testing
- Future work
- **Summary & Conclusion**

Summary & Conclusion

- Successful final full-size prototype of the new Outer Tracker ASIC
- CBC3 working to specification
- Re-designed Stub identification & new output data chain both functional
- Pipeline: Corrected the radiation induced effects seen on CBC2
- Improved SEU performance of configuration registers
- 8 wafers tested with 5 sent to PacTech for bumping
- Some functional modifications needed for the production version



Acknowledgements

- Thank you to all our colleagues at CERN, Bristol (UK), Gdańsk UoT (PL), KIT (DE), IPHC (FR), for their contributions