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CBC3: a CMS Micro-Strip Readout ASIC with Logic for Track-Trigger Modules at HL-LHC

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The CBC3 is the latest version of the CMS Binary Chip for readout of the outer radial region of the upgraded CMS Tracker at HL-LHC. This 254-channel, 130nm CMOS ASIC is designed to be bump-bonded to a substrate to which sensors will be wire-bonded. It will instrument double-layer 2S-modules, consisting of two overlaid silicon micro-strip sensors with aligned micro-strips. On-chip logic identifies L1 trigger primitives from high transverse-momentum tracks by selecting correlated hits in the sensors. Delivered in late 2016, the CBC3 has been under test for several months, including x-ray irradiations and SEU testing. Results and performance are reported.

Summary

The CBC3 is the latest version of the CMS Binary Chip ASIC for readout of the outer radial region of the upgraded CMS Tracker at HL-LHC. It advances the technique of identifying L1 trigger primitives ("stubs") first demonstrated by its forerunner the CBC2, and introduces many new features, such as stub bend calculation, fast data output, and e-fuses for trimming of the new band-gap and chip identification. In addition to these new features, the performance of the analogue channel has been fine-tuned and the programmable analogue biasing improved.

Designed in 130nm CMOS, the CBC3 is a 254 channel binary readout ASIC with each channel comprised of a pre-amplifier, shaper and comparator. Channel outputs are stored in a 512-deep digital pipeline to accommodate trigger latencies of up to 12.8 microseconds. In addition to doubling capacity, the CBC3 pipeline has been redesigned to eliminate radiation induced leakage effects present on the CBC2 design. The L1-triggered data from the pipeline is now combined into a serial data packet along with a 9-bit L1 count, and output at 320 Mb/s via a differential SLVS output driver to meet the requirement of a 1 MHz average trigger rate.

Like its predecessor, the CBC3 is designed to instrument double-layer 2S-modules and includes coincidence logic for identifying potential stubs, along with programmable cluster-width discrimination and programmable geometric-offset correction. The CBC3 improves on the original stub recognition logic by increasing the resolution to half-strip and providing bend information associated with the stub's direction. Additional logic is included to assign an 8-bit address to each identified stub and assemble a data packet containing up to three stub addresses per bunch-crossing, along with their corresponding 4-bit bend information and status flags. This data packet is divided into five bytes and output from the ASIC via five differential SLVS output drivers operating at 320 Mb/s, thus allowing the complete data packet to be sent in one bunch crossing.

The CBC3 retains the I2C compatible slow control interface for programming the configuration registers of biases and other functions, but adopts a 320 Mb/s serial command interface for fast commands such as the L1 Trigger. These commands are now received in the form of a serial 8-bit word via a differential SLVS input.

Whereas the CBC2 was able to operate off a single 40 MHz clock, the CBC3 required an additional 320 MHz clock domain for the fast I/O. To simplify module design, the CBC3 derives its own 40 MHz clock from a synchronisation pattern contained within the fast command-word data stream. This derived clock can be phase shifted by a programmable Delay-Locked-Loop in order to optimise timing relative to the bunch-crossing.

The CBC3 was delivered in late 2016, and wire-bonded prototypes were evaluated for performance. We will present results from electrical characterization including x-ray irradiations and SEU testing. Probe testing

of the remaining wafers was carried out before they were sent to be processed with bumps in readiness for mounting on a dual-chip hybrid.

Our plans for future developments will be outlined.

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