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Results from CHIPIX-FE0, a Small Scale Prototype of a New Generation Pixel Readout ASIC in 65nm CMOS for HL-LHC

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CHIPIX65-FE0 is a readout ASIC in CMOS 65nm designed by the CHIPIX65 project for a pixel detector at the HL-LHC, consisting of a matrix of 64x64 pixels of dimension 50x50 μm^2. It is fully functional, can work at low thresholds down to 250e$^-$ and satisfies all the specifications. Results confirm low-noise, fast performance of both the synchronous and asynchronous front-end in a complex digital chip. CHIPIX65-FE0 has been irradiated up to 600 Mrad and is only marginally affected on analog performance. Further irradiation to 1 Grad will be performed. Bump bonding to silicon sensors is now on going and detailed measurements will be presented.

Summary

The HL-LHC accelerator will constitute a new frontier for particle physics after year 2024. One major experimental challenge resides in the inner tracking detectors, measuring particle position: here the dimension of the sensitive area (pixel) has to be scaled down with respect to LHC detectors.

This paper describes the results obtained by CHIPIX65-FE0, a readout ASIC in CMOS 65nm designed by the CHIPIX65 project as small-scale demonstrator for a pixel detector at the HL-LHC. It consists of a matrix of 64x64 pixels of dimension 50x50 um2 pixels and contains several pieces that are included in RD53A, a large scale ASIC designed by the RD53 Collaboration: two out of three front-ends (a synchronous and an asynchronous architecture); several building blocks; a (4x4) pixel region digital architecture with central local buffer storage, complying with a 3 GHz/cm2 hit rate and a 1 MHz trigger rate maintaining a very high efficiency (above 99%). The chip is 100% functional, either running in triggered or trigger-less mode. All building-blocks (DAC, ADC, Band Gap, SER, sLVS-TX/RX) and very front ends are working as expected.

Analog performance shows a remarkably low ENC of 90e-, a fast-rise time below 25ns and low-power consumption (about 4µA/pixel) in both synchronous and asynchronous front-ends; a very linear behavior of CSA and discriminator. No significant cross talk from digital electronics has been measured, achieving a low threshold of 250e-. Signal digitization is obtained with a 5b-Time over Threshold technique and is shown to be fairly linear, working well either at 80 MHz or with higher frequencies of 300 MHz obtained with a tunable local oscillator.

Irradiation results up to 600 Mrad at low temperature (-20°C) show that the chip is still fully functional and analog performance is only marginally degraded. Further irradiation will be performed up to 1 Grad either at low or room temperature, to further understand the level of radiation hardness of CHIPIX65-FE0.

We are now in the process of bump bonding CHIPIX65-FE0 to 3D and possibly planar silicon sensors during spring. Detailed results will be presented in the conference paper.

Authors: PATERNO, Andrea (Universita e INFN Torino (IT)); RIVETTI, Angelo (Universita e INFN Torino (IT)); MARZOCCA, Cristoforo (Politecnico di Bari and INFN Bari); MONTEIL, Ennio (Universita e INFN Torino

(IT)); LODDO, Flavio (INFN-BARI); DE CANIO, Francesco (Universita e INFN (IT)); LICCIULLI, Francesco (Universita e INFN, Bari (IT)); TRAVERSI, Gianluca (Universita e INFN, Pavia (IT)); MAZZA, Gianni (Universita e INFN Torino (IT)); DELLACASA, Giulio (Universita e INFN Torino (IT)); MAGAZZU, Guido (INFN Sezione di Pisa, Universita' e Scuola Normale Superiore, P); DEMARIA, Lino (Universita e INFN Torino (IT)); RATTI, Lodovico (University of Pavia); PACHER, Luca (Universita e INFN Torino (IT)); GAIONI, Luigi (Universita e INFN, Pavia (IT)); DA ROCHA ROLO, Manuel Dionisio (Universita e INFN Torino (IT)); PLACIDI, Pisana; WHEADON, Richard; MARCONI, Sara (INFN and University of Perugia (IT)); MATTIAZZO, Serena (Universita e INFN, Padova (IT)); PANATI, Serena (Universita e INFN Torino (IT)); RE, Valerio (INFN)

Presenter: PACHER, Luca (Universita e INFN Torino (IT))

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