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Monolithic Pixel Development in 180 nm CMOS for the Outer Pixel Layers in the ATLAS Experiment

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The ATLAS experiment at CERN plans to upgrade its Inner Tracking system for the High-Luminosity LHC in 2026. After the ALPIDE monolithic sensor for the ALICE ITS was successfully implemented a 180nm CMOS Imaging Sensor technology, the process was modified to combine full sensor depletion with a low sensor capacitance (˜2.5fF), for increased radiation tolerance and low analog power consumption. Efficiency and charge collection time were measured with comparisons before and after irradiation. An overview of the measurements and the ATLAS-specific development towards full-reticle size CMOS sensors and modules in this modified technology will be given

Summary

The Inner Tracking system (ITk) of the ATLAS detector [1] will be upgraded in 2026 for the High-Luminosity Large Hadron Collider. The present ITk pixel detector is based on hybrid sensors. Monolithic active pixel sensors (MAPS) can be produced in commercial CMOS technology and offer higher resolution and lower material in the vertex detector.

ALICE is the first experiment at the LHC implementing a large silicon tracker with MAPS. The ALPIDE monolithic sensor implemented in a 180 nm CMOS Imaging Sensor technology [2] features a high resistivity epilayer ($>$1 kΩ·cm) with possibility to apply reverse bias (-6V). However, the sensor depletion volume is limited to the region around the collection electrode and signal charge generated outside the depleted area is still collected primarily by diffusion. The required tolerance to non-ionizing energy loss (NIEL) in the outer ATLAS pixel layers is 1.5×10^{15}1 MeV n_{eq}/cm^2, two orders of magnitude higher than the ALICE ITS. This requires a drift field and hence depletion over the full sensitive layer to reduce charge carriers collection time and reduce the probability of charge trapping signal loss. Moreover, a short charge collection time, combined with a fast front-end, is fundamental to separate hits from consecutive bunch crossings (25 ns).

For use in high radiation environments like the ATLAS ITk, a process modification in this technology developed in collaboration with the foundry [3] creates a deep planar junction to obtain full depletion of the epitaxial layer and charge collection by drift, while maintaining a small collection electrode with a small sensing node capacitance ($\approx$ 2.5 fF) essential for a low power pixel design. The process modification has been tested with the Investigator pixel chip [4], a sensor characterization device designed in the framework of the monolithic sensor development for ALICE ITS. It implements different pixel geometries giving direct access to the sensing node transient voltage to study signal collection characteristics and detection efficiency. ^{90}Sr source measurements show charge collection is virtually unaffected by non-ionizing energy loss up to 10^{15} 1 MeV n_{eq}/cm^2. Beam test measurements show no efficiency loss after irradiation.

This opened the way to the design of two large scale demonstrators for the ATLAS ITk outermost pixel layers, where the expected hit rate is 0.4 to 2 MHz/mm^2. MALTA contains a 512$\times$512 pixel matrix of 36.4 μm pitch featuring a 1 μW frontend with in-pixel discrimination based on ALPIDE [5] with a time response $<$ 20ns. The full asynchronous readout without clock distribution over the matrix reduces digital power. TJ-Monopix implements the same front-end as MALTA combining it with the well-established column drain architecture [6]. Charge collection and test beam results and an outlook on the chip development will be presented.
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