FE65-P2:
A Prototype Pixel Readout Chip in 65nm Technology for HL-LHC Upgrades

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Santa Cruz

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Tracker at the HL-LHC

What does the high luminosity upgrade of the LHC mean for the tracker?

LHC → Summer Rain

HL-LHC → Pouring Storm

- Store full time sequence of drops until trigger (not collect in a bucket) → more memory
- High resolution to distinguish between drops → smaller pixels
- Drops damage sensor and readout chip → higher radiation tolerance

RD53 Collaboration

	RD53	Current Tracker
Chip Size	2x2 cm^2	2x2cm^2
Pixel Size	50x50 μm^2	50x250 μm^2
Pixel Hit Rate	3 GHz/cm^2	400 MHz/cm^2
Trigger rate	1 MHz	200 kHz
Trigger Latency	12.8 µs	6.4 µs
Current consumption	<8 µA/pixel	20 µA/pixel
Radiation Tolerance	0.5-1 Grad	300 Mrad
Min. stable Threshold	600 e	1500 e

Where does FE65-P2 fit in:

- Designed in context of the RD53 collaboration
- One of two test vehicles to pave the way to RD53A (see other being CHIPIX 65)
- Submitted Fall 2015 to get test results in time for RD53A design

RD53 at TWEPP 2017

Other RD53 related presentations/posters at TWEPP 2017:

- SEU Tolerant Latches Study for the RD53A Chip - Denis Fougeron
- Development of a Large Pixel Chip Demonstrator in RD53 for ATLAS and CMS Pixel Upgrades - Elia Conti
- Characterization and Verification Environment for the 65 nm Pixel Readout-Chip RD53A - Marco Vogt
- Serial Powering Optimization for CMS and ATLAS Pixel Detectors within RD53 Collaboration for HL-LHC: System Level Simulations and Testing - Stella Orfanelli
- Results from CHIPIX-FE0, a Small Scale Prototype of a New Generation Pixel Readout ASIC in 65nm CMOS for HL-LHC - Luca Pacher
- Characterization of SLVS Driver and Receiver in a 65 nm CMOS Technology for High Energy Physics Applications - Francesco De Canio
- Design and Test of a 65nm CMOS Front-End with Zero Dead Time for Next Generation Pixel Detectors - Davide Braga

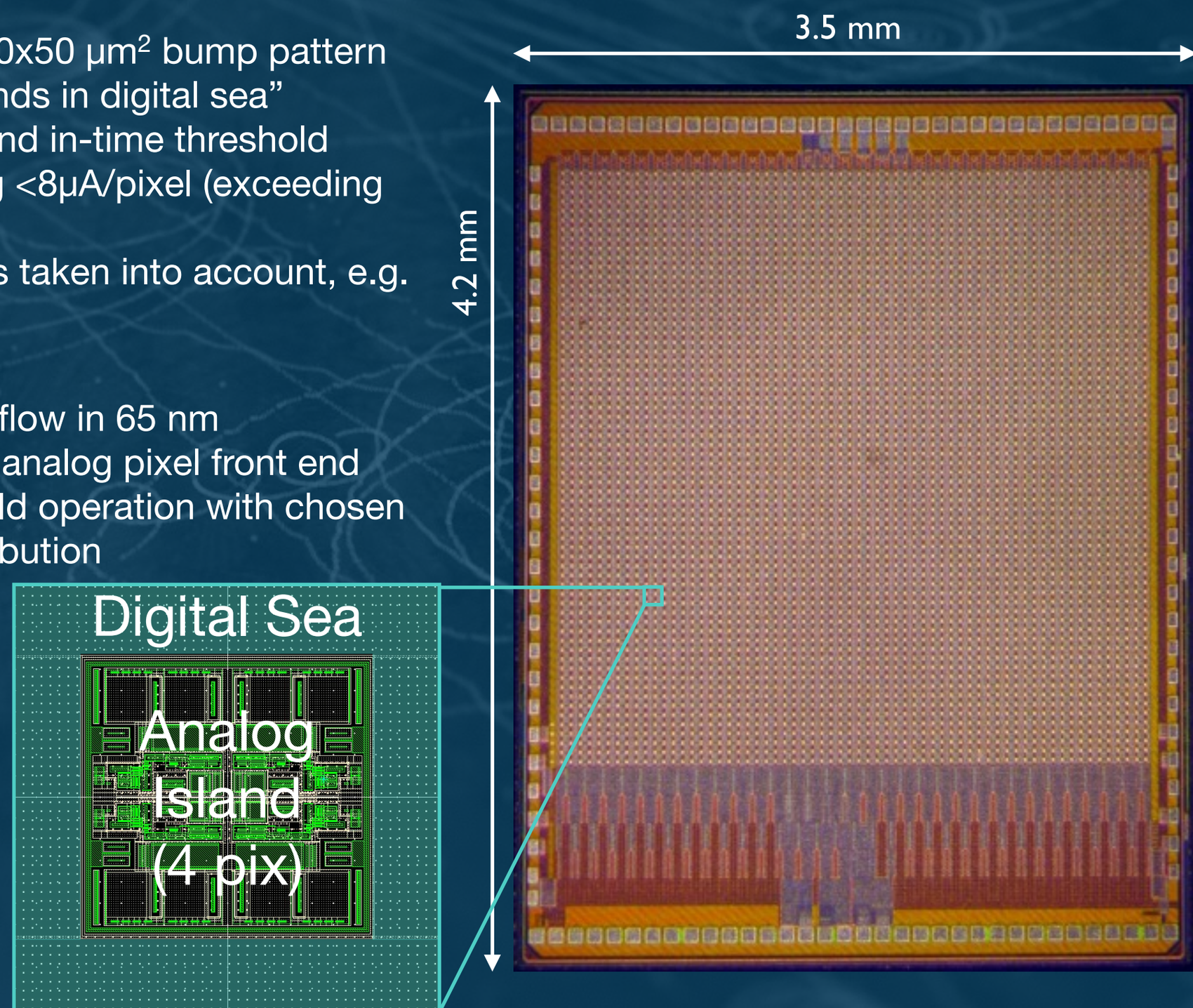
FE65-P2 Overview

Specifications:

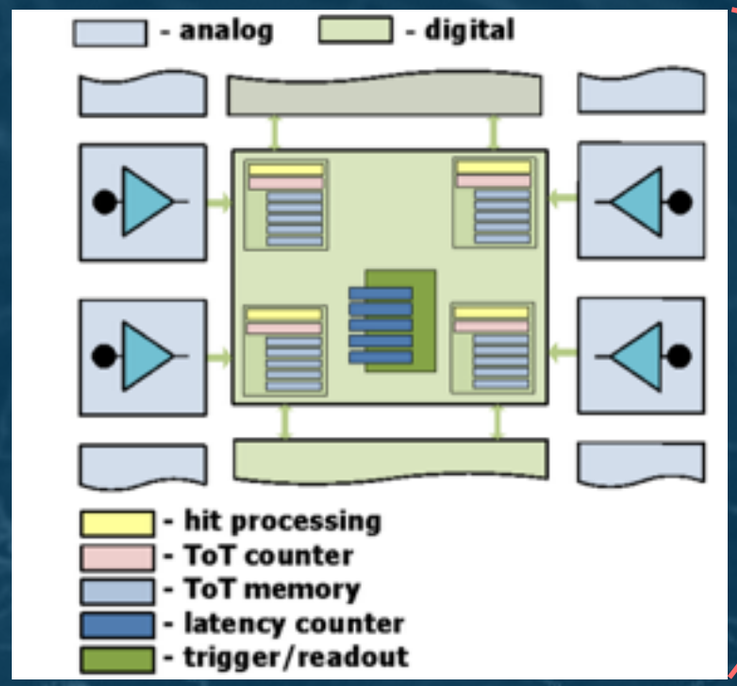
- 65 nm design
- 64x64 pixel matrix with 50x50 μm^2 bump pattern
- Designed as “analog islands in digital sea”
- Stable threshold <500e and in-time threshold <1000e, while consuming <8μA/pixel (exceeding RD53A spec)
- Large chip considerations taken into account, e.g. power distribution

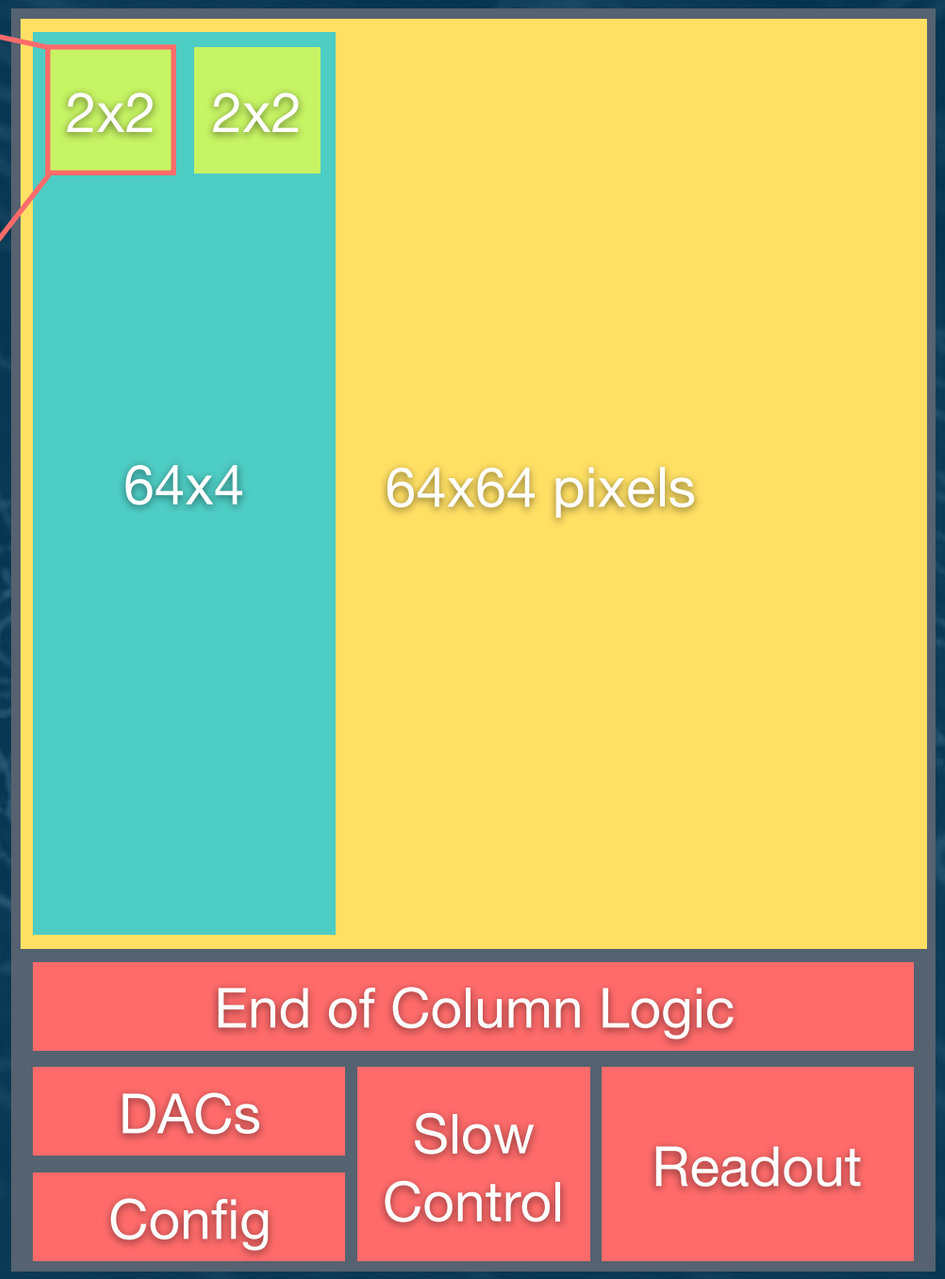
Goals:

- Exercise and test design flow in 65 nm
- Test prototype version of analog pixel front end
- Demonstrate low threshold operation with chosen isolation and power distribution
- Use for sensor testing
- Test radiation hardness



Digital Design





not to scale

Details presented at
FEE 2016 by T. Hemperek

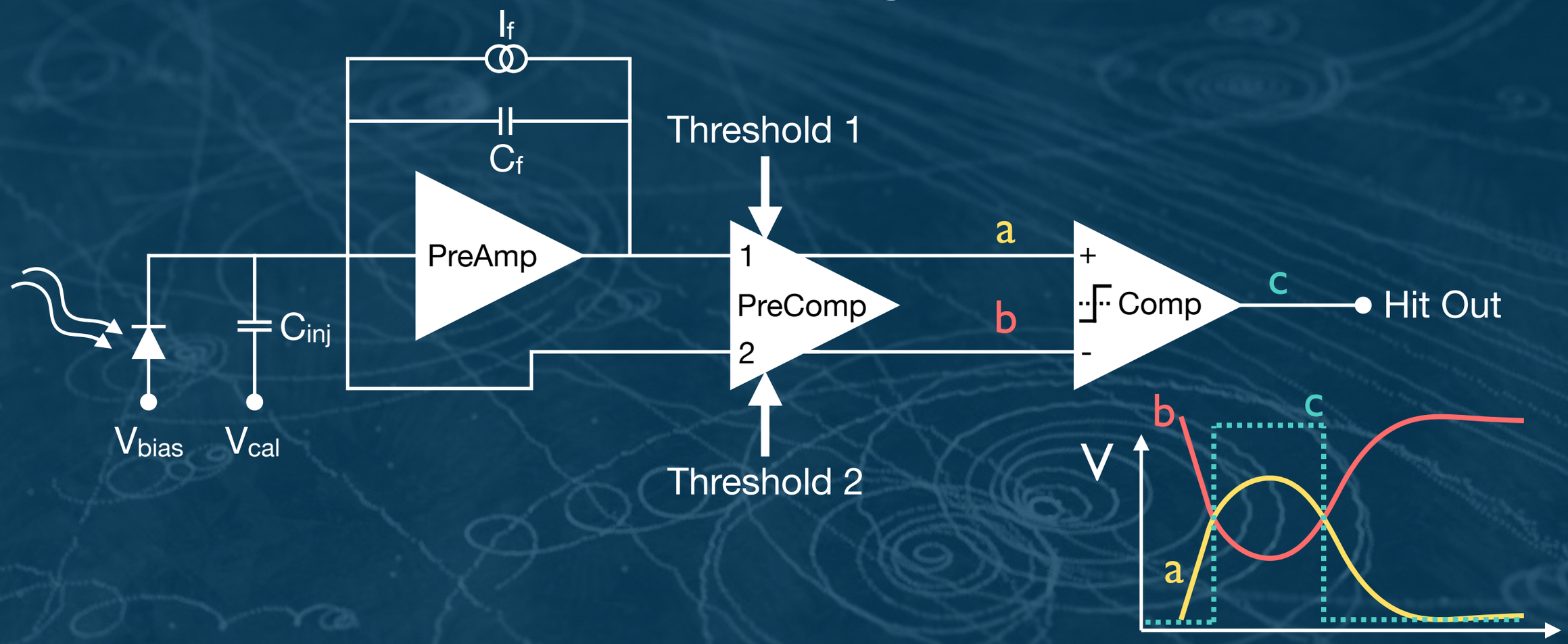
Matrix Layout:

- 64x4 pixel matrix organised in “flat” synthesised quad columns → no step & repeat
- Total of 16 quad columns in step & repeat process
- 2x2 pixel share digital region (Distributed Buffer Architecture)
- 4bit ToT counter, 7 memory locations
- 9bit BCId memory (2x9bit gray counter distributed)

Peripheral Logic:

- End-of-Column logic with token based trigger system
- Serial programming interface to access global and pixel register
- Up to 320 Mb/s 8b10b encoded readout

Analog Front-End



Preamplifier:

- Straight cascode design
- Global settings for I_f (8bit DAC)
- Preamp bias, follower and feedback current
- Leakage current compensation (not shown)
- No per pixel adjustment

Two Stage Comparator:

- Differential design
- Threshold adjustable for each input with global 8bit DAC and two per pixel 4bit DACs**
- Optimised for low threshold operation

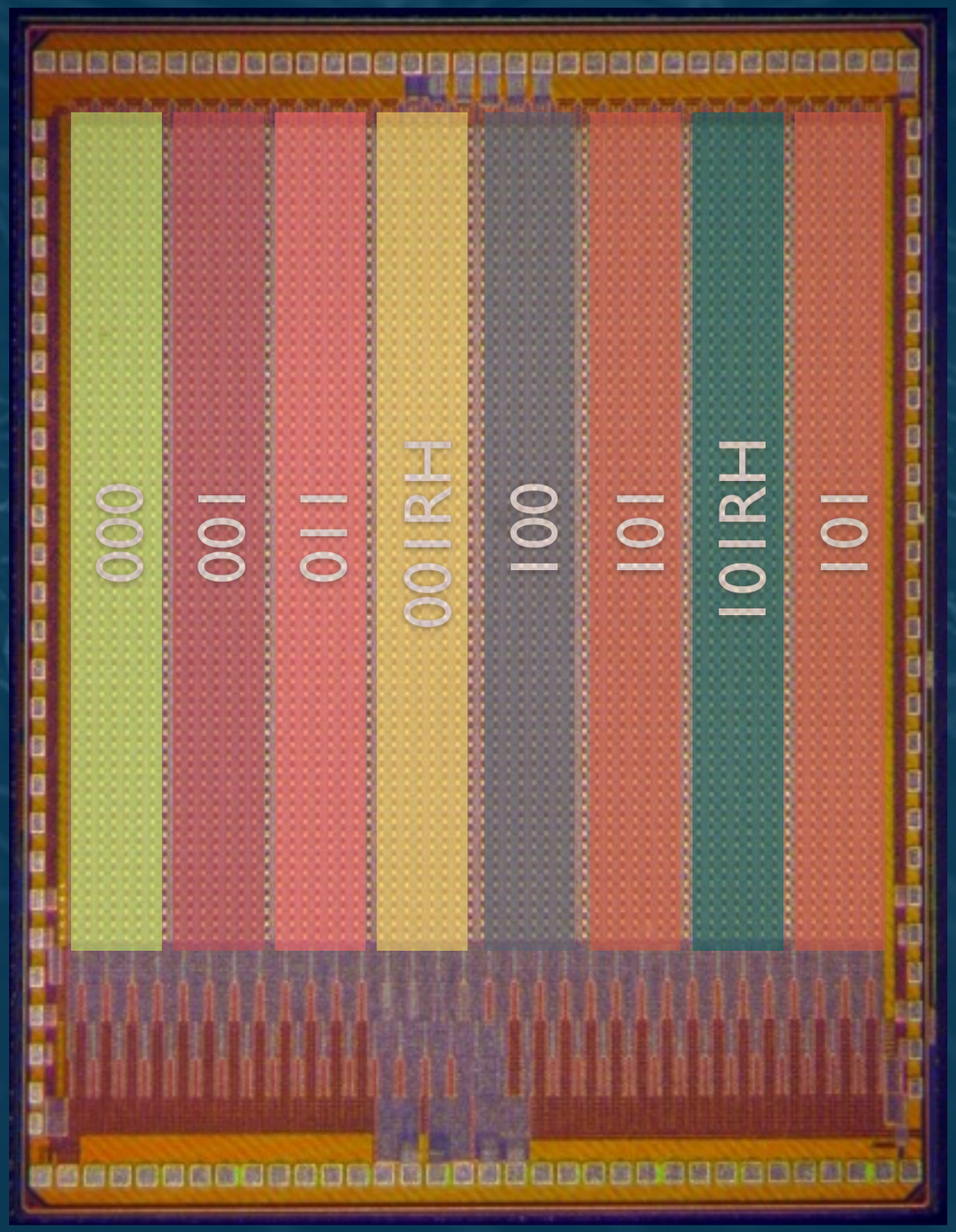
**accessible as one 5bit DAC

Analog Versions

Versions:

- Two types of Cf0/Cf1 (switchable)
- One region with power down functionality
- Two different “rad-hard” regions
- For each feedback pair one region w/o leakage current compensation

Version	Column	CF0/CF1 (fF)	Power Down	Leakage Comp	W of amp2 load PMOS
"000"	1 to 8	3.36/4.99	NO	NO	0.2u
"001"	9 to 16	3.36/4.99	NO	YES	0.2u
"011"	17 to 24	3.36/4.99	YES	YES	0.2u
"001RH"	25 to 32	3.36/4.99	NO	YES	0.48u
"100"	33 to 40	5.15/7.76	NO	NO	0.2u
"101"	41 to 48	5.15/7.76	NO	YES	0.2u
"101RH"	49 to 56	5.15/7.76	NO	YES	0.48u
"101"	57 to 64	5.15/7.76	NO	YES	0.2u



DAQ

USBPIX:

- FPGA based Multi-IO board connected via USB to PC
- General Purpose Analog Card (GPAC)
- Python based readout software
- Software and firmware fully integrated into chip simulation (cocoTB)

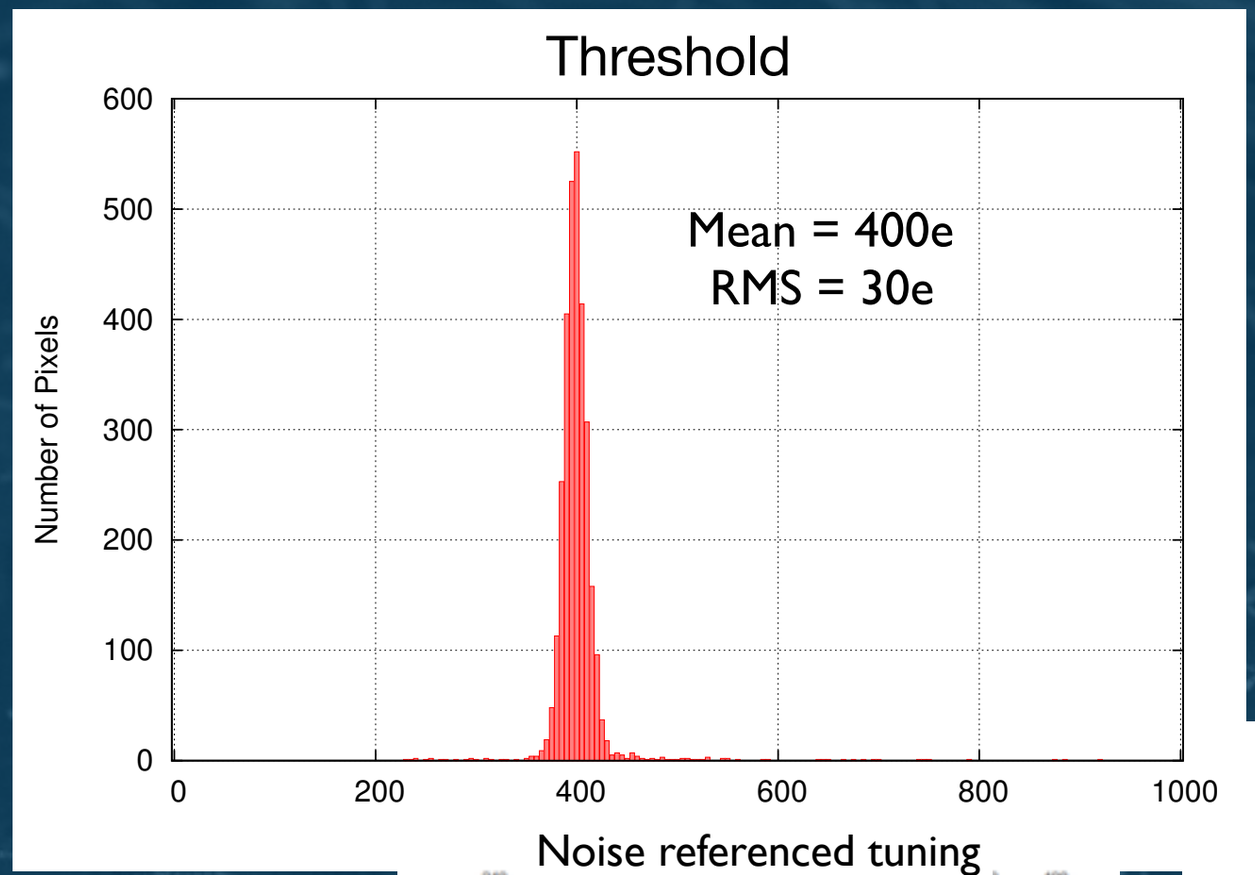
more details in Marco's talk

YARR:

- COTS PCIe FPGA cards (SPEC & XpressK7)
- Purpose build adapter card interfaced via VHDCI connector
- C++ based readout software

more details on Nikola's poster

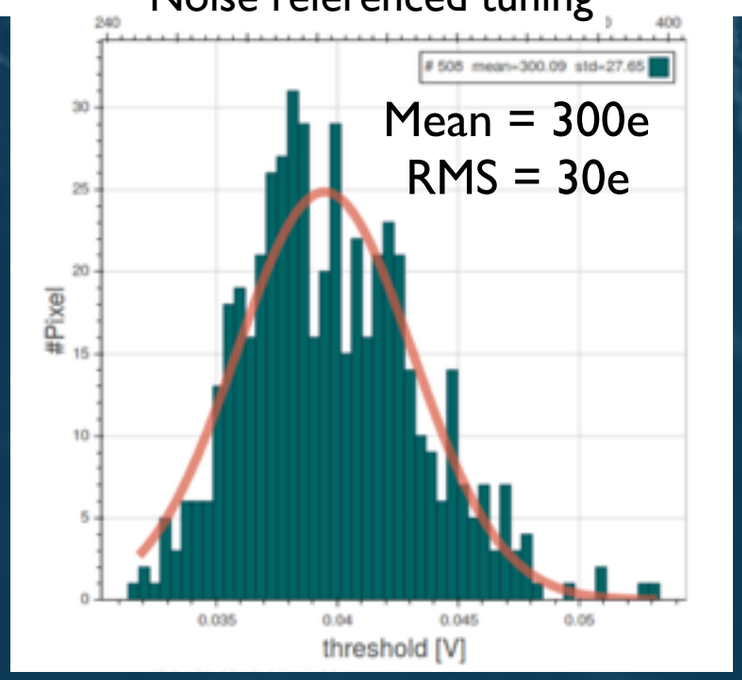
Threshold Performance

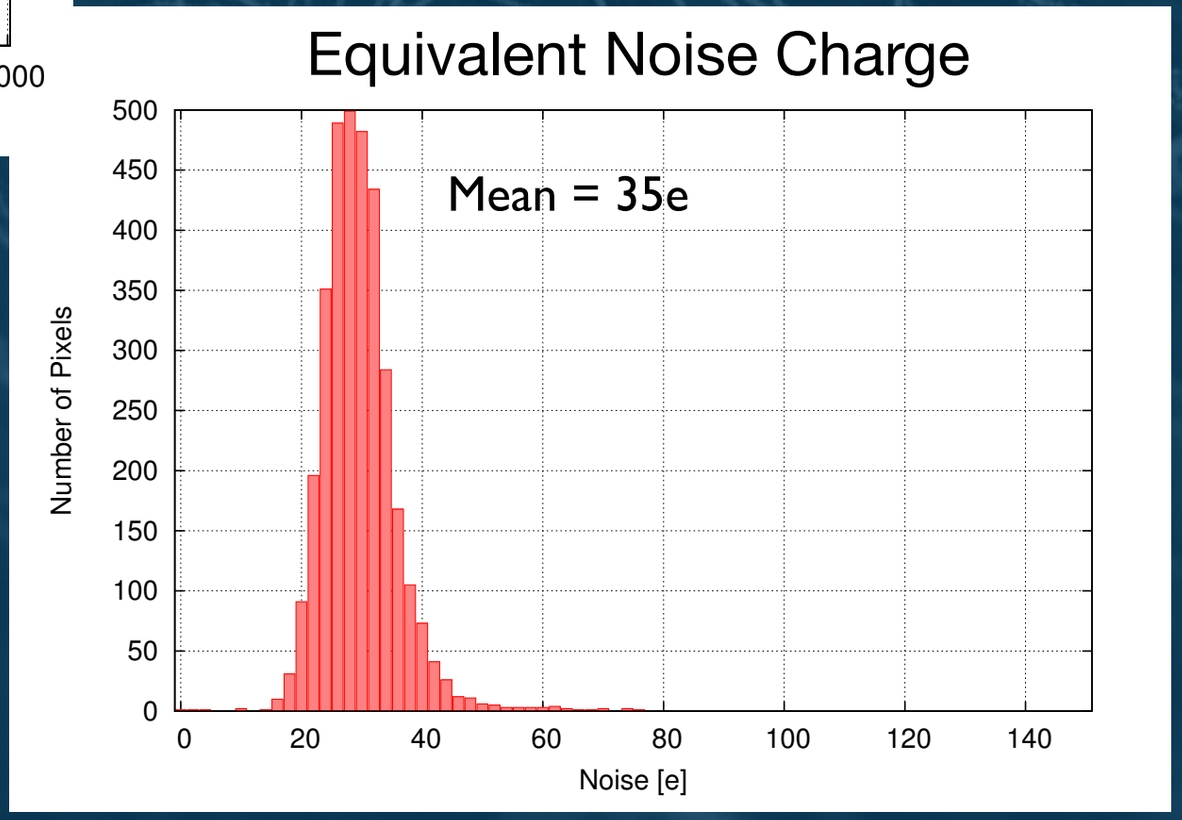


Threshold & Noise:

- 400e threshold with traditional tuning
- 300e with noise based tuning
- 30e threshold dispersion
- Average of 35e noise

Noise referenced tuning





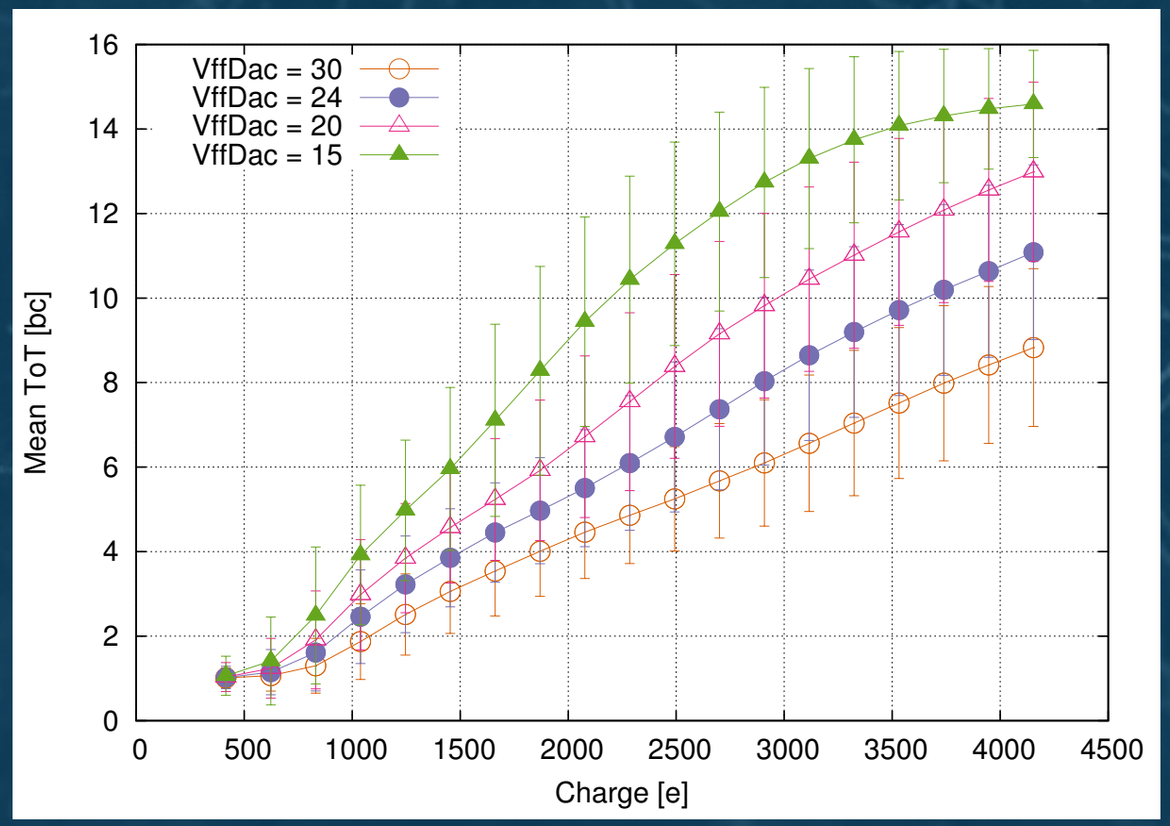
related poster showing self tuning pixels

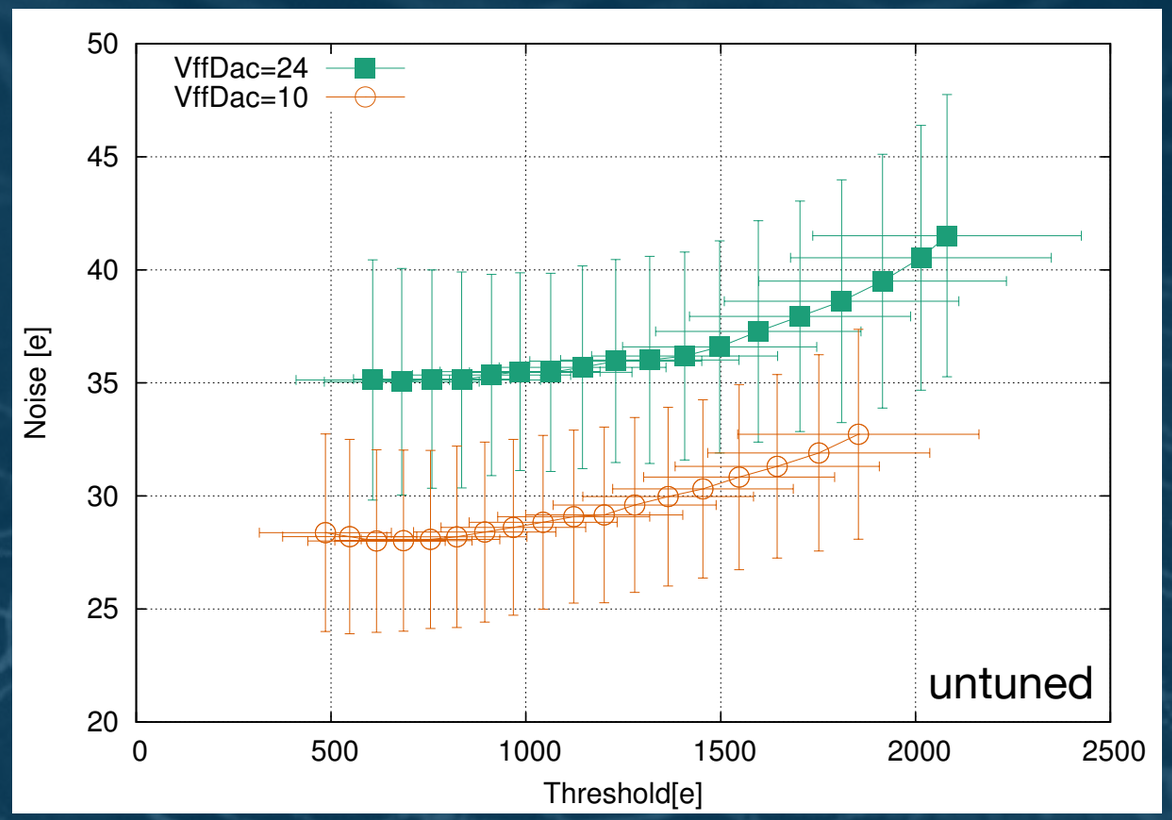
non irrad
no sensor

Threshold Performance II

Optimisation:

- Analog Front-End optimised for low threshold operation
- Noise increase with higher threshold





Feedback current:

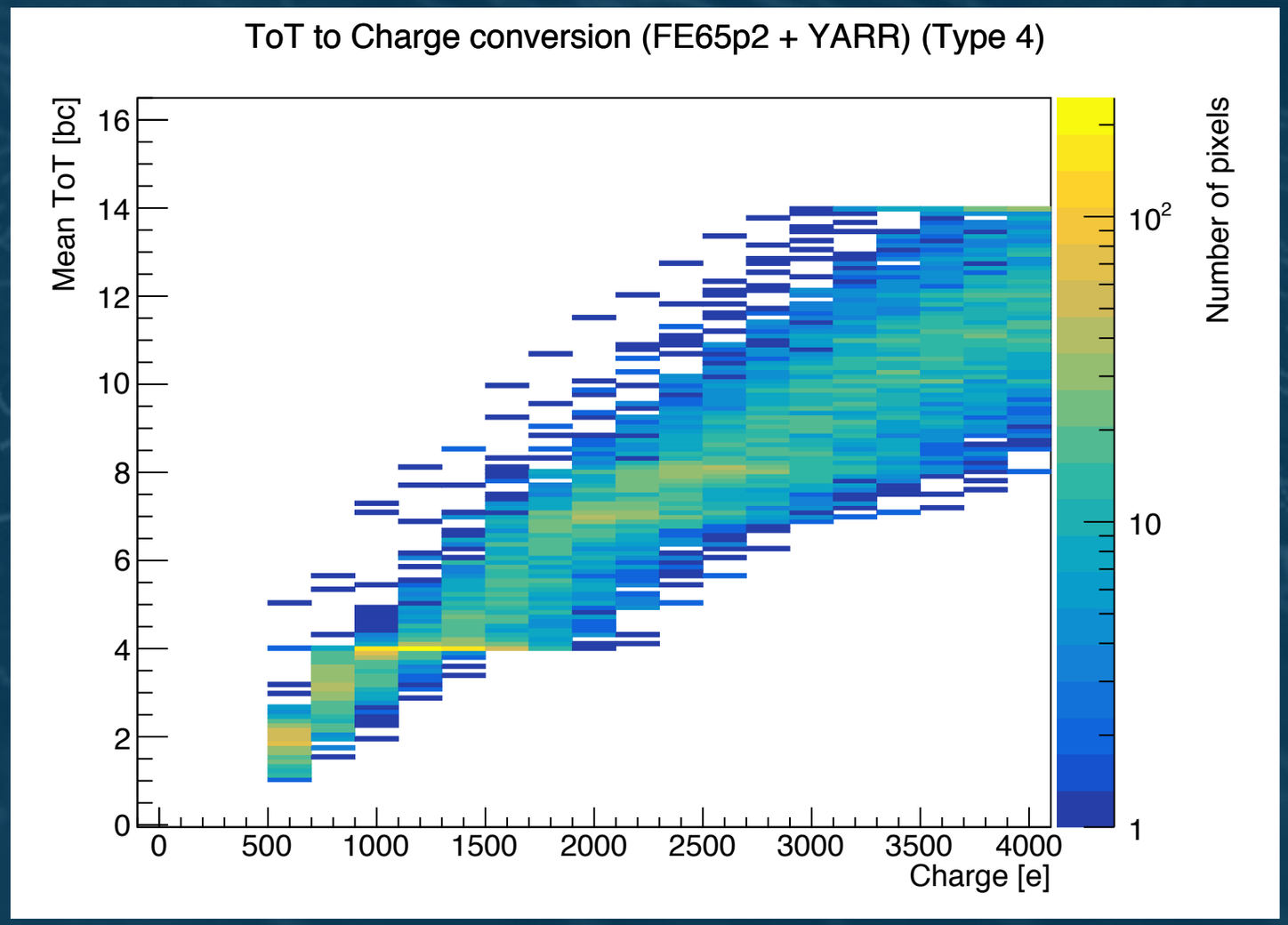
- Controlled via VffDAC
- Controls return-to-baseline
- Higher feedback current results in higher noise
- Higher feedback current needed to avoid in-pixel pile-up

non irrad
no sensor

Charge Conversion

ToT:

- No per-pixel adjustment
- Dispersion due to slow falling edge
- Dispersion deemed to be acceptable for detector operation (e.g. can be compensated via offline calibration)

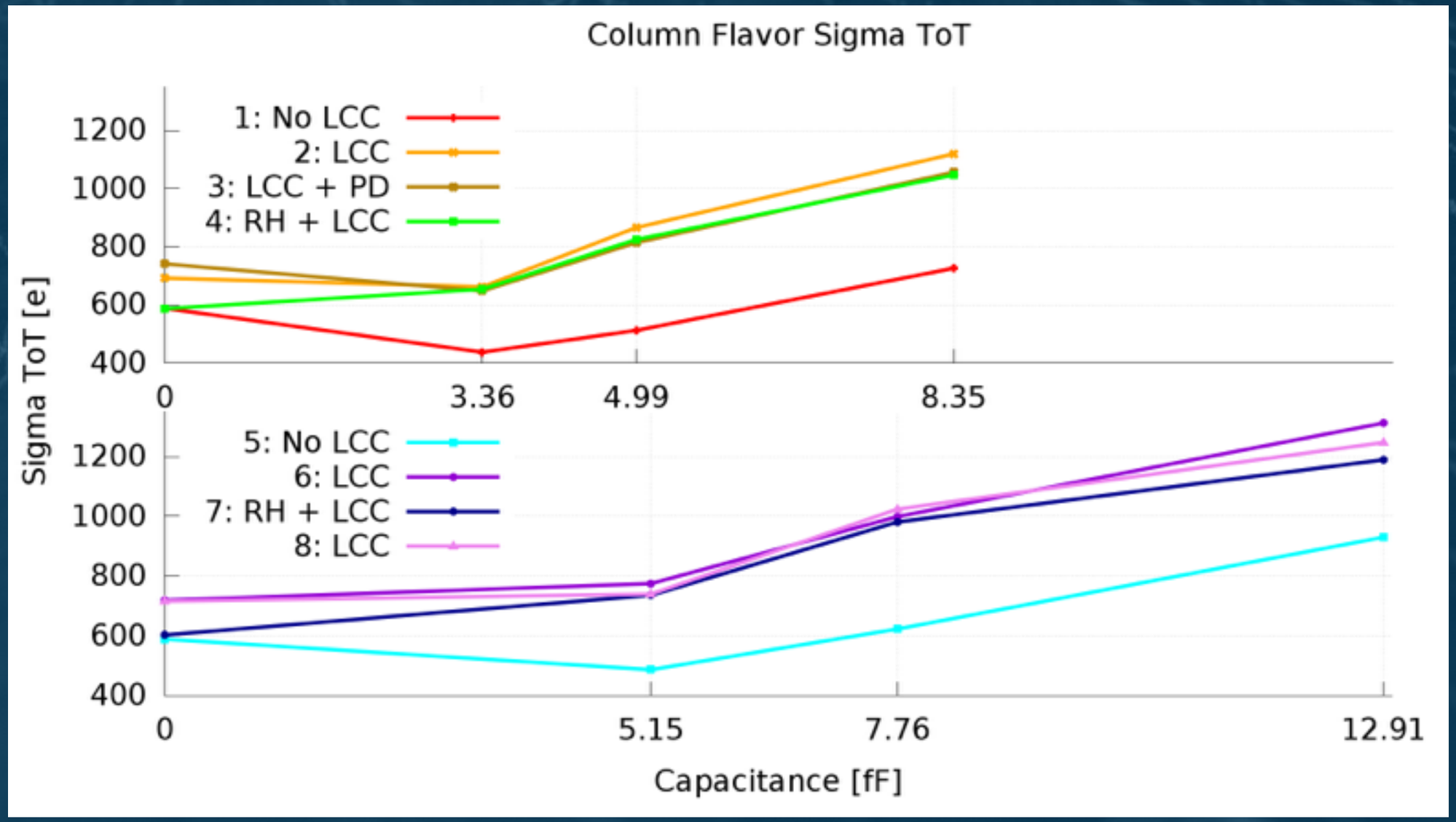


non irrad
no sensor

Gain Settings

Switchable Feedback Capacitance:

- Testing if higher feedback capacitance helps with ToT dispersion (highest gain should be best, but based on parasitic capacitance)
- Observing no change or minor improvement when enabling smallest feedback capacitance
- Keeping the option for RD53A to switch in small feedback capacitance

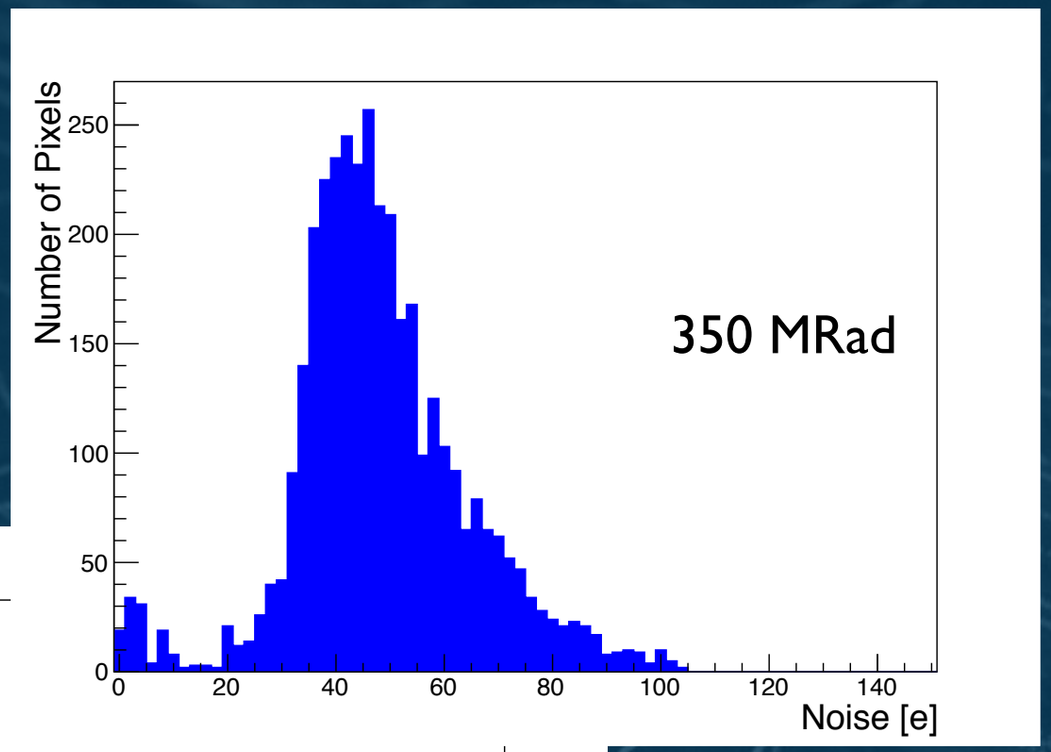


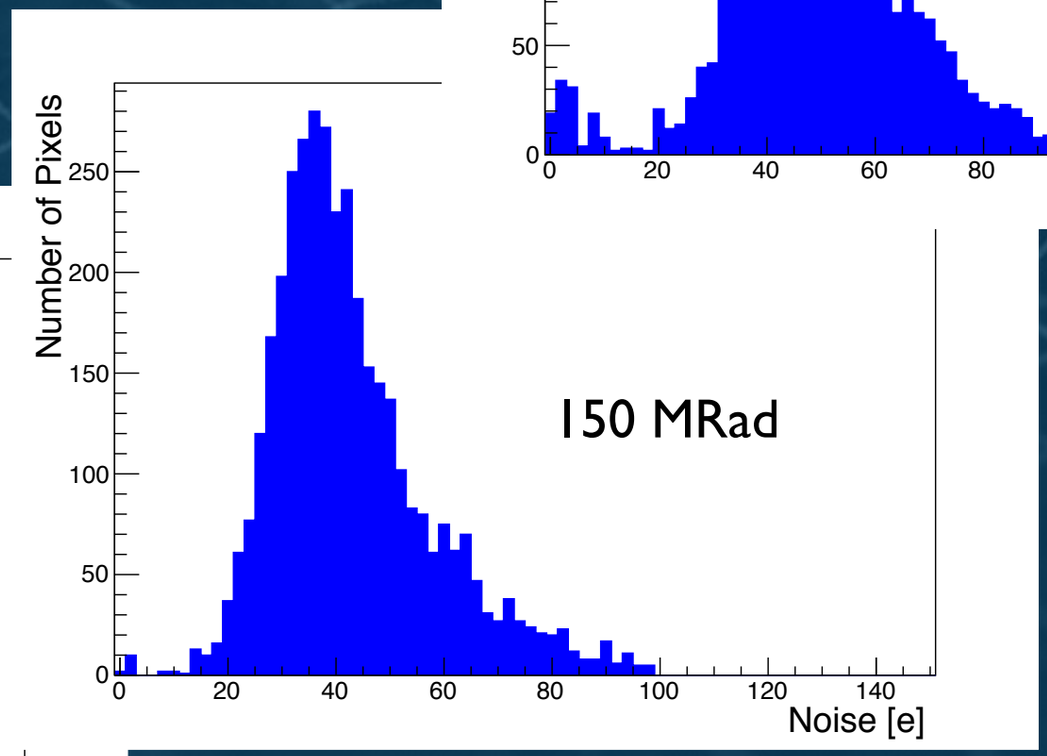
non irrad
no sensor

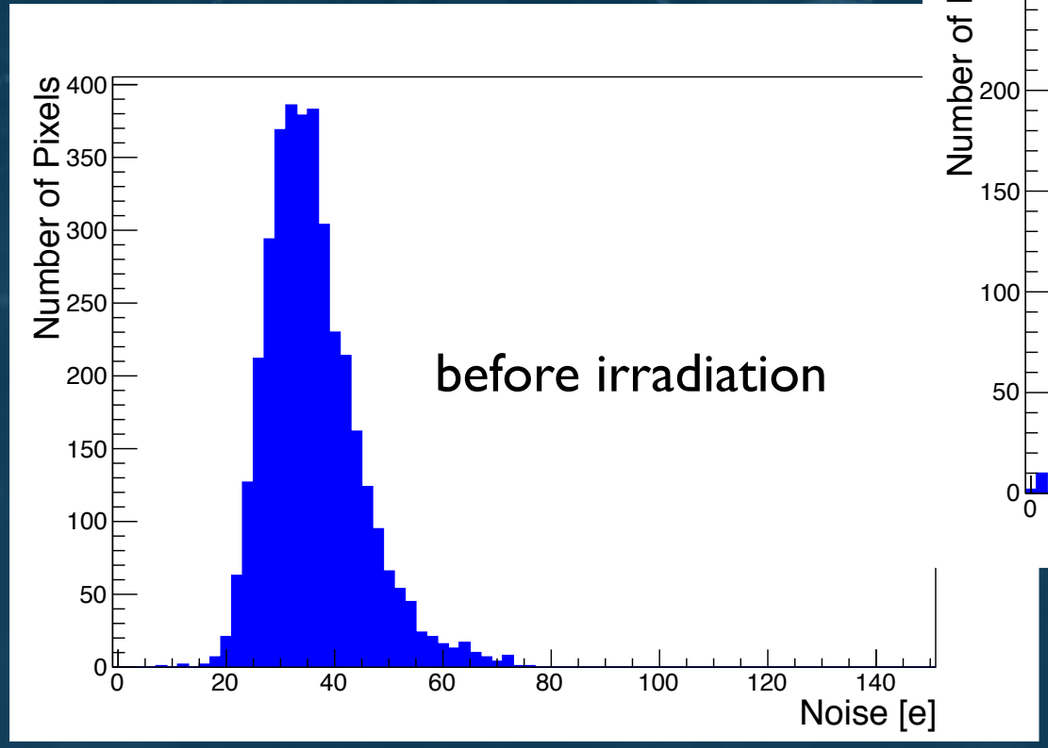
FE65P2 Irradiation

Proton irradiation:

- 800MeV protons at LANL
- Irradiated total of 6 modules
- Two chips for each TID: 150MRad, 350MRad, and 500MRad
- Unfortunately one 500MRad chip died of ESD before irrad., and the other was not centred in the beam



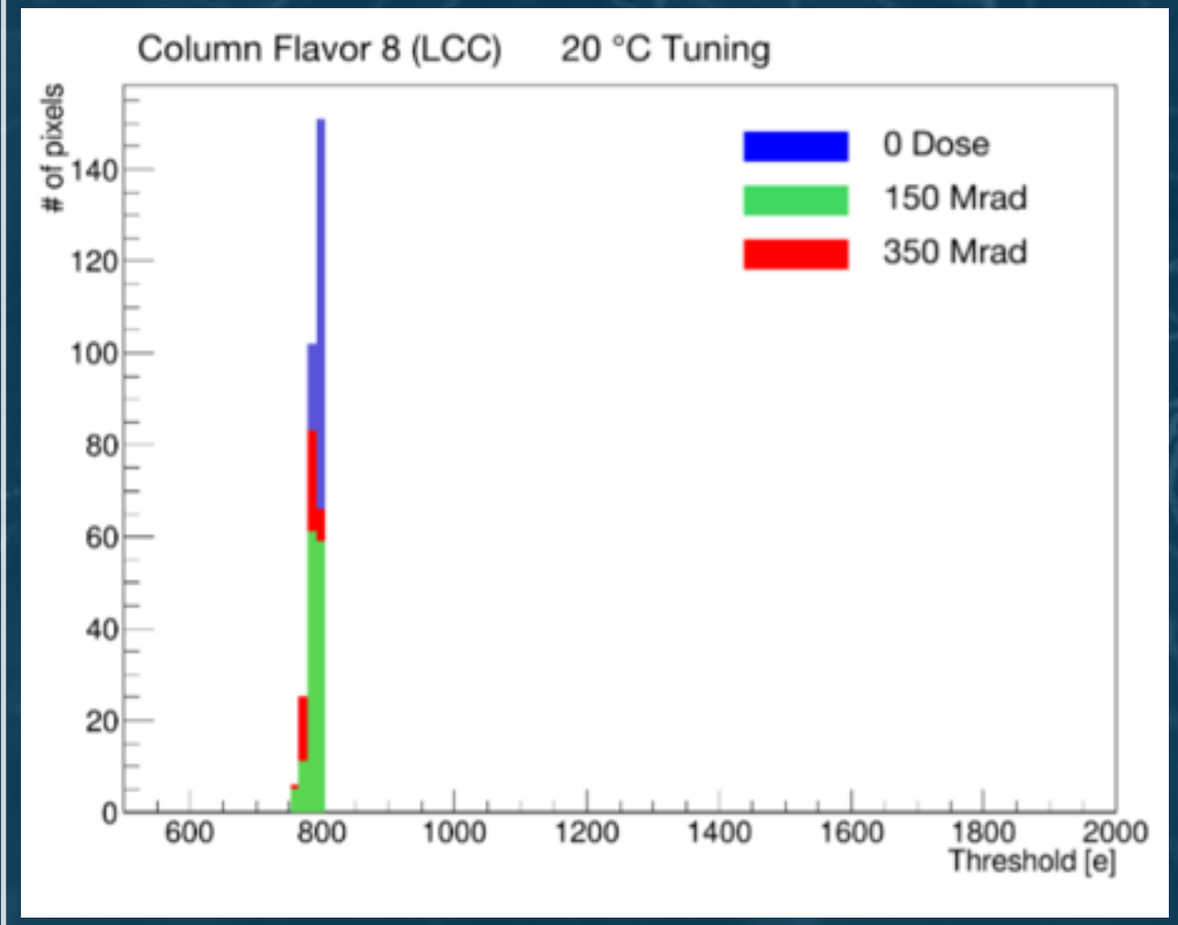


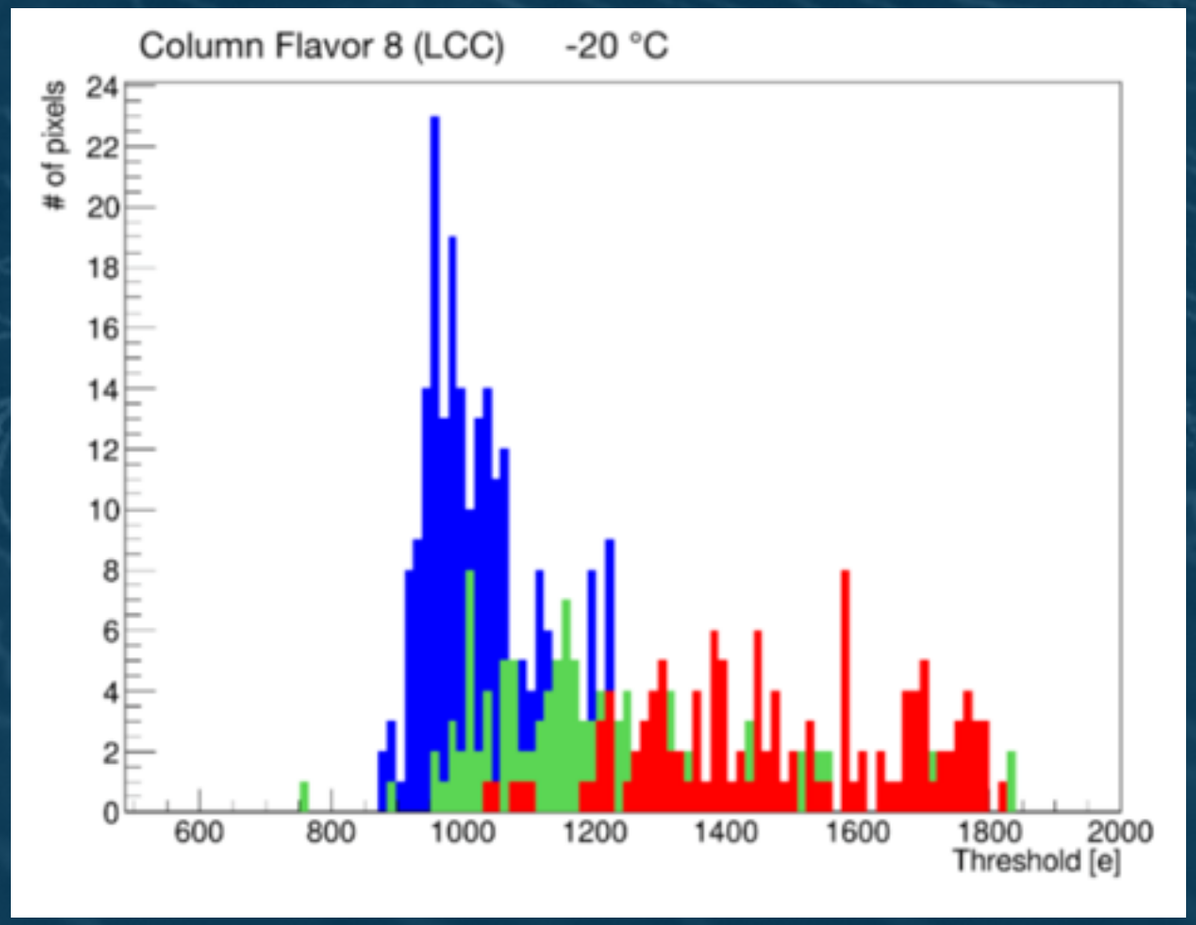


no sensor

Threshold Stability: Temperature

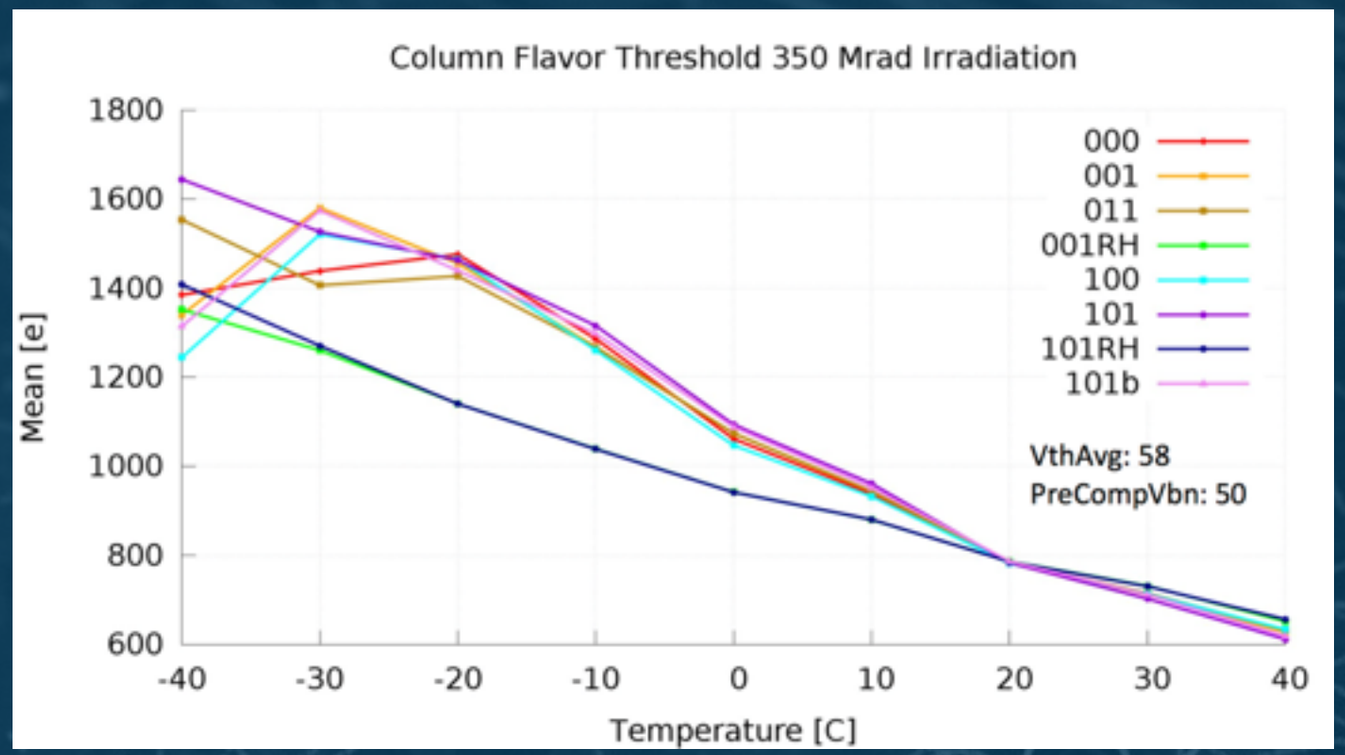
ΔT=40˚C

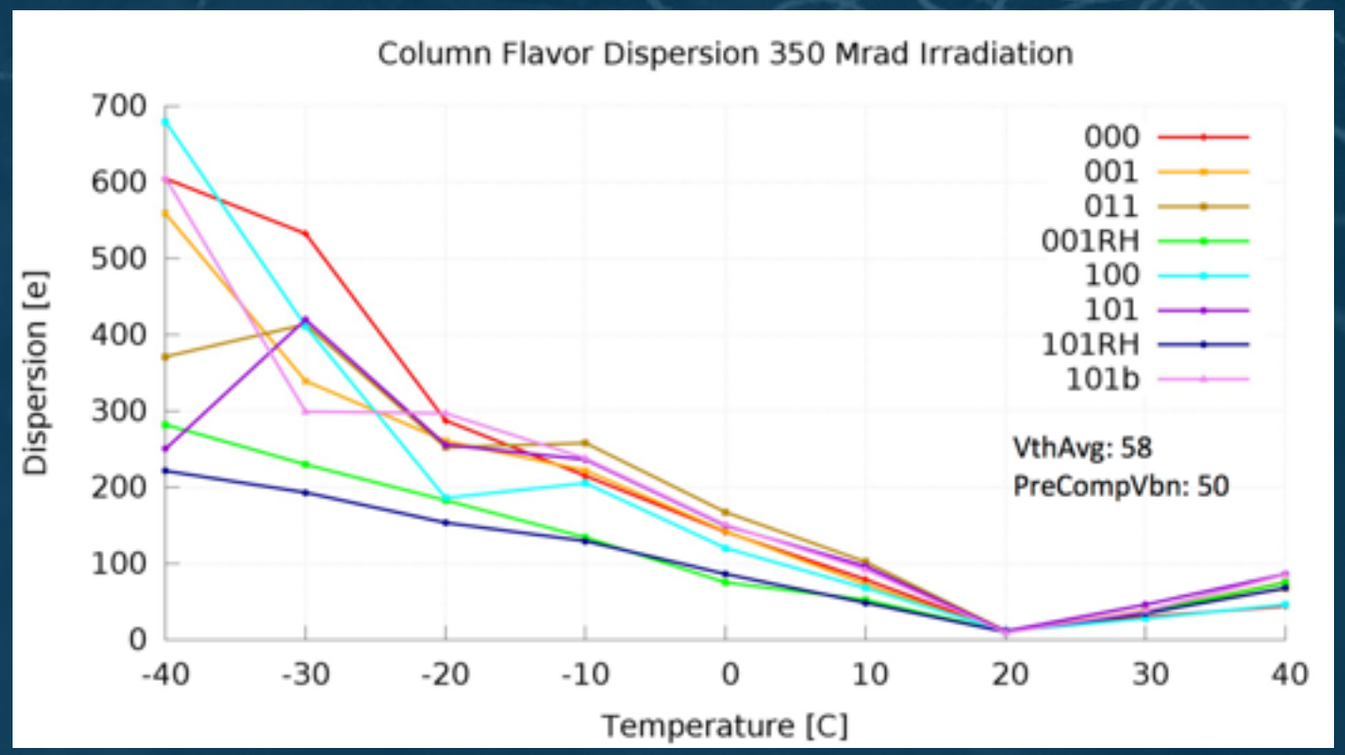




no sensor

Threshold Stability: Temperature



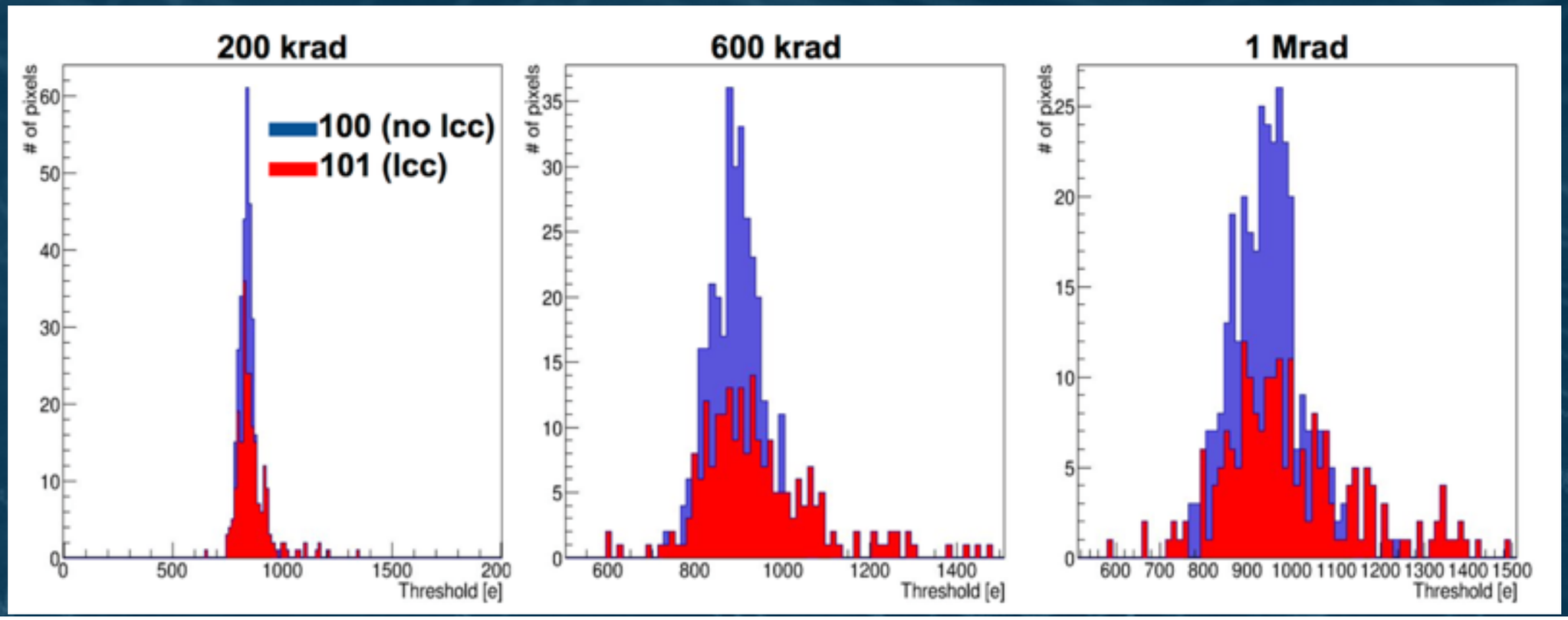


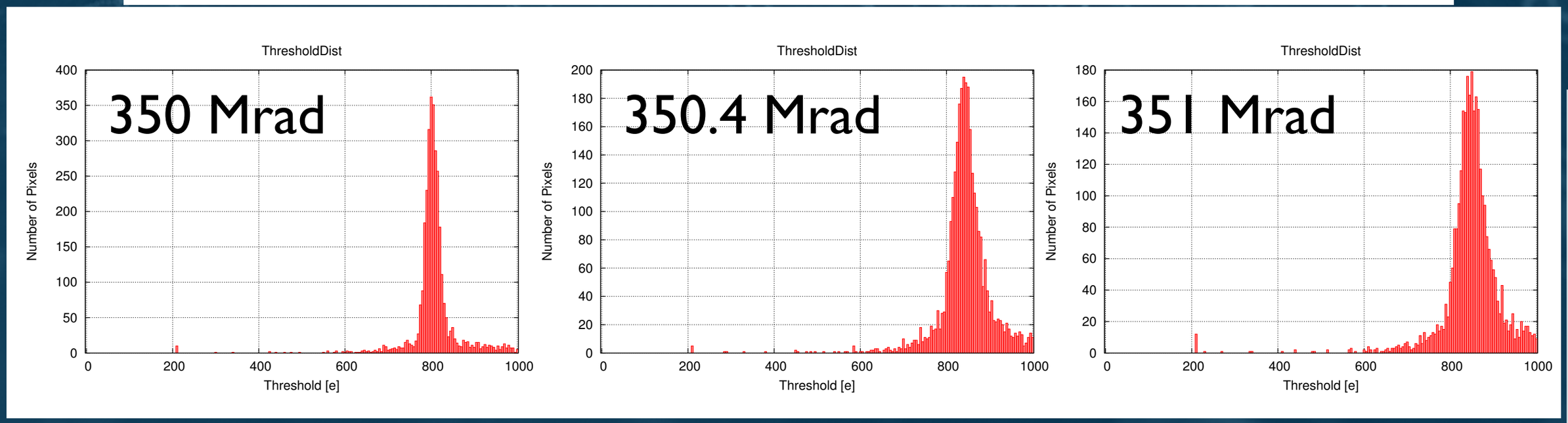
Results:

- Temperature shift in all versions non negligible
- “Rad hard” columns give best results
- Not nice, but acceptable for operation (temp. should not change)

no sensor

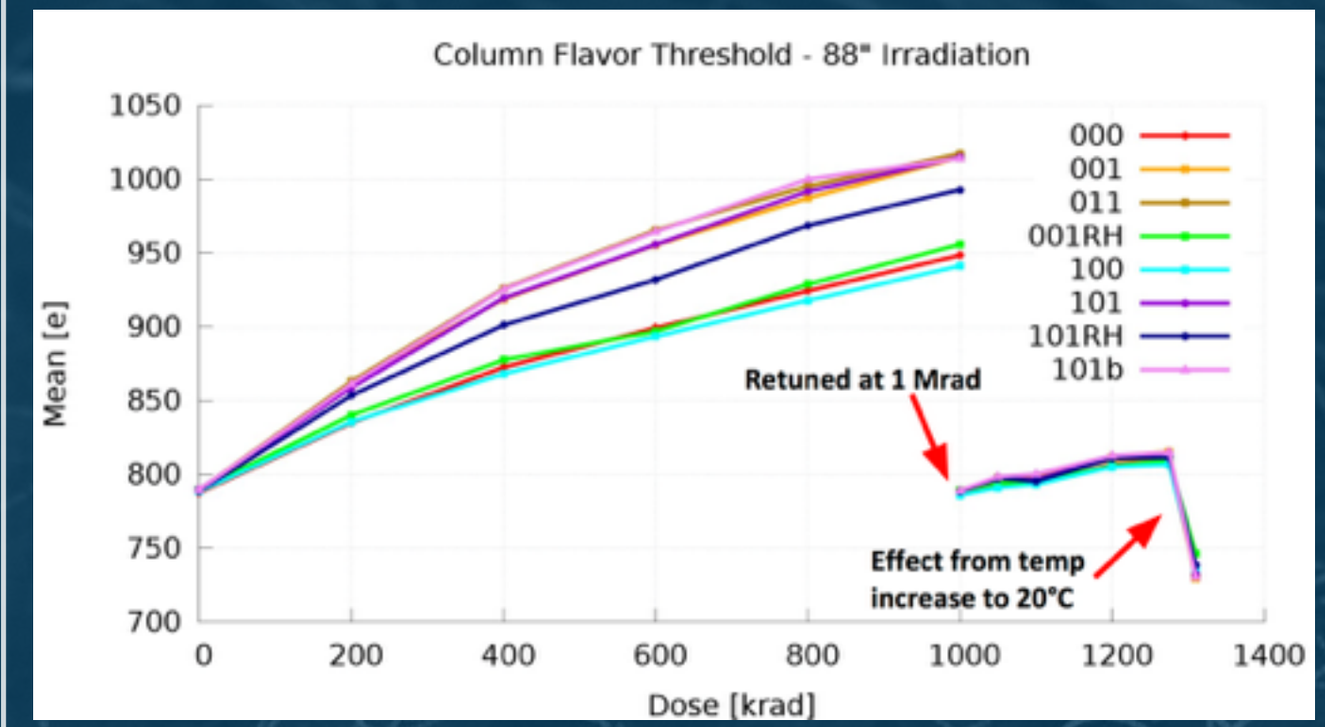
Threshold Stability: Radiation

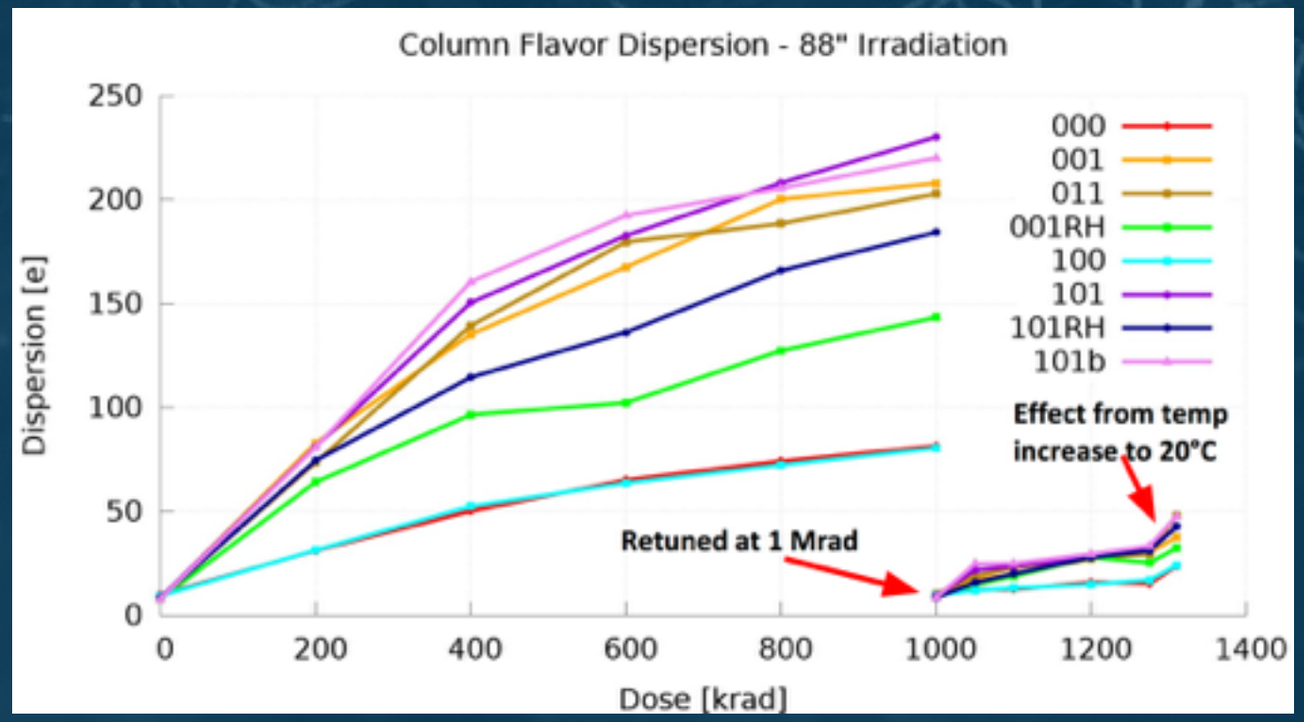




no sensor

Threshold Stability: Radiation





Results:

- Shift during early irradiation non negligible and not optimal (~1Mrad = one HL-LHC run)
- Only affected during early stage irradiation, 150 Mrad does not show a significant shift

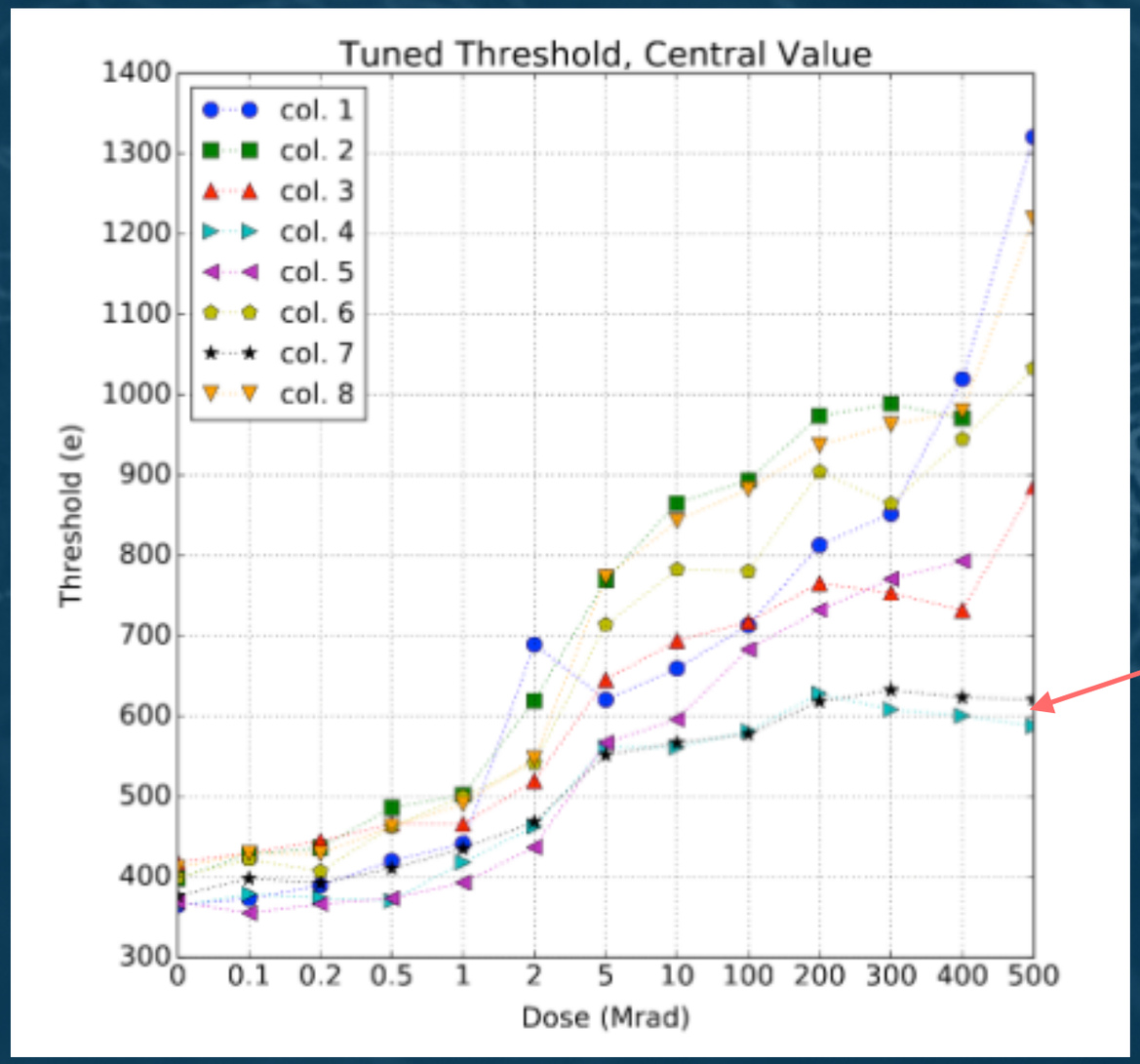
Further details in PoS ICHEP2016 (2016) 272

no sensor

FE65P2 Irradiation II

X-ray irradiation:

- Continuous monitoring during irradiation
- “Rad-hard” analog front-end behaves the best

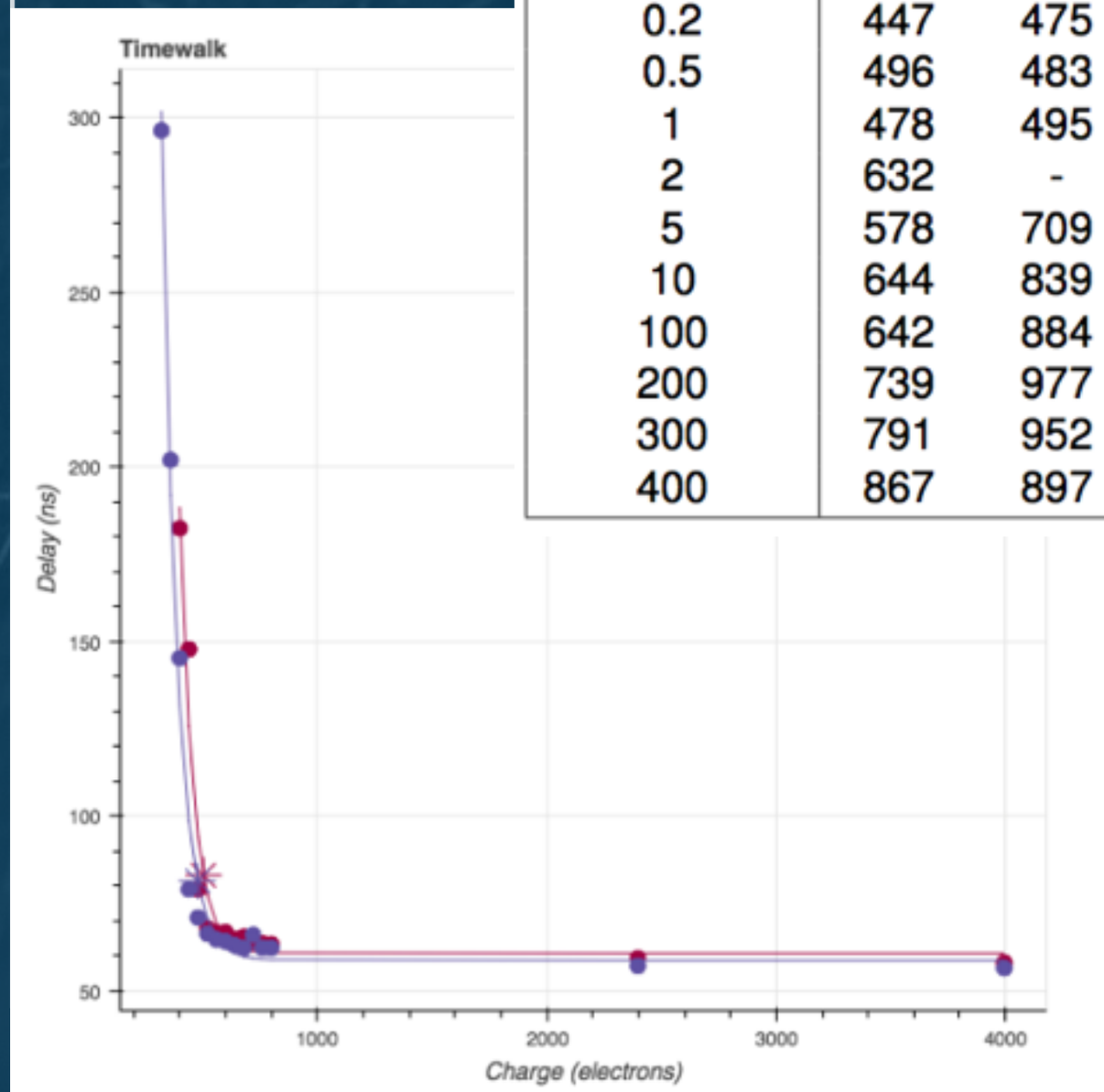


used for RD53A

no sensor

In-Time Threshold

Dose (Mrad)	In-time threshold (electrons)							
	col. 1	col. 2	col. 3	col. 4	col. 5	col. 6	col. 7	col. 8
0	453	443	477	490	478	442	472	430
0.1	452	456	486	531	454	441	519	449
0.2	447	475	545	426	487	455	454	524
0.5	496	483	498	418	422	562	487	507
1	478	495	511	463	476	524	510	611
2	632	-	526	484	485	515	533	617
5	578	709	545	741	648	524	520	999
10	644	839	666	770	691	559	540	1109
100	642	884	624	769	764	550	568	1155
200	739	977	714	780	807	575	546	1262
300	791	952	663	773	838	537	607	1157
400	867	897	640	807	895	582	613	1194



no sensor

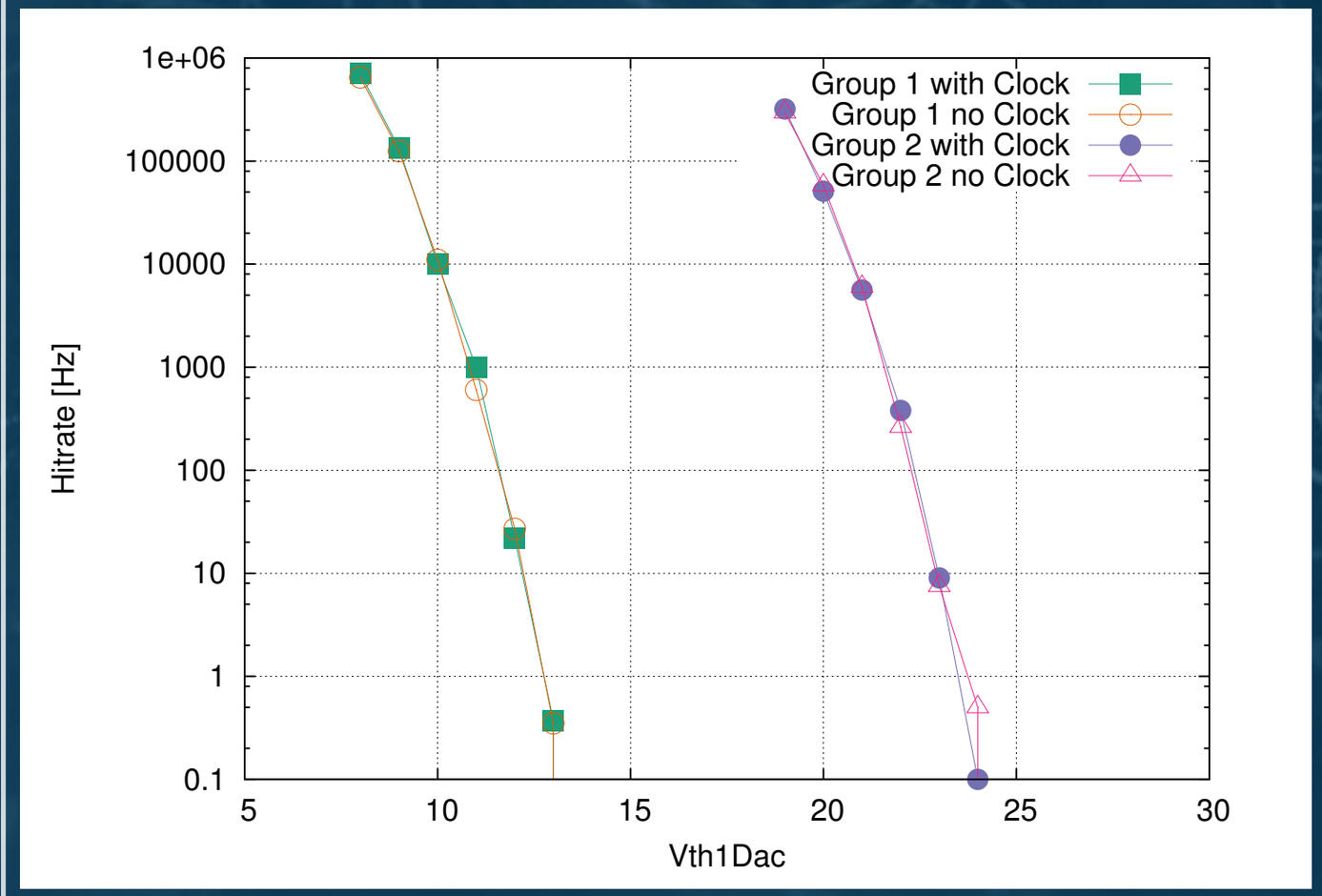
Time-walk:

- Min. charge resolved in 25ns (LHC bunch crossing frequency) = in-time threshold
- Here measured for single pixels
- Basically no time-walk before irradiation
- Timewalk still in specification (1000e in-time threshold) after irradiation

Isolation Strategy

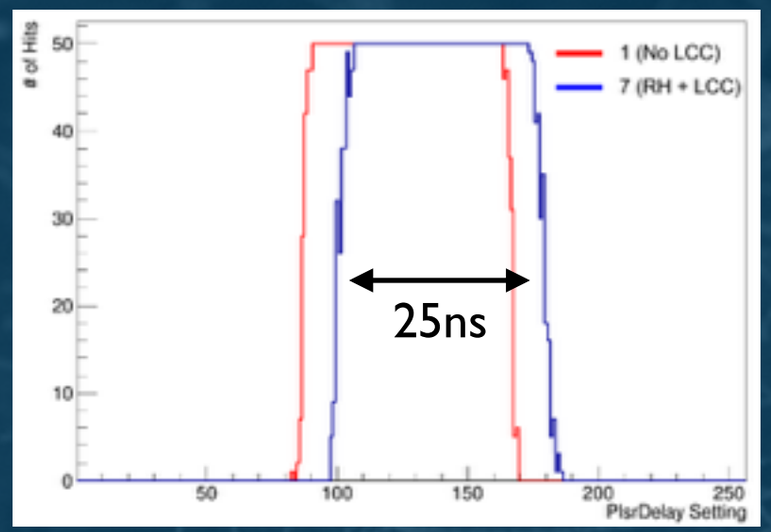
Isolation Strategy in FE65-P2:

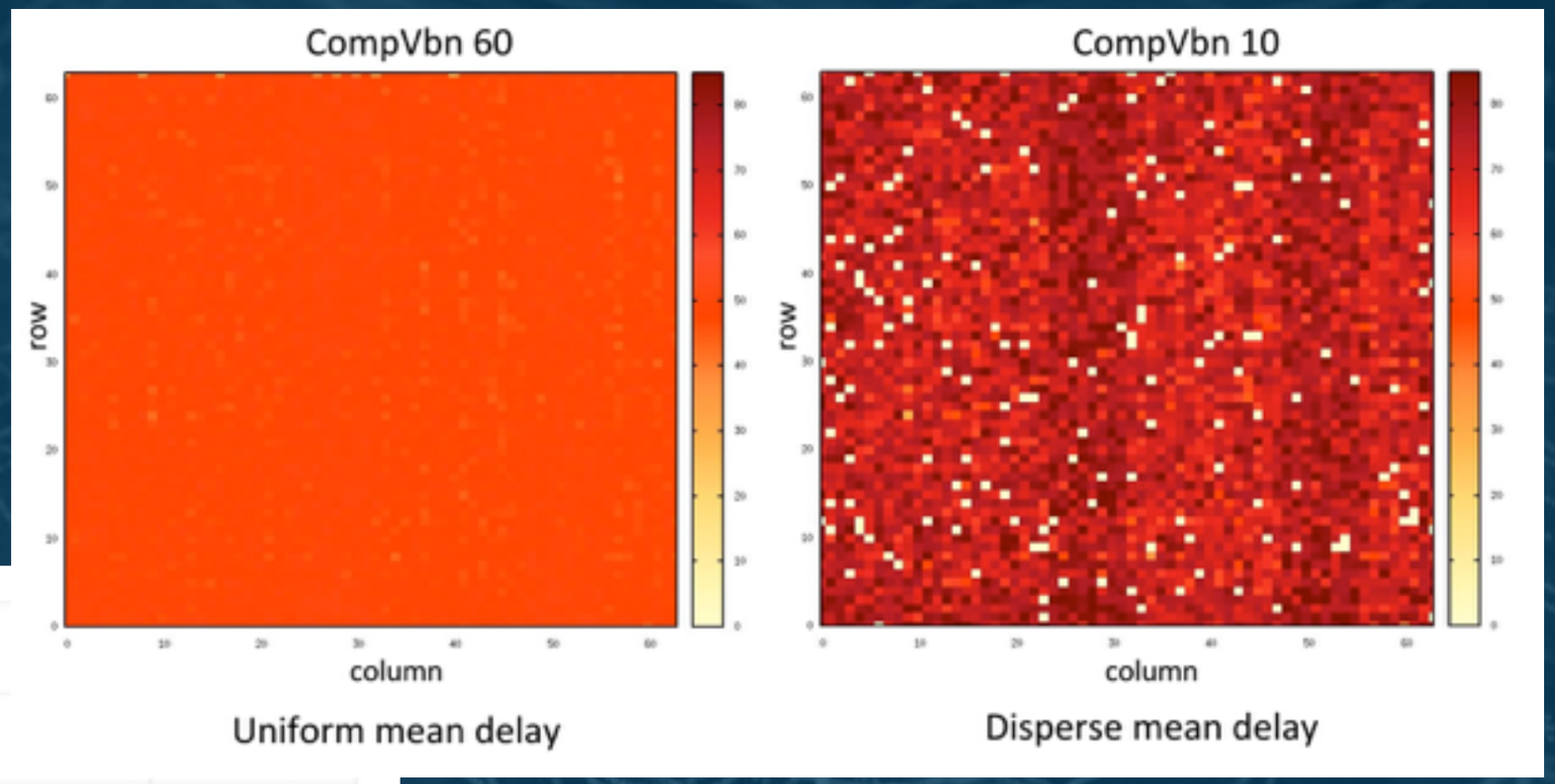
- Analog and digital in separate deep-N-wells
- Both are fully isolated from substrate
- Resubmitted FE65-P2 removing analog substrate isolation to test effect in apples to apples comparison

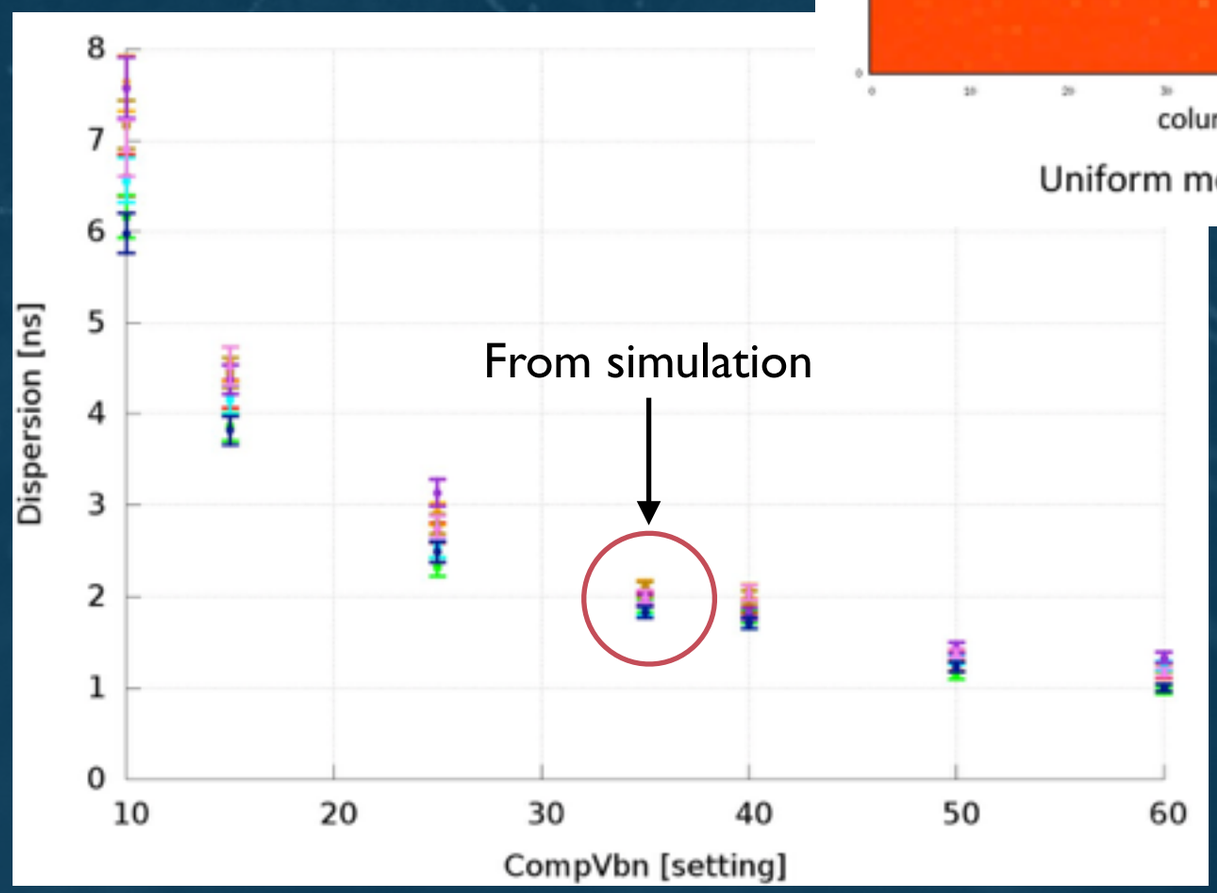


non irrad
no sensor

Discriminator Speed



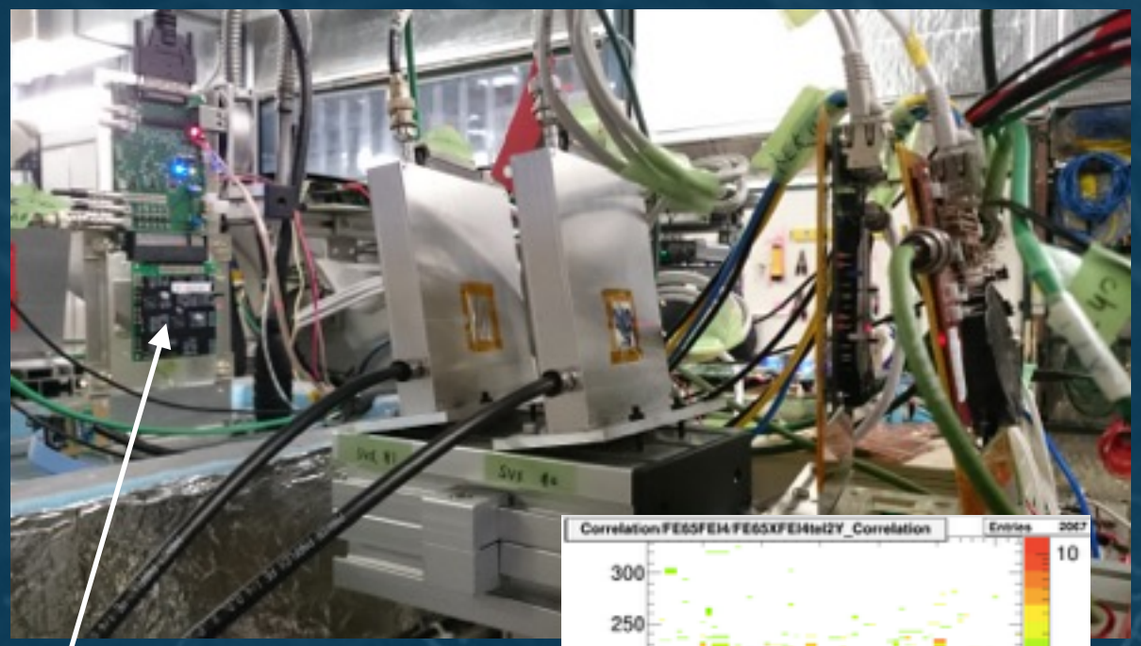




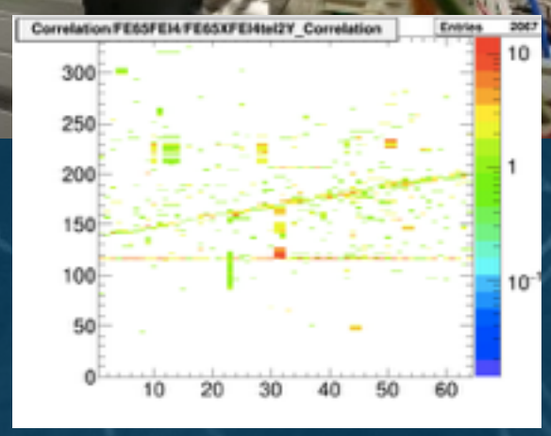
Trade-off:
higher CompVbn = less timing dispersion, but higher current consumption

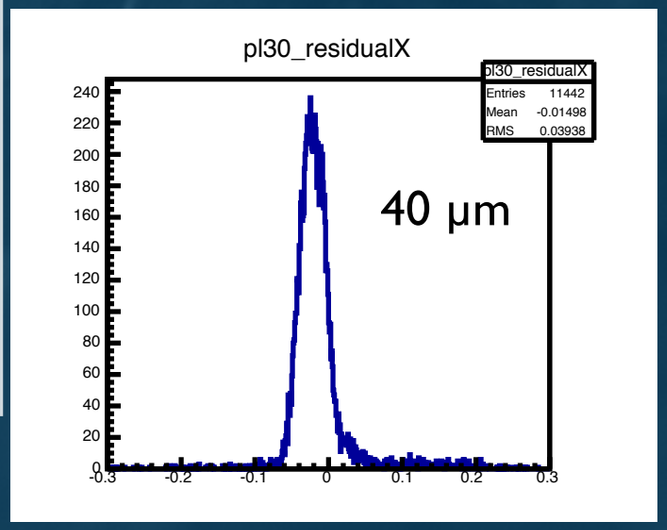
non irrad
no sensor

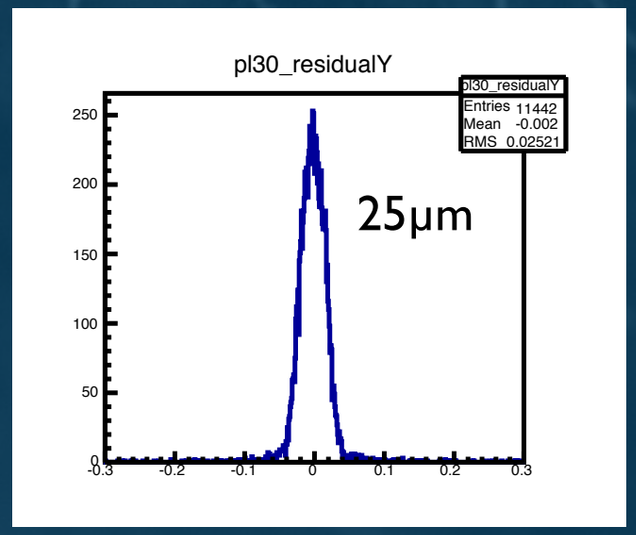
FE65P2 Sensor Module

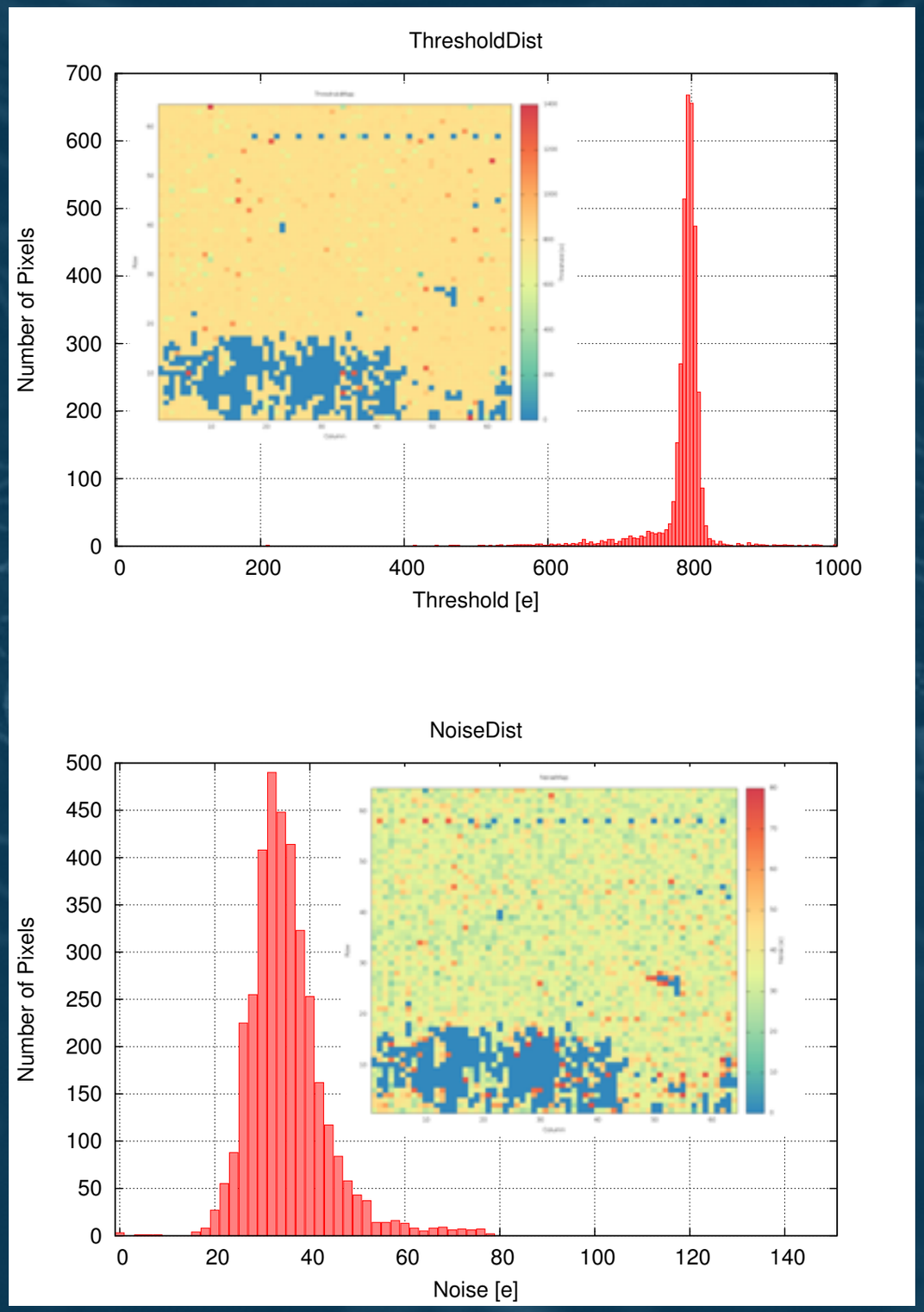


FE65P2









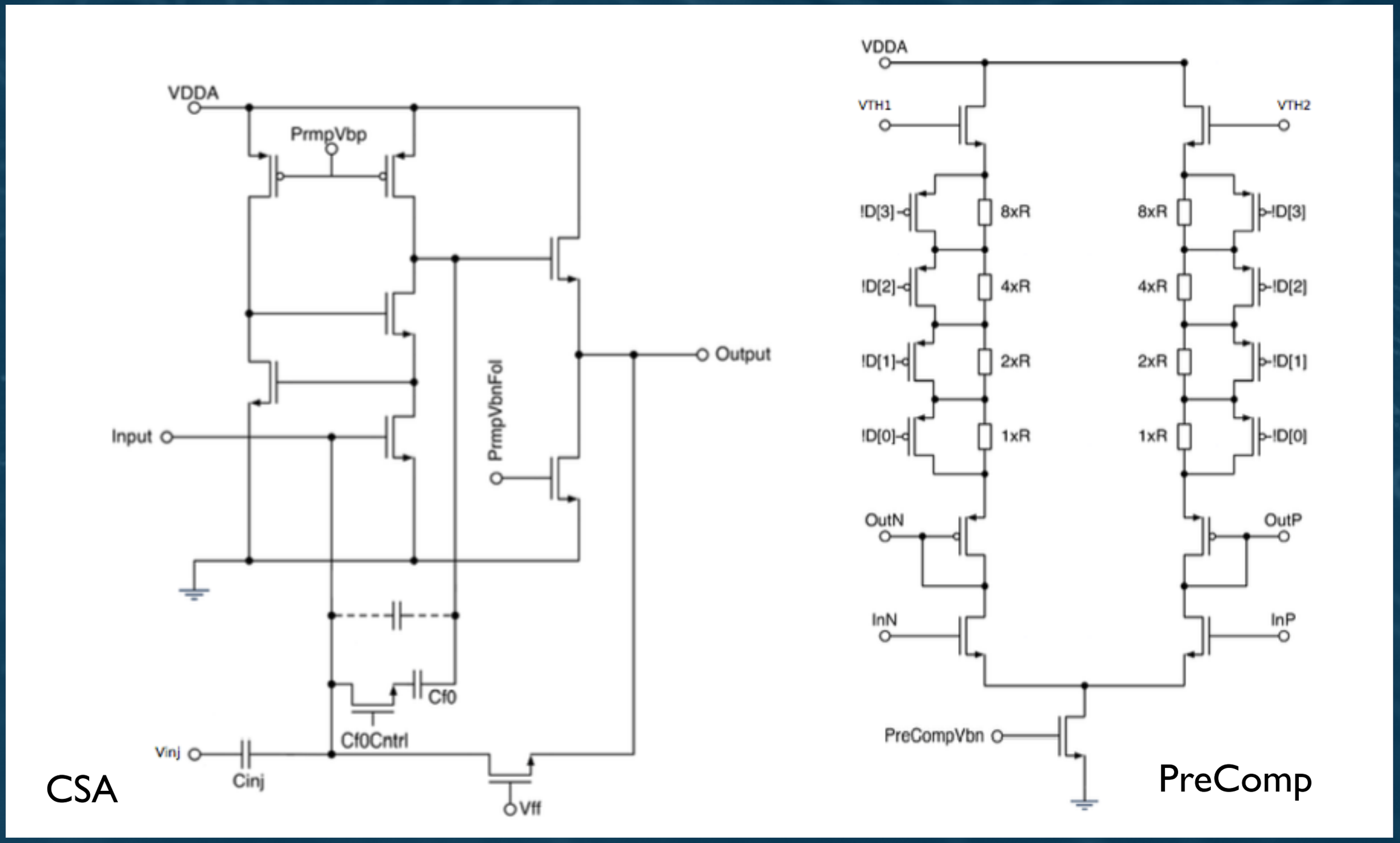
non irrad

Conclusion & Summary

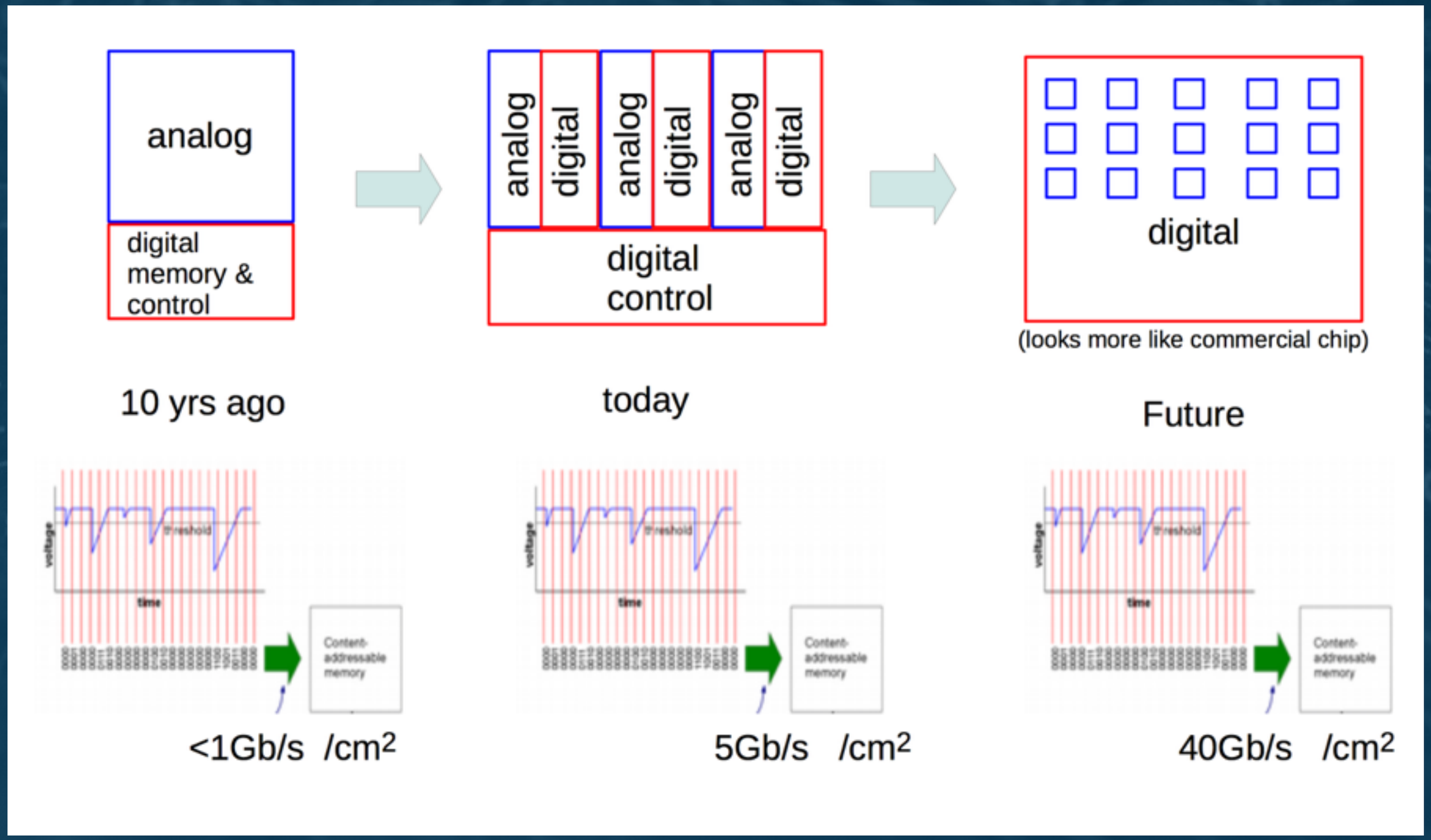
- FE65-P2 is a prototype readout chip with 50 x 50 μm^2 pixel size in a 64 by 64 pixel array manufactured in 65 nm
- The purpose of this chip is to test the design process in 65 nm and test the new analog pixel front end
- Low threshold operation down to 300e threshold and only 35e noise
- Successful irradiations up to 500 MRad with positive results
- Successfully assembled modules at SLAC with HPK planar sensors → Used for test beam measurements at SLAC & CERN for sensor irradiation studies
- Characterisation has led to improvements of the analog pixel front end for RD53A
- Resubmitted FE65-P2 (with RD53A) with modified isolation strategy

Backup

Diff. Front-End Schematic



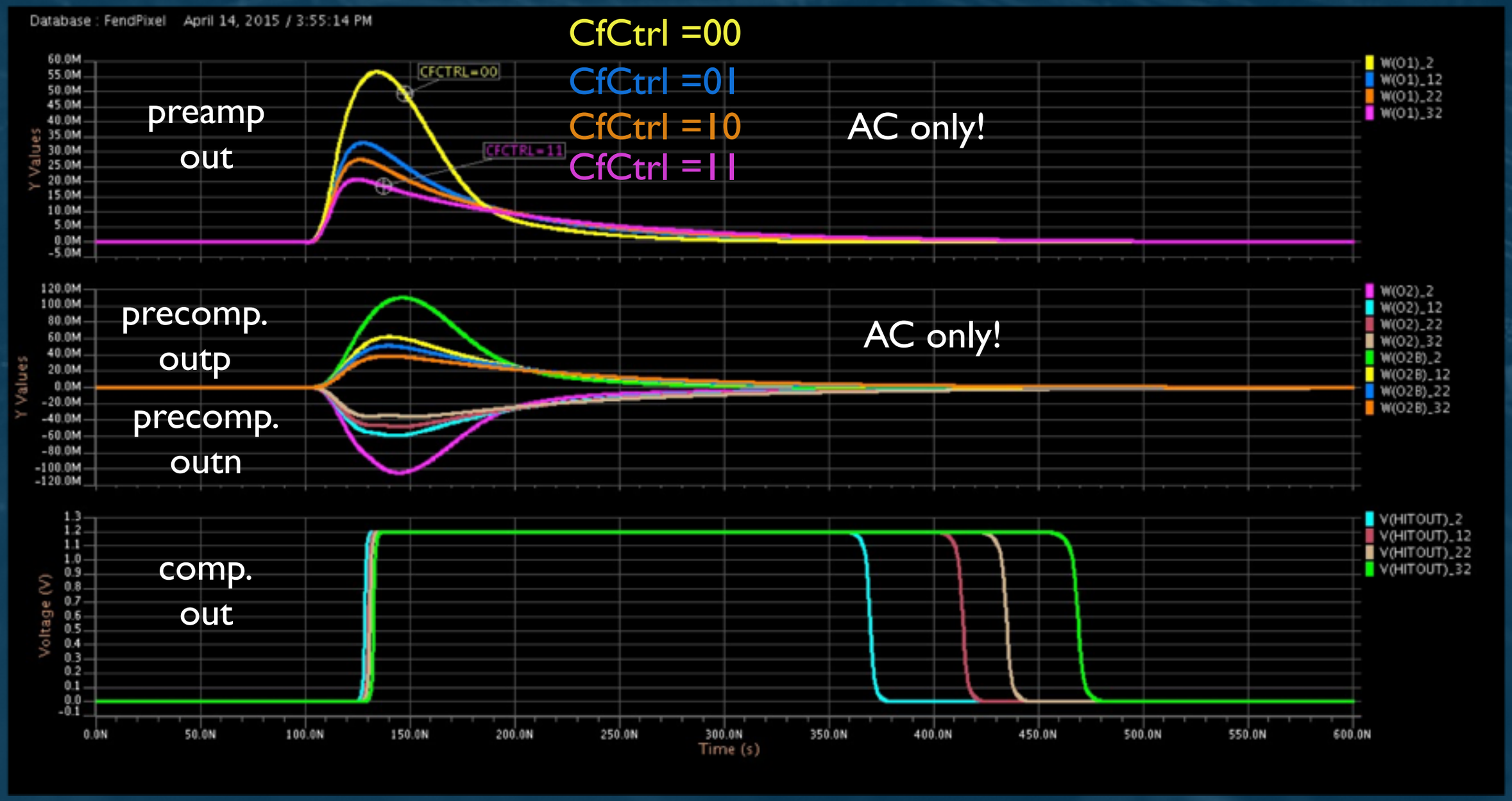
Design Process



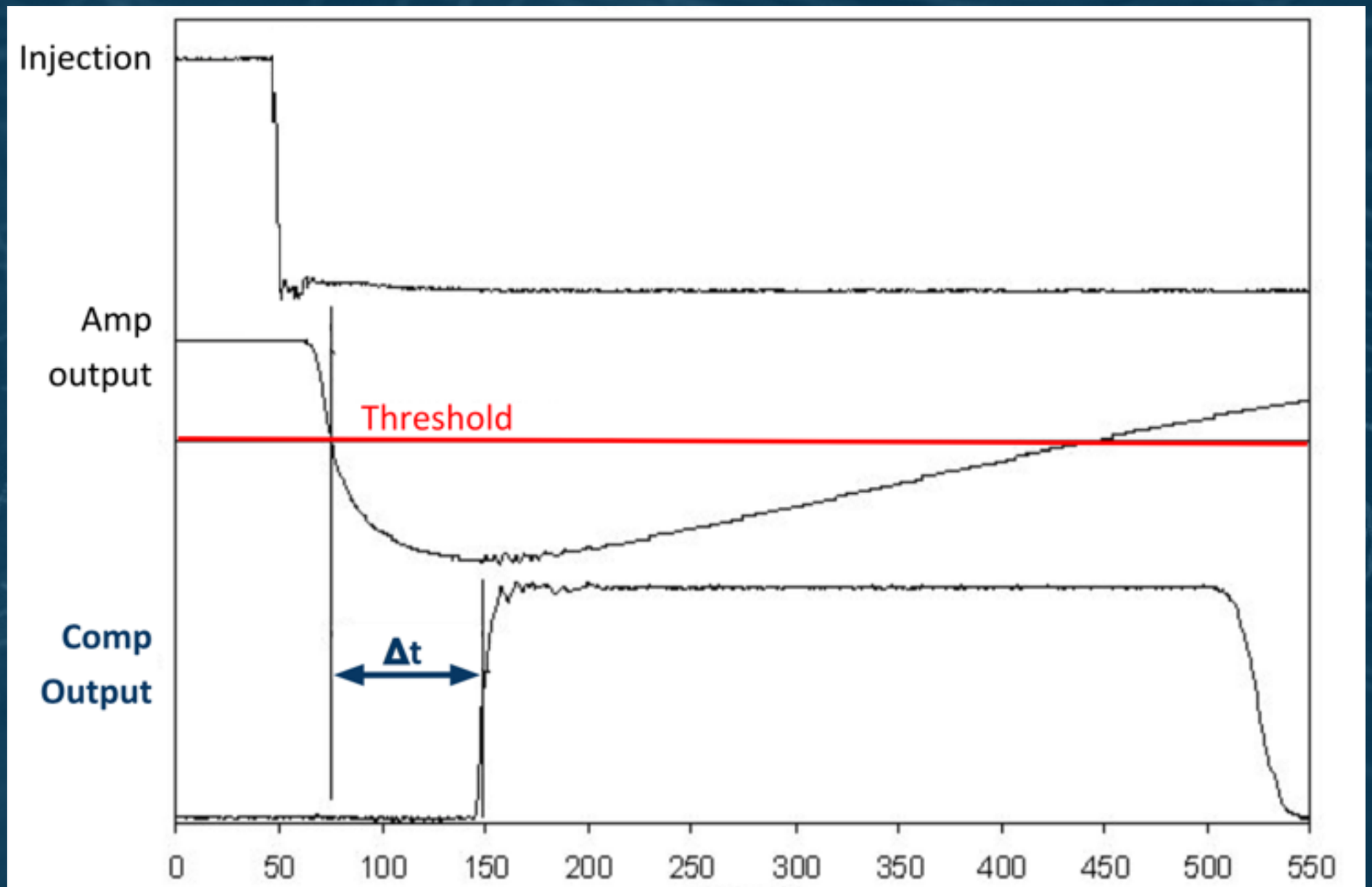
Simulation

Signal conversion:

- Qin = 2000e
- Varying feedback capacitance CfCtrl from 00 to 11

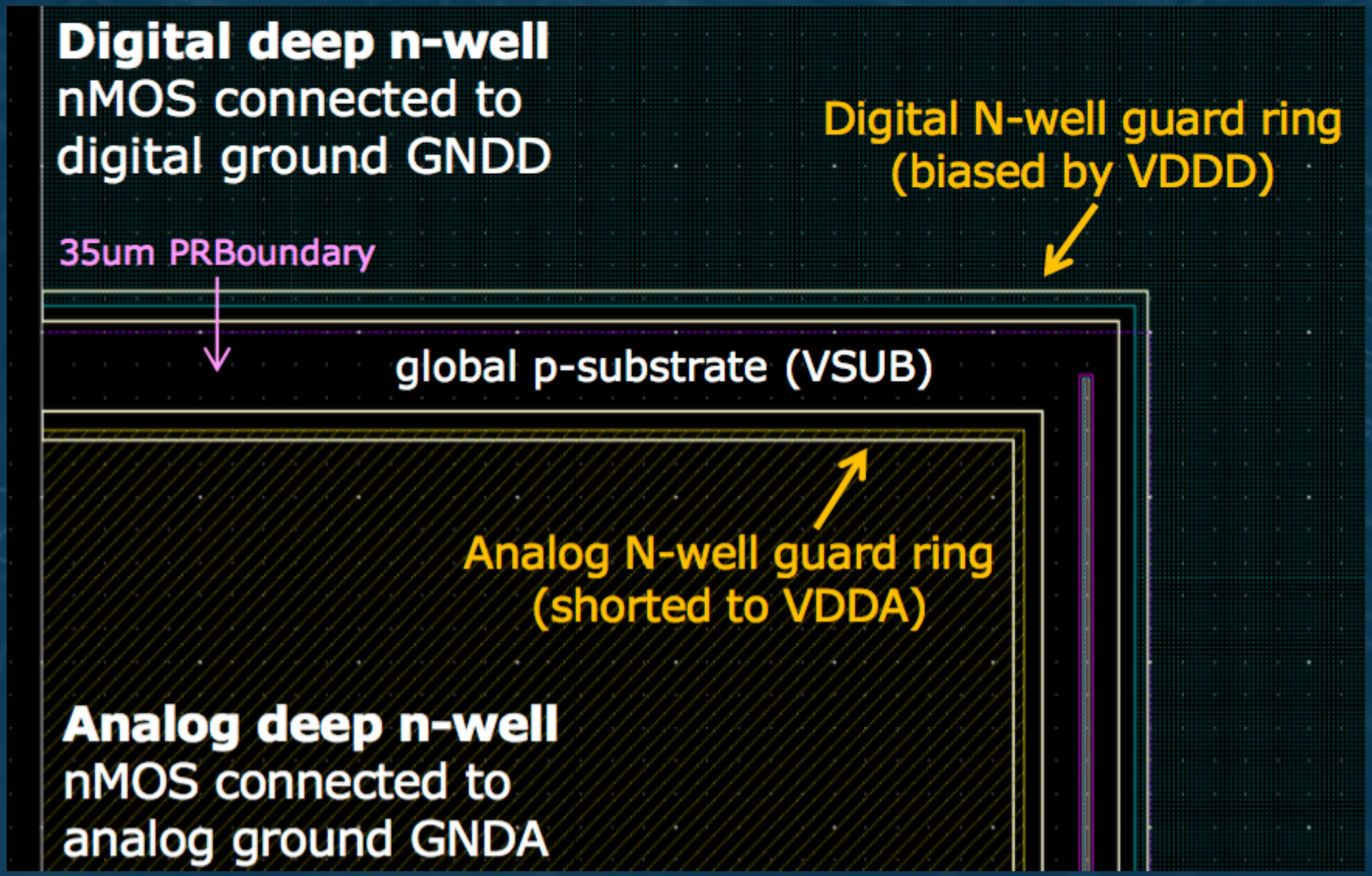


Timing Measurement



Δt between signal crossing threshold and output of comparator depends on **comparator current (CompVbn)**

Isolation


Digital deep n-well
nMOS connected to
digital ground GNDD
Digital N-well guard ring
(biased by VDDD)
35um PRBoundary
global p-substrate (VSUB)
Analog N-well guard ring
(shorted to VDDA)
Analog deep n-well
nMOS connected to
analog ground GNDA