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ALTIROC0, a 20 Pico-Second Time Resolution ASIC for the ATLAS High Granularity Timing Detector (HGTD)

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ALTIROC0 is an 8-channel ASIC prototype designed to readout 1x1 or 2x2 mm2 50 µm thick Low Gain Avalanche Diodes (LGAD) of the ATLAS HGTD detector. The targeted combined time resolution of the sensor and the readout electronics is 30 ps/MIP. Each analog channel of the ASIC must exhibit an extremely low jitter noise to ensure this challenging time resolution, while keeping a low power consumption of 2 mW/channel. A "Time Over Threshold"and a "Constant Fraction Discriminator"architecture are integrated to correct for the time walk.
The ASIC was received in April 2017 and testbench measurements will be presented.

Summary

The expected increase of the pile-up at the high luminosity phase of the LHC due to the 200 interactions per bunch crossing will have a severe impact on the physics. A High Granularity Timing Detector (HGTD) is proposed in front of the Liquid Argon End-Cap calorimeters for pile-up mitigation at Level-0 trigger level and in the offline reconstruction. Four layers of very thin Low Gain Avalanche Diodes (LGAD), with a transverse size of 1-2 mm2, are foreseen to provide precise timing information for charged and neutral particles with a time resolution of about 30 pico-seconds per MIP. The readout FE electronics is designed to cope with the high radiation and time resolution requirements while keeping a power dissipation lower than 2 mW/cell.

To preserve the excellent intrinsic time resolution of LGAD sensors (25 ps before irradiation for gain larger than 20), the front-end ASIC must exhibit an electronics jitter smaller than 20 ps for a MIP signal (10 fC for a LGAD with a gain of 20).

ALTIROC0 is a first ASIC prototype designed in TSMC 130 nm. It integrates 8 analog channels. Each one is made of a preamplifier followed by a discriminator, which are both determinant for the overall electronics time performance. The time resolution depends on the "electronics jitter"and the "Time Walk"effect. In the final version, a 20 ps-bin Time to Digital Convertor (TDC), a digital memory and a serializer will follow the discriminator to deliver real time digital data.
The input preamplifier is the cornerstone of the design to minimize the electronics jitter. The preamplifier must be very fast (Gain Bandwidth Product larger than 10 GHz) while exhibiting a noise smaller than 0.5 fC to ensure a Signal over Noise ratio of 10. Besides, the available power dissipation for the preamplifier must be smaller than 400 µW.
The discriminator is also crucial as it determines the time accuracy measurement. The Time Walk can be corrected using Time over Threshold (TOT) architecture or Constant Fraction Discriminator (CFD) architecture. The TOT technique requires calibration and offline correction, which prevents real time results and their use in the trigger path.
The Constant Fraction Discrimination option has also been integrated to compensate for the Time Walk effect as it eliminates the shortcomings of the classical TOT technique. The position of the discriminator pulse is independent of the original pulse amplitude, compensating naturally the Time Walk. Best CFDs integrated in ASICs so far have shown time walk limitations around 1 ns, making this 20 ps requirement more than an order of magnitude beyond the state of the art. Simulation results show a time resolution better than 30 ps

for input signals varying from 1 to 10 MIP. The actual time performance of the chip and the sensitivity of the integrated CFD to the pulse shape variation must be studied in real conditions.

The ALTIROC0 ASIC was received in April 2017. Its overall performance on test bench and with LGAD sensors will be presented in this presentation.

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